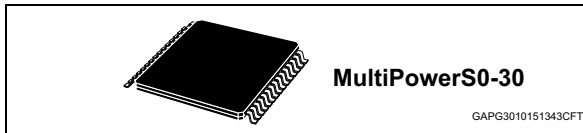


Double 4mΩ high-side driver with analog CurrentSense for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	4 mΩ
Current limitation (typ)	I_{LIMH}	90 A
Off-state supply current	I_S	2 μA ⁽¹⁾

1. Typical value with all loads connected

- Automotive qualified
- General
 - Very low standby current
 - 3.0 V CMOS compatible inputs
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - Compliant with European directive 2002/95/EC
 - Very low current sense leakage
- Diagnostic functions
 - Proportional load current sense
 - High current sense precision for wide currents range
 - Diagnostic enable pin
 - Off-state open-load detection
 - Output short to V_{CC} detection
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
- Protection
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients

- Protection against loss of ground and loss of V_{CC}
- Overtemperature shutdown with auto restart (thermal shutdown)
- Inrush current active management by power limitation
- Reverse battery protection with self switch on of the Power MOSFET
- Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

Description

The device is a double channel high-side driver manufactured using ST proprietary VIPower[®] M0-5 technology and housed in a MultiPowerSO-30 package. The device is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to V_{CC} diagnosis and on-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the DE pin low to share the external sense resistor with similar devices.

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1 Block diagram and pin configurations

Figure 1. Block diagram

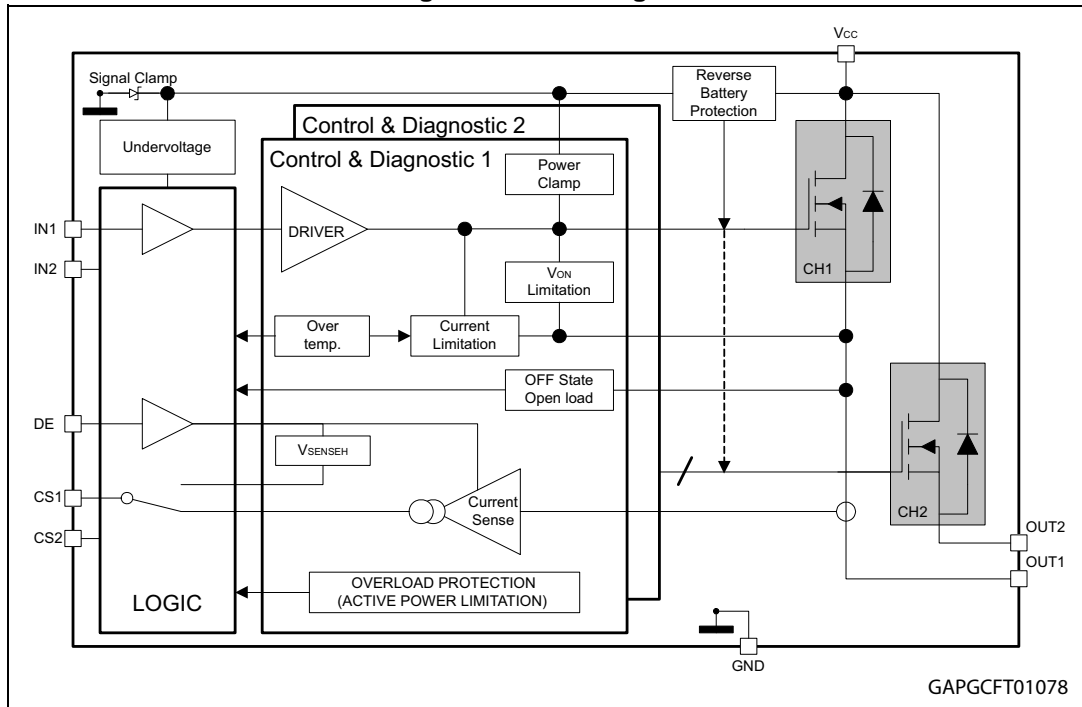


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection
OUT1,2	Power output
GND	Ground connection
IN1,2	Voltage controlled input pin with hysteresis, CMOS compatible, controls output switch state
CS1,2	Analog current sense pin; delivers a current proportional to the load current
DE	Active high diagnostic enable pin

Figure 2. Configuration diagram (not in scale)

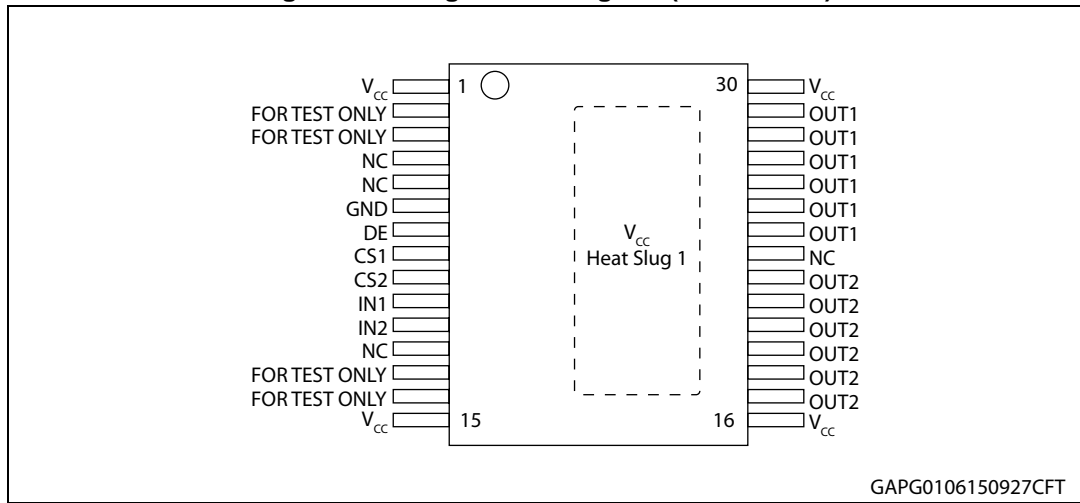


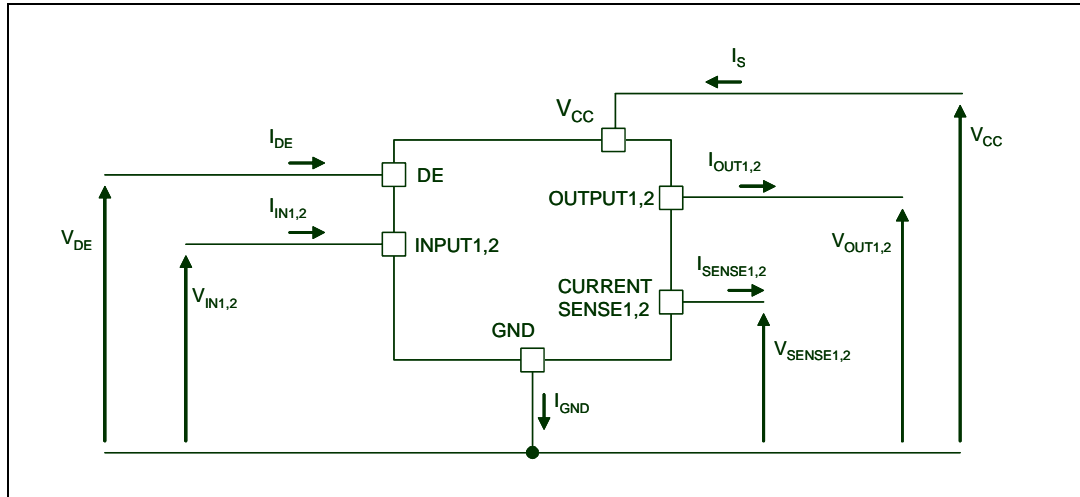
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CurrentSense	NC ⁽¹⁾	Output	Input	DE	For test only
Floating	Not allowed	X	X	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor	Through 10 kΩ resistor	Not allowed

1. Not connected

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Applying stress which exceeds above the ratings listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage ($T < 400$ ms, $R_{load} > 0.5 \Omega$)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	70	A
I_{IN}	DC input current	-1 to 10	mA
I_{DE}	DC diagnostic enable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage ($V_{CC} > 0$ V)	$V_{CC} - 41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 0.3$ mH; $R_L = 0 \Omega$; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}(Typ.)$)	600	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: $R = 1.5$ k Ω ; $C = 100$ pF)	2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	0.35	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	58 ⁽¹⁾	°C/W

1. PCB FR4 area 58 mm x 58 mm, PCB thickness 2 mm, Cu thickness 35 μm, minimum pad layout

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 24\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 15\text{ A}; T_j = 25\text{ °C}$		3		mΩ
		$I_{OUT} = 15\text{ A}; T_j = 150\text{ °C}$			6	mΩ
		$I_{OUT} = 15\text{ A}; V_{CC} = 5\text{ V}; T_j = 25\text{ °C}$			6	mΩ
$R_{ON REV}$	R_{DSon} in reverse battery condition	$V_{CC} = -13\text{ V}; I_{OUT} = -15\text{ A}; T_j = 25\text{ °C}$		3		mΩ
V_{clamp}	V_{CC} clamp voltage	$I_{CC} = 20\text{ mA}; I_{OUT1,2} = 0\text{ A}$	41	46	52	V
I_S	Supply current	Standby $V_{DE} = 0\text{ V}; V_{CC} = 13\text{ V}; T_j = 25\text{ °C}; V_{IN} = 0;$ $V_{OUT} = V_{SENSE} = 0\text{ V}$		2	5	μA
		Off-state; $V_{CC} = 13\text{ V}; V_{DE} = 5\text{ V}; T_j = 25\text{ °C};$ $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		10	15	μA
		On-state; $V_{CC} = 13\text{ V}; V_{DE} = 5\text{ V}; V_{IN} = 5\text{ V}; I_{OUT} = 0\text{ A}$		3.5	6	mA

Table 5. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off)}$	Off-state output current ⁽¹⁾	$V_{IN} = 0\text{ V}$ or $V_{DE} = 0\text{ V}$; $V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$	0	0.01	3	μA
		$V_{IN} = 0\text{ V}$ or $V_{DE} = 0\text{ V}$; $V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_j = 125\text{ °C}$	0		5	μA

1. For each channel

Table 6. Switching ($V_{CC} = 13\text{ V}$; $T_j = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 0.87\ \Omega$ (see Figure 6)	—	25	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 0.87\ \Omega$ (see Figure 6)	—	35	—	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 0.87\ \Omega$	—	See Figure 26	—	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 0.87\ \Omega$	—	See Figure 28	—	$\text{V}/\mu\text{s}$
W_{ON}	Switching energy losses during t_{won}	$R_L = 0.87\ \Omega$ (see Figure 6)	—	5.4	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L = 0.87\ \Omega$ (see Figure 6)	—	2.3	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL1,2}$	Input low level voltage				0.9	V
$I_{IL1,2}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
$V_{IH1,2}$	Input high level voltage		2.1			V
$I_{IH1,2}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{I(hyst)1,2}$	Input hysteresis voltage		0.25			V
$V_{ICL1,2}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
V_{DEL}	DE low level voltage				0.9	V
I_{DEL}	DE low level current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{DEH}	DE high level voltage		2.1			V
I_{DEH}	DE high level current	$V_{IN} = 2.1\text{ V}$			10	μA
$V_{DE(hyst)}$	DE hysteresis voltage		0.25			V
V_{DECL}	DE clamp voltage	$I_{DE} = 1\text{ mA}$	5.5		7	V
		$I_{DE} = -1\text{ mA}$		-0.7		V

Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	$V_{CC} = 13\text{ V}$	65	90	130	A
		$5\text{ V} < V_{CC} < 24\text{ V}$			130	A
I_{limL}	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V};$ $T_R < T_j < T_{TSD}$		40		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		$T_{RS}+1$	$T_{RS}+5$		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis ($T_{TSD}-T_R$)			7		°C
V_{DEMG}	Turn-off output voltage clamp	$I_{OUT} = 2\text{ A}; V_{IN} = 0;$ $L = 6\text{ mH}$	$V_{CC}-28$	$V_{CC}-32$	$V_{CC}-35$	V
V_{ON}	Output voltage drop limitation	$I_{OUT} = 1\text{ A};$ $T_j = -40\text{ °C to }150\text{ °C}$ (see Figure 8)		25		mV

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	$I_{OUT} = 5\text{ A}; V_{SENSE} = 4\text{ V}; V_{DE} = 5\text{ V};$ $T_j = -40\text{ °C to }150\text{ °C}$ $T_j = 25\text{ °C to }150\text{ °C}$	11420 12130	17580 17580	23740 23030	—
K_1	I_{OUT}/I_{SENSE}	$I_{OUT} = 10\text{ A}; V_{SENSE} = 4\text{ V}; V_{DE} = 5\text{ V};$ $T_j = -40\text{ °C to }150\text{ °C}$ $T_j = 25\text{ °C to }150\text{ °C}$	11830 12680	16910 16910	21990 21140	—
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 10\text{ A}; V_{SENSE} = 4\text{ V}; V_{DE} = 5\text{ V};$ $T_j = -40\text{ °C to }150\text{ °C}$	-14		14	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT} = 15\text{ A}; V_{SENSE} = 4\text{ V}; V_{DE} = 5\text{ V};$ $T_j = -40\text{ °C to }150\text{ °C}$ $T_j = 25\text{ °C to }150\text{ °C}$	11760 13040	16110 16110	20460 19180	—
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 15\text{ A}; V_{SENSE} = 4\text{ V};$ $V_{DE} = 5\text{ V}; T_j = -40\text{ °C to }150\text{ °C}$	-10		10	%
K_3	kI_{OUT}/I_{SENSE}	$I_{OUT} = 30\text{ A}; V_{SENSE} = 4\text{ V}; V_{DE} = 5\text{ V};$ $T_j = -40\text{ °C to }150\text{ °C}$ $T_j = 25\text{ °C to }150\text{ °C}$	13040 13810	15520 15520	18000 17230	—
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 30\text{ A}; V_{SENSE} = 4\text{ V};$ $V_{DE} = 5\text{ V}; T_j = -40\text{ °C to }150\text{ °C}$	-5		5	%

Table 9. Current sense ($8\text{ V} < V_{CC} < 18\text{ V}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	Analog sense leakage current	$I_{\text{OUT}} = 0\text{ A}$; $V_{\text{SENSE}} = 0\text{ V}$; $V_{\text{DE}} = 0\text{ V}$; $V_{\text{IN}} = 0\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	0		1	μA
		$I_{\text{OUT}} = 0\text{ A}$; $V_{\text{SENSE}} = 0\text{ V}$; $V_{\text{DE}} = 5\text{ V}$; $V_{\text{IN}} = 5\text{ V}$; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	0		2	μA
		$I_{\text{OUT}} = 15\text{ A}$; $V_{\text{SENSE}} = 0\text{ V}$; $V_{\text{DE}} = 0\text{ V}$; $V_{\text{IN}} = 5\text{ V}$;	0		1	μA
I_{OL}	Open-load on-state current detection threshold	$V_{\text{IN}} = 5\text{ V}$; $8\text{ V} < V_{CC} < 18\text{ V}$ $I_{\text{SENSE}} = 5\text{ }\mu\text{A}$	10		150	mA
V_{SENSE}	Max analog sense output voltage	$I_{\text{OUT}} = 45\text{ A}$; $V_{\text{CSD}} = 0\text{ V}$; $R_{\text{SENSE}} = 3.9\text{ k}\Omega$	5			V
V_{SENSEH}	Analog sense output voltage in fault condition ⁽²⁾	$V_{CC} = 13\text{ V}$; $R_{\text{SENSE}} = 3.9\text{ k}\Omega$		8		V
I_{SENSEH}	Analog sense output current in fault condition ⁽²⁾	$V_{CC} = 13\text{ V}$; $V_{\text{SENSE}} = 5\text{ V}$		9		mA
t_{DSENSE1H}	Delay response time from rising edge of DE pin	$V_{\text{SENSE}} < 4\text{ V}$; $5\text{ A} < I_{\text{OUT}} < 30\text{ A}$; $I_{\text{SENSE}} = 90\%$ of $I_{\text{SENSE max}}$ (see Figure 4)		50	100	μs
t_{DSENSE1L}	Delay response time from falling edge of DE pin	$V_{\text{SENSE}} < 4\text{ V}$; $5\text{ A} < I_{\text{OUT}} < 30\text{ A}$; $I_{\text{SENSE}} = 10\%$ of $I_{\text{SENSE max}}$ (see Figure 4)		5	20	μs
t_{DSENSE2H}	Delay response time from rising edge of INPUT pin	$V_{\text{SENSE}} < 4\text{ V}$; $5\text{ A} < I_{\text{OUT}} < 30\text{ A}$; $I_{\text{SENSE}} = 90\%$ of $I_{\text{SENSE max}}$ $V_{\text{DE}} = 5\text{ V}$ (see Figure 4)		200	600	μs
t_{DSENSE2L}	Delay response time from falling edge of INPUT pin	$V_{\text{SENSE}} < 4\text{ V}$; $5\text{ A} < I_{\text{out}} < 30\text{ A}$; $I_{\text{SENSE}} = 10\%$ of $I_{\text{SENSE max}}$ $V_{\text{DE}} = 5\text{ V}$ (see Figure 4)		100	250	μs

1. Parameter guaranteed by design; it is not tested.

2. Fault condition includes: power limitation, overtemperature and open-load off-state detection.

Table 10. Open-load detection ($8\text{ V} < V_{CC} < 18\text{ V}$; $V_{\text{DE}} = 5\text{ V}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off-state voltage detection threshold	$V_{\text{IN}} = 0\text{ V}$, $V_{\text{DE}} = 5\text{ V}$; See Figure 5	2	—	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	$V_{\text{DE}} = 5\text{ V}$; See Figure 5	180	—	1200	μs
$I_{\text{L(off2)r}}$	Off-state output current at $V_{\text{OUT}} = 4\text{ V}$	$V_{\text{IN}} = 0\text{ V}$; $V_{\text{SENSE}} = 0\text{ V}$; $V_{\text{DE}} = 5\text{ V}$; V_{OUT} rising from 0 V to 4 V	-120	—	90	μA

Table 10. Open-load detection ($8\text{ V} < V_{CC} < 18\text{ V}$; $V_{DE} = 5\text{ V}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off2)f}$	Off-state output current at $V_{OUT} = 2\text{ V}$	$V_{IN} = 0\text{ V}$; $V_{SENSE} = V_{SENSEH}$; $V_{DE} = 5\text{ V}$; V_{OUT} falling from V_{CC} to 2 V	-50	—	90	μA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open-load	$V_{OUT} = 4\text{ V}$; $V_{IN} = 0\text{ V}$; $V_{DE} = 5\text{ V}$; $V_{SENSE} = 90\%$ of V_{SENSEH}		—	20	μs
td_voh	Delay response from output falling edge to V_{SENSE} falling edge in open-load	$V_{OUT} = 2\text{ V}$; $V_{IN} = 0\text{ V}$; $V_{DE} = 5\text{ V}$; $V_{SENSE} = 10\%$ of V_{SENSEH}		—	20	μs

Figure 4. CurrentSense delay characteristics

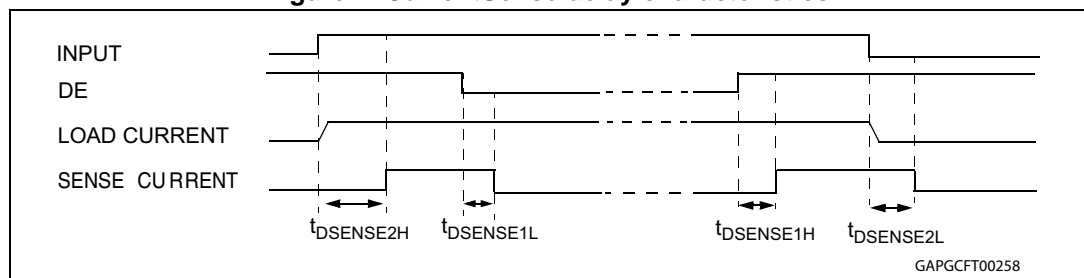


Figure 5. Open-load off-state delay timing

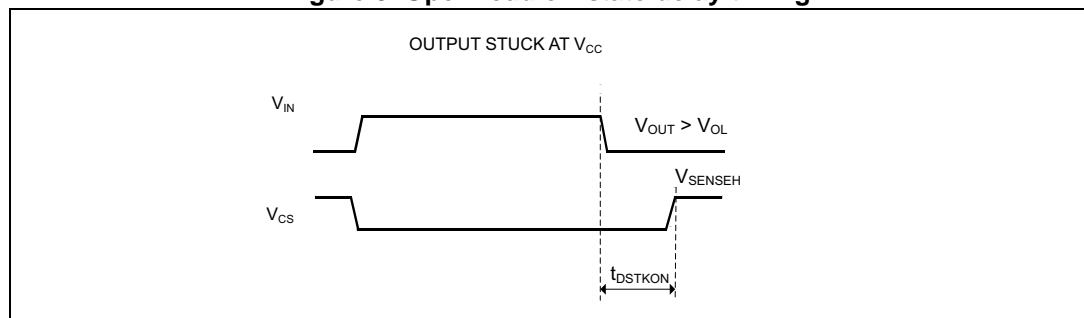
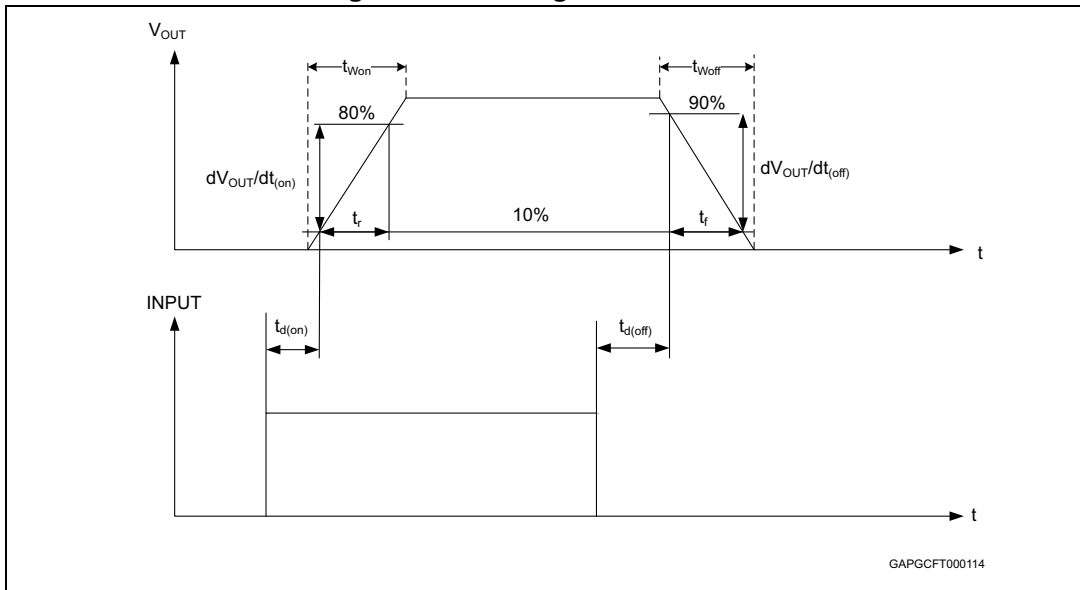
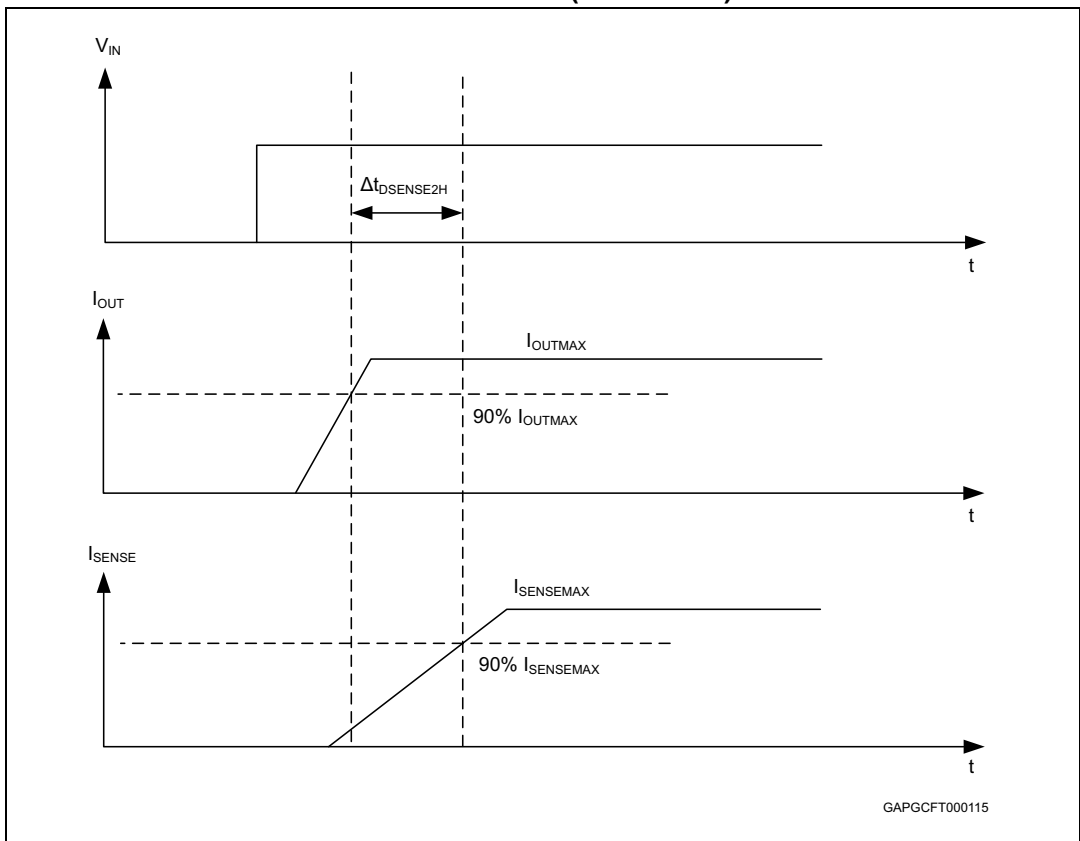


Figure 6. Switching characteristics



GAPGCFT000114

Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)



GAPGCFT000115

Figure 8. Output voltage drop limitation

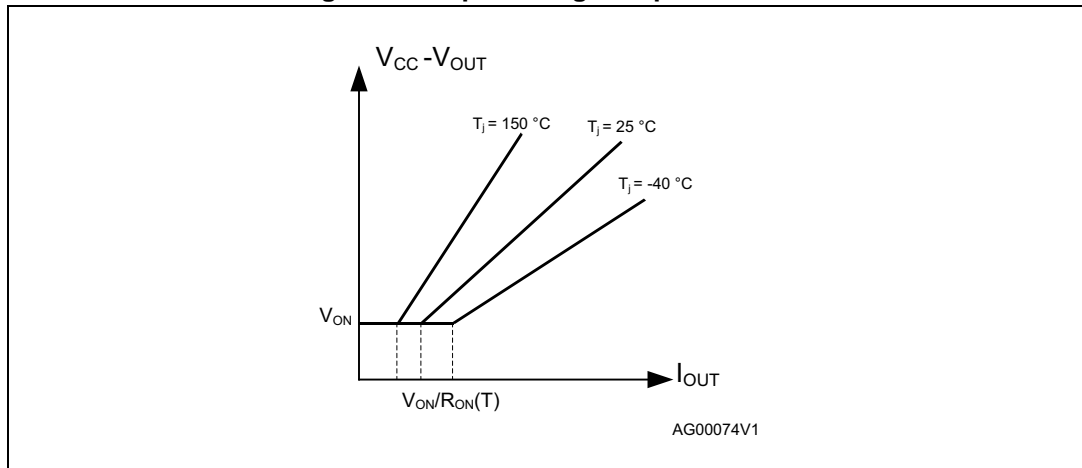


Figure 9. IOUT/ISENSE vs IOUT

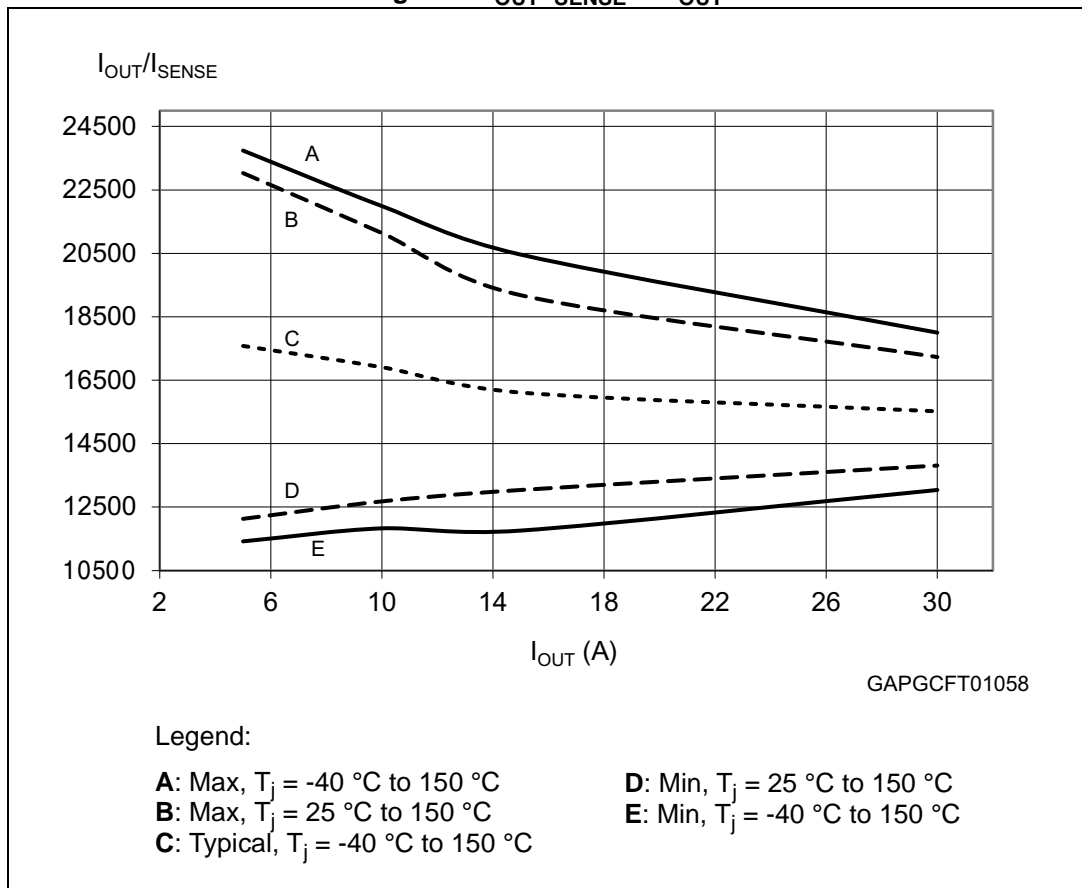
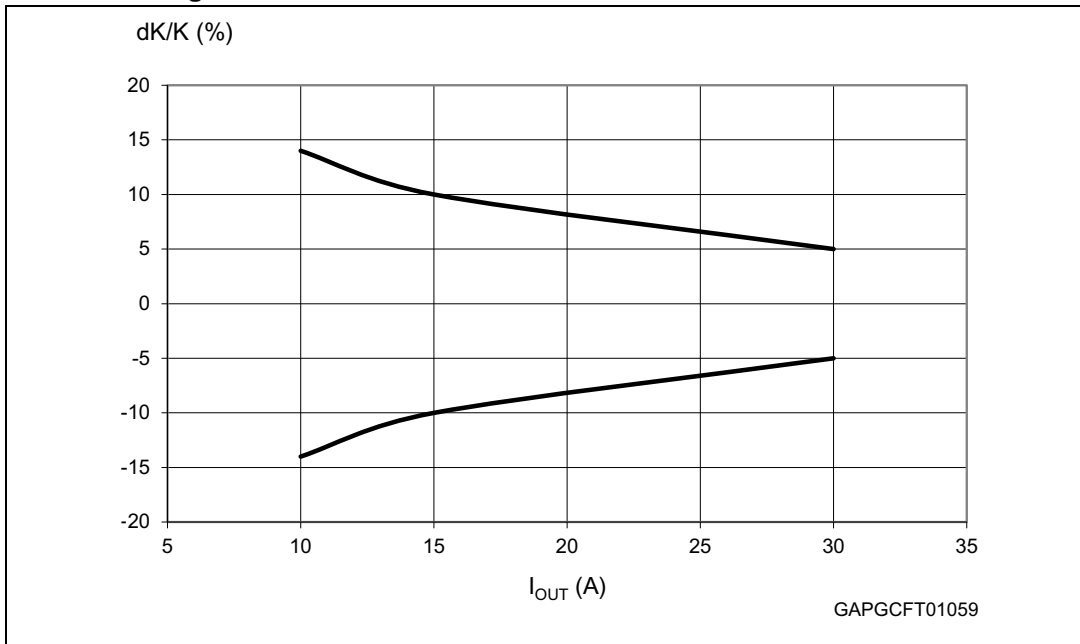


Figure 10. Maximum current sense ratio drift vs load current



1. Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Enable	Input	Output	Sense ($V_{DE}=5V$) ⁽¹⁾
Normal operation	H	L	L	0
	H	H	H	Nominal
Overtemperature	H	L	L	0
	H	H	L	V_{SENSEH}
Undervoltage	H	L	L	0
	H	H	L	0
Overload	H	H	X (no power limitation)	Nominal
	H	H	Cycling (power limitation)	V_{SENSEH}
Short circuit to GND (Power limitation)	H	L	L	0
	H	H	L	V_{SENSEH}
Open-load off-state (with external pull up)	H	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	H	L	H	V_{SENSEH}
	H	H	H	$V_{SENSEH} < \text{Nominal}$
Negative output voltage clamp	H	L	L	0

1. If the V_{DE} is low, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) Test pulse	Test levels ⁽¹⁾		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to Vcc = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) Test pulse	Test level results ⁽¹⁾	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b ⁽²⁾ (3)	C	C

1. The above test levels must be considered referred to Vcc = 13.5V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 3](#).

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

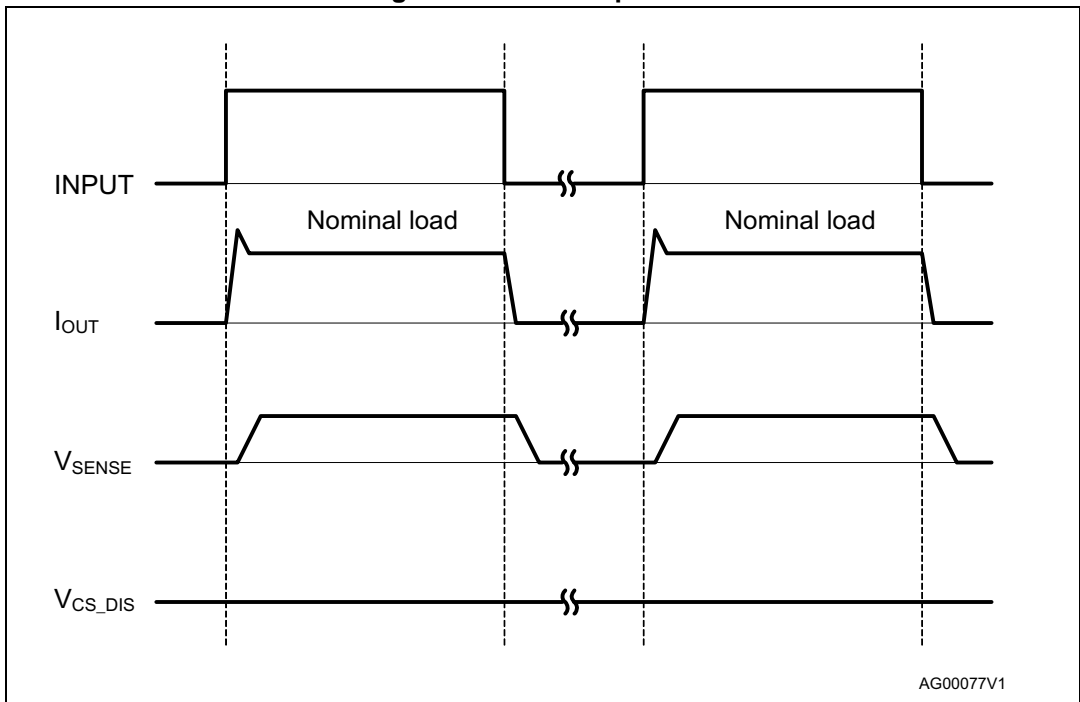


Figure 12. Overload or short to GND

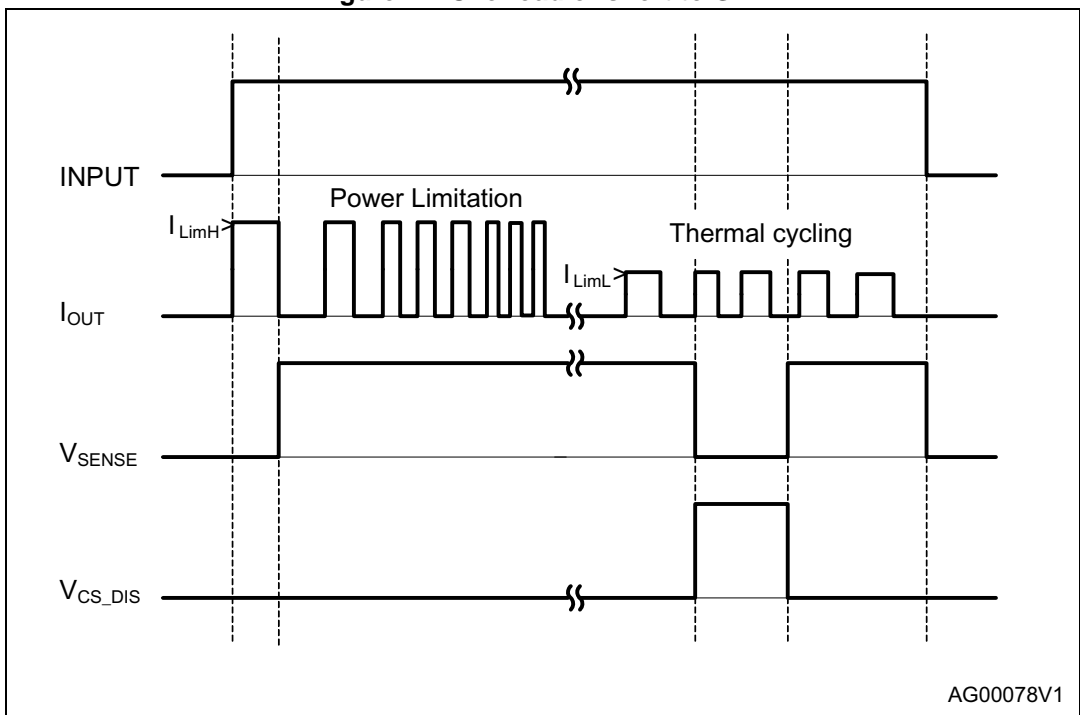


Figure 13. Intermittent overload

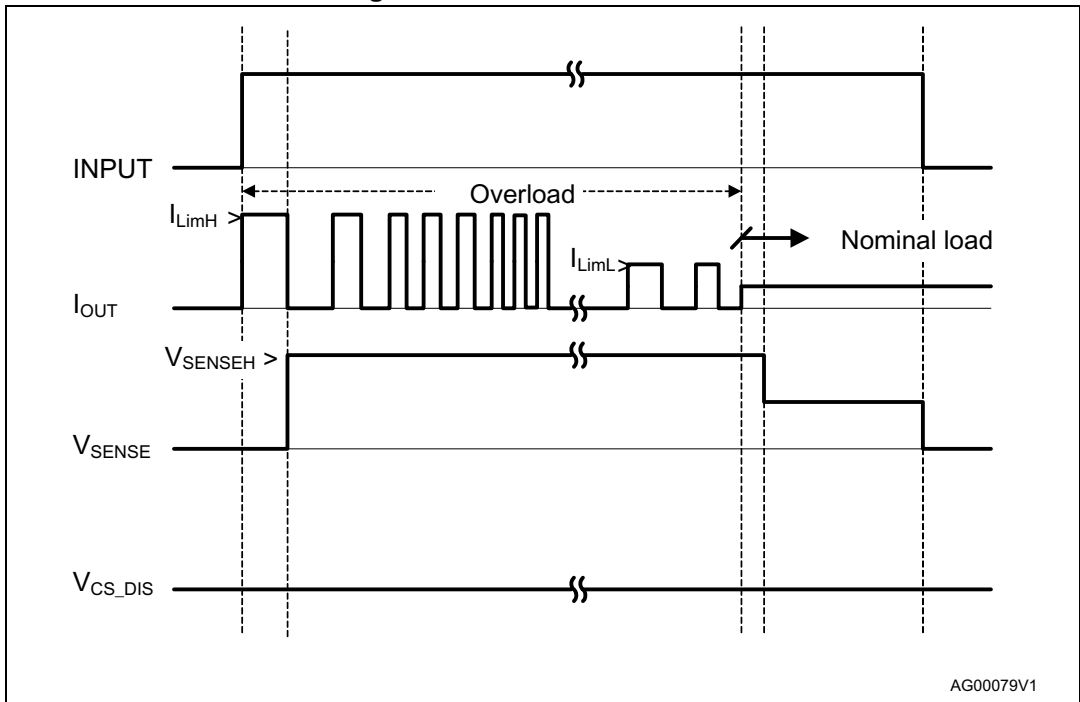


Figure 14. Off-state open-load with external circuitry

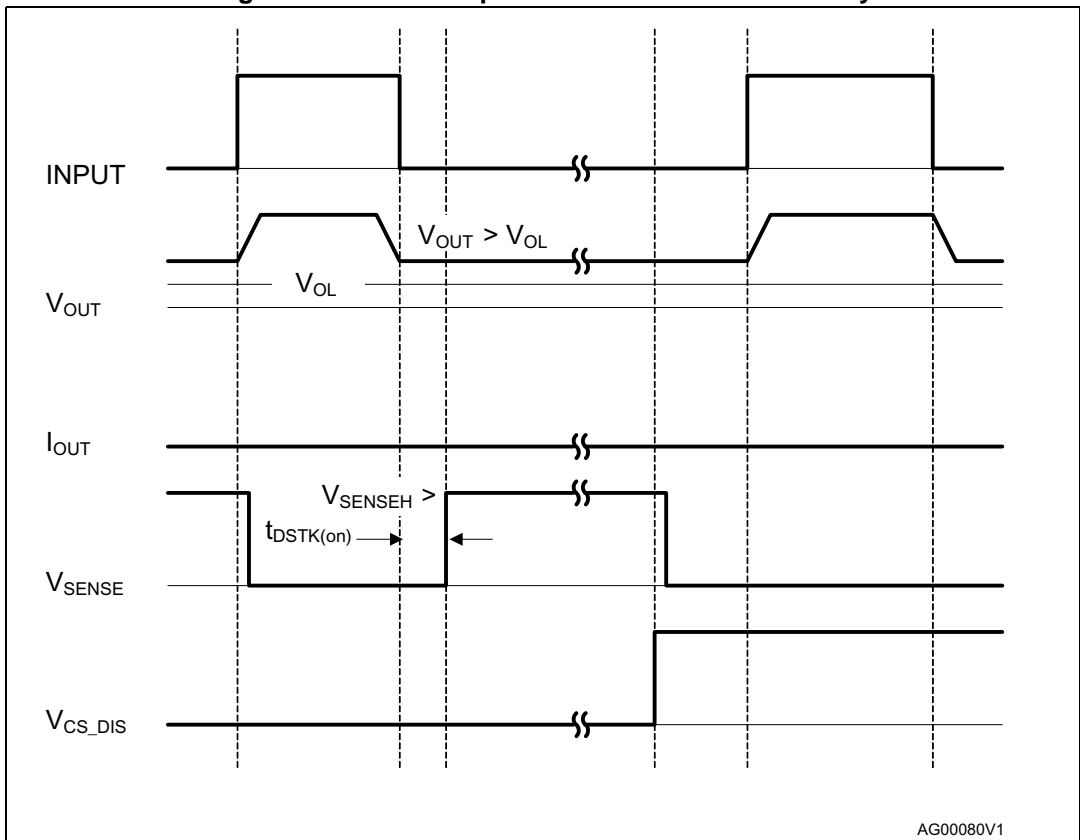


Figure 15. Short to V_{CC}

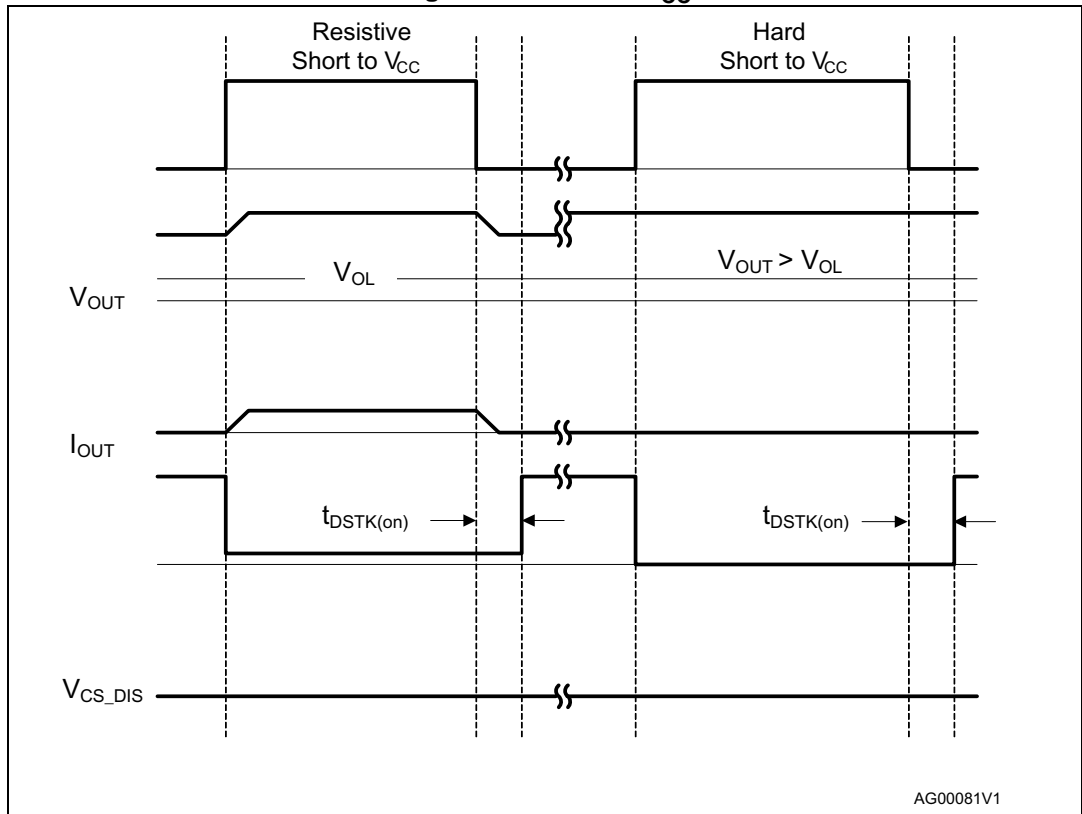
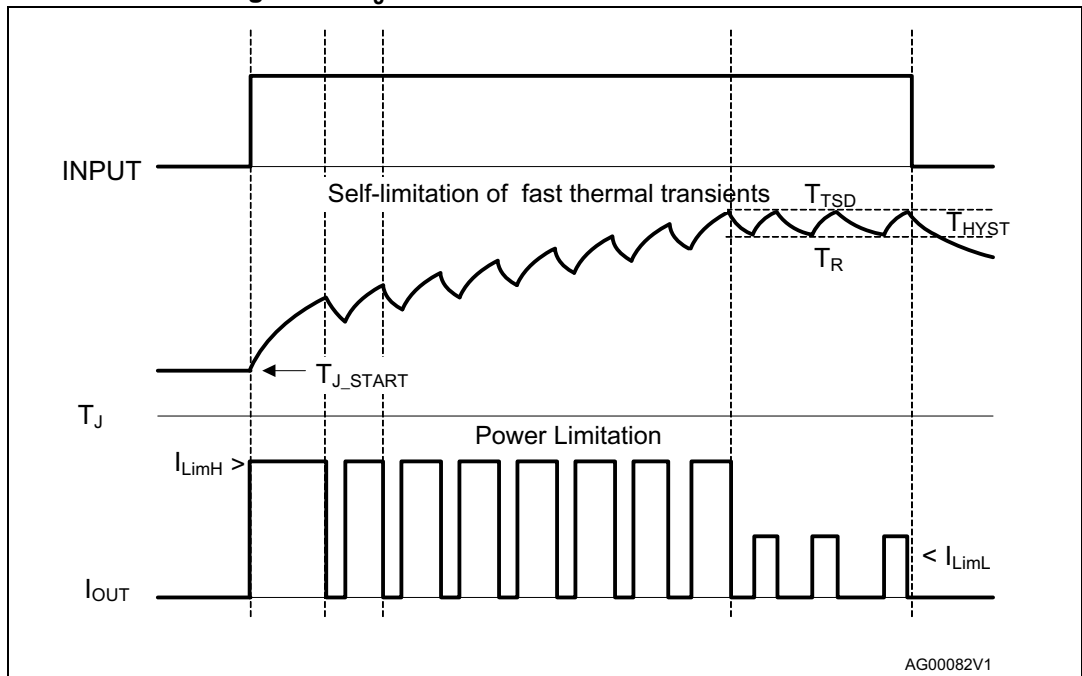
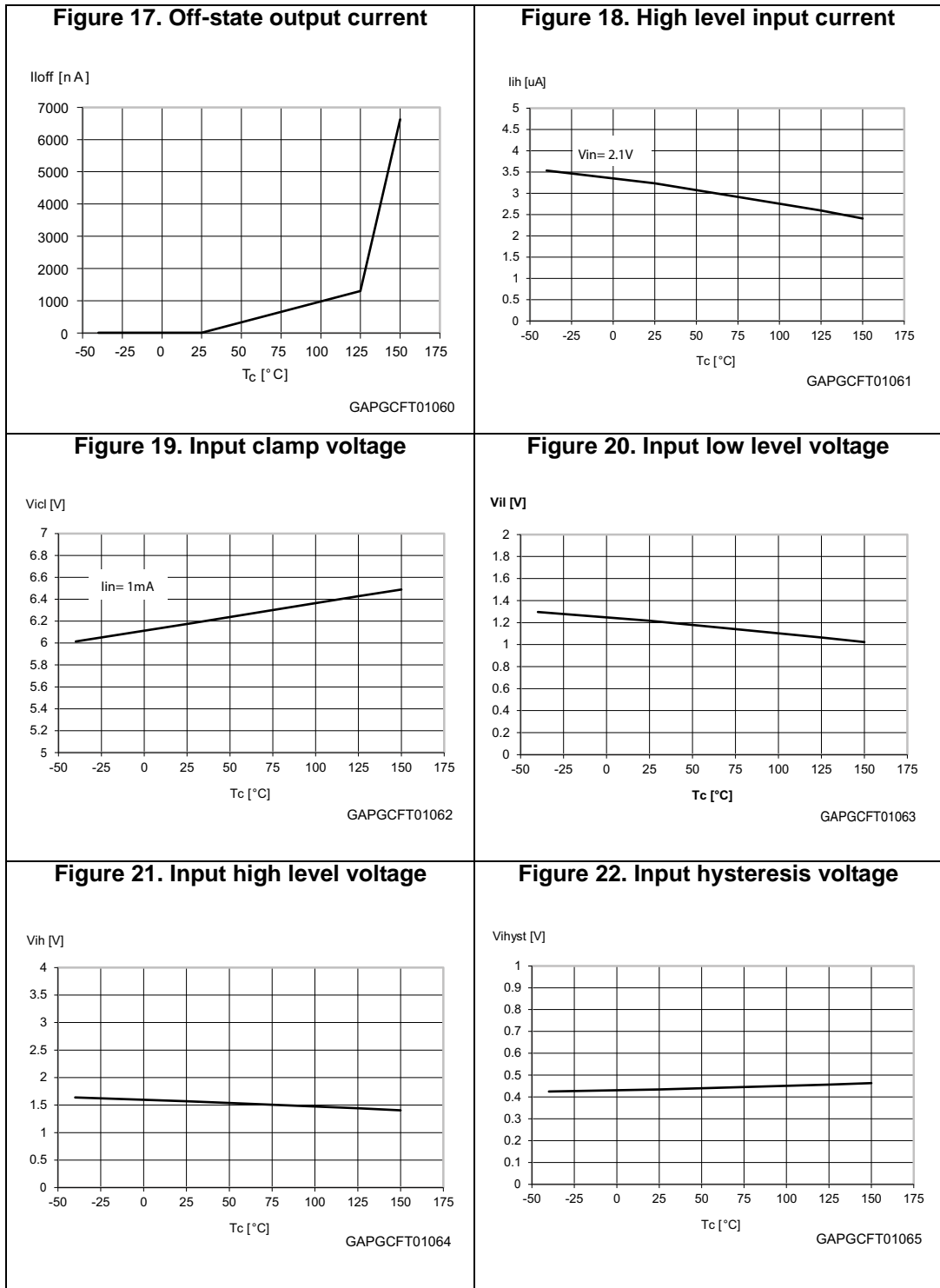


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves



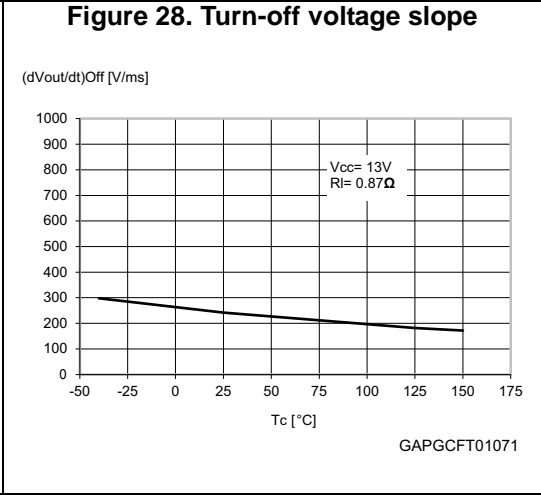
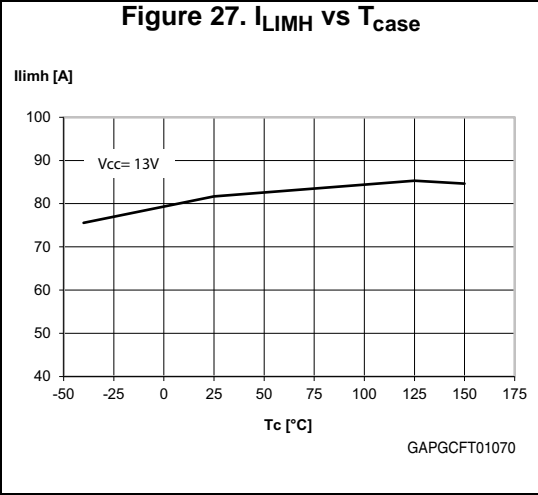
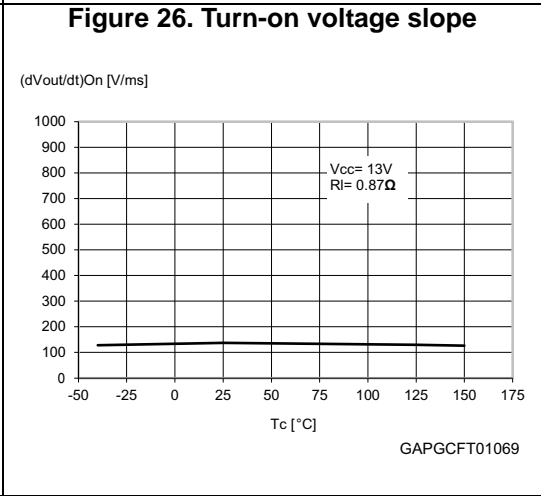
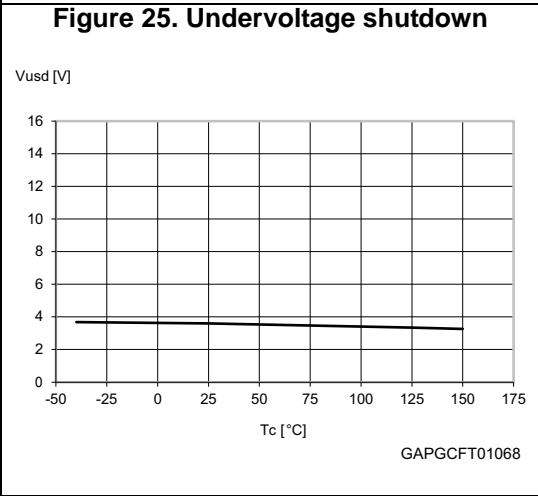
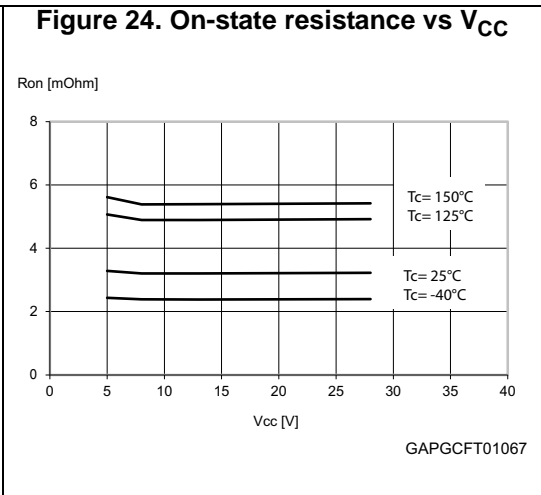
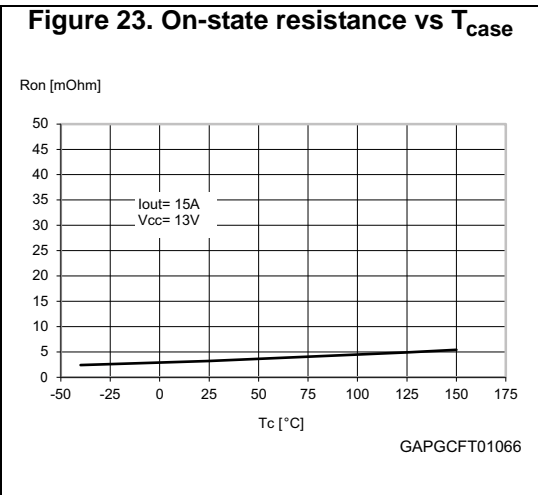


Figure 29. DE high level voltage

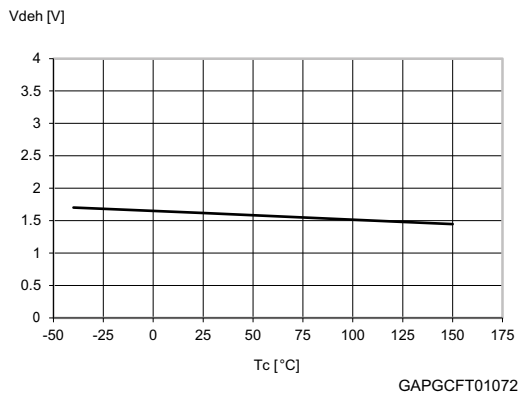


Figure 30. DE clamp voltage

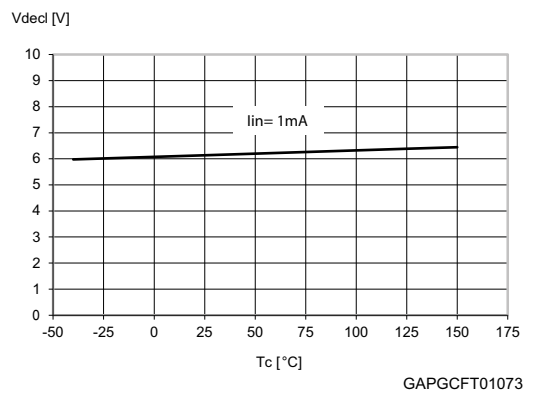
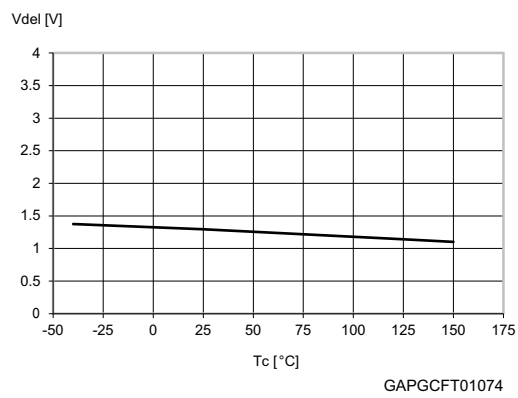
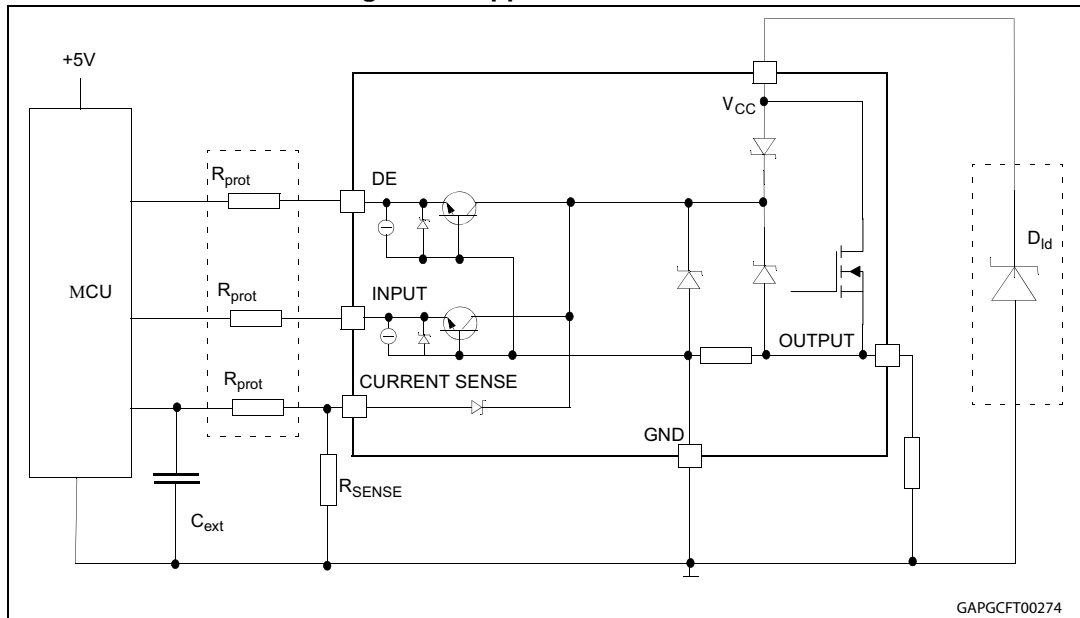


Figure 31. DE low level voltage



3 Application information

Figure 32. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the microcontroller I/O pins from latching up.

The values of these resistors provide a compromise between the leakage current of the microcontroller, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -1.5V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$75\Omega \leq R_{prot} \leq 240k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} maximum rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

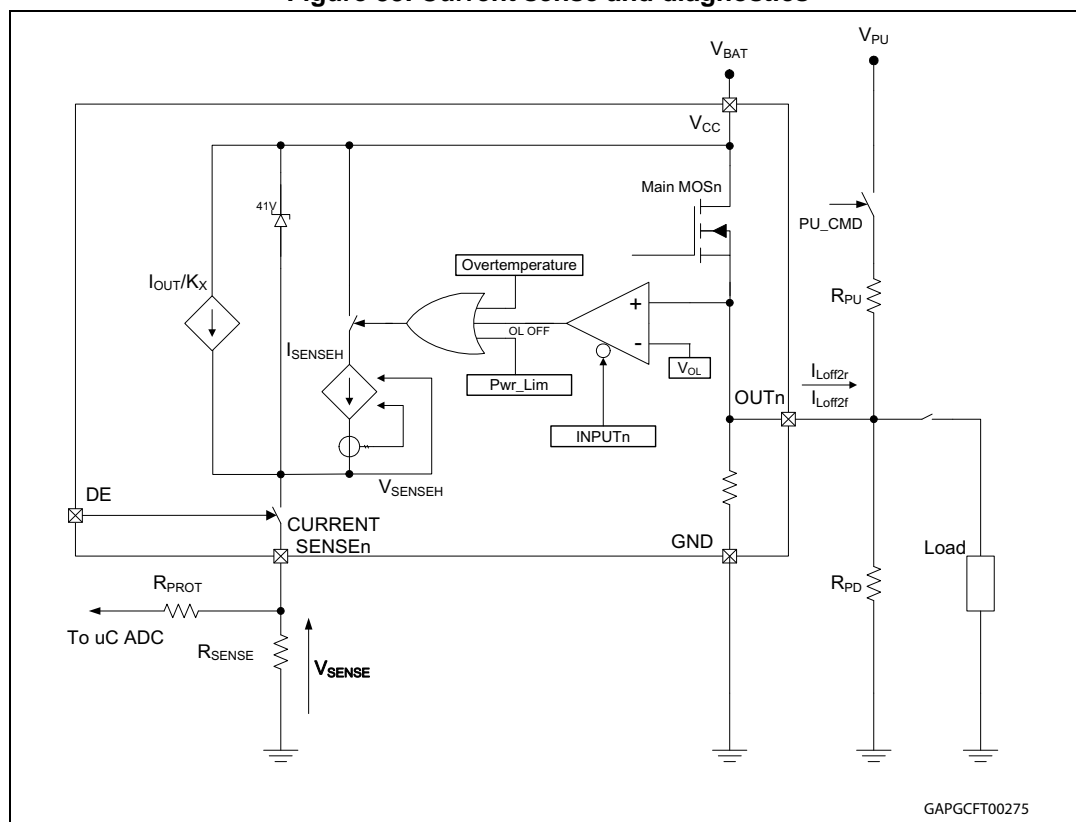
3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostics*):

- **Current mirror of the load current in normal operation**, delivering a current proportional to the load current according to a known ratio K_x .
The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE} . Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < VCC < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < VCC < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
 - Power limitation activation
 - Overtemperature
 - Short to V_{CC} in off-state
 - Open-load in off-state with additional external components.

A logic level low on the DE pin simultaneously sets all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing the sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostics



3.3.1 Short to V_{CC} and off-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Little or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

Off-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor (R_{PU}) connecting the output to a positive supply voltage (V_{PU}).

It is preferable that V_{PU} be switched off during the module standby mode to avoid an increase in the overall standby current consumption in normal conditions, that is, when the load is connected.

An external pull down resistor (R_{PD}) connected between output and GND is mandatory to avoid misdetection in case of floating outputs in off-state (see [Figure 33: Current sense and diagnostics](#)).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled up by the external circuitry:

$$V_{OUT}|_{Pull-up_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2V$$

$R_{PD} \leq 22 \text{ K}\Omega$ is recommended.

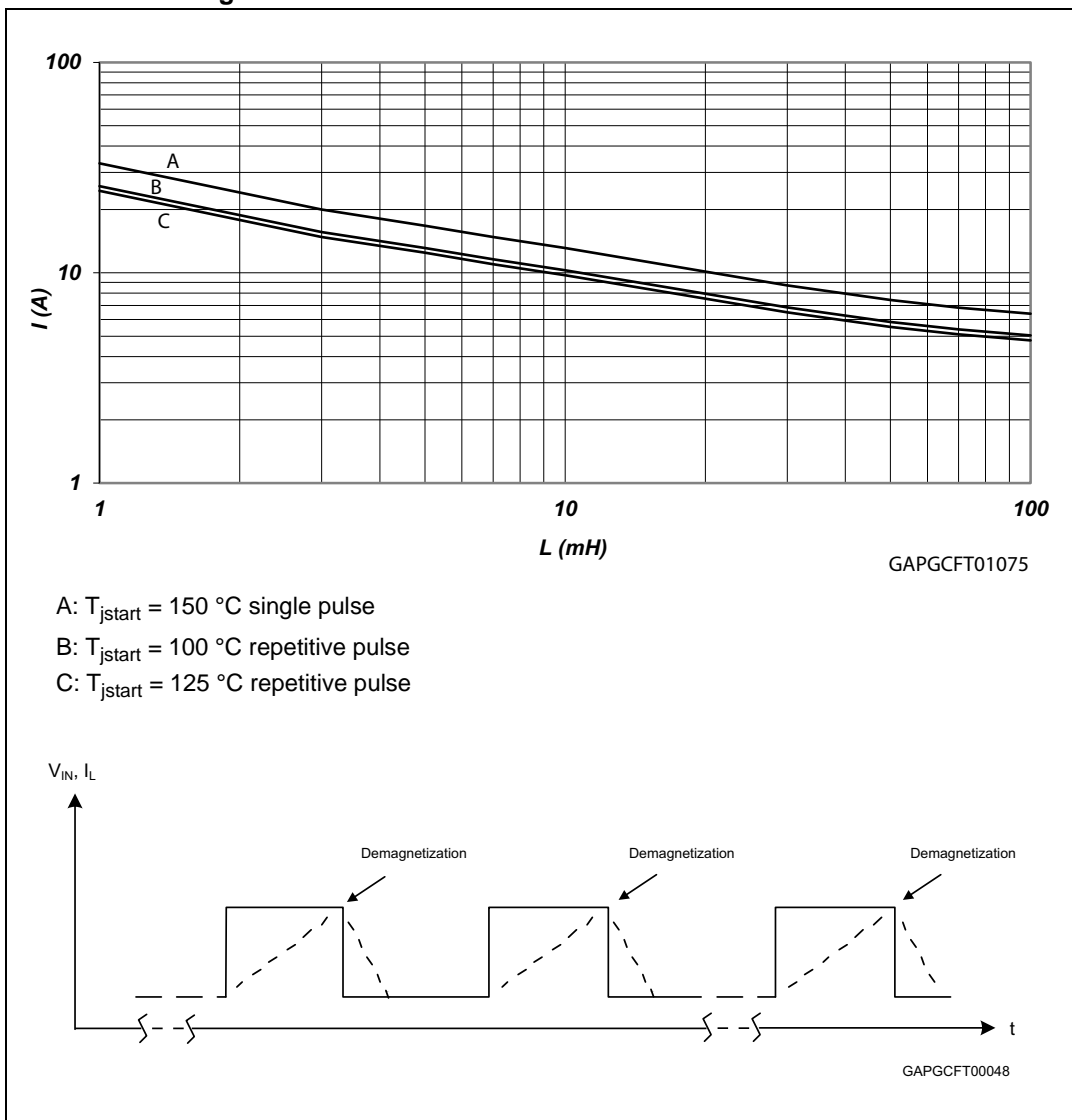
For proper open-load detection in off-state, the external pull-up resistor must be selected according to the following formula:

$$V_{OUT}|_{Pull-up_ON} = \frac{R_{PD} \cdot V_{PU} - R_{PU} \cdot R_{PD} \cdot I_{L(off2)r}}{R_{PU} + R_{PD}} = V_{OLmax} = 4V$$

For the values of V_{OLmin} , V_{OLmax} , $I_{L(off2)r}$ and $I_{L(off2)f}$ see [Table 10: Open-load detection](#) ($8 \text{ V} < V_{CC} < 18 \text{ V}$; $V_{DE} = 5 \text{ V}$).

3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 34. Maximum turn-off current versus inductance



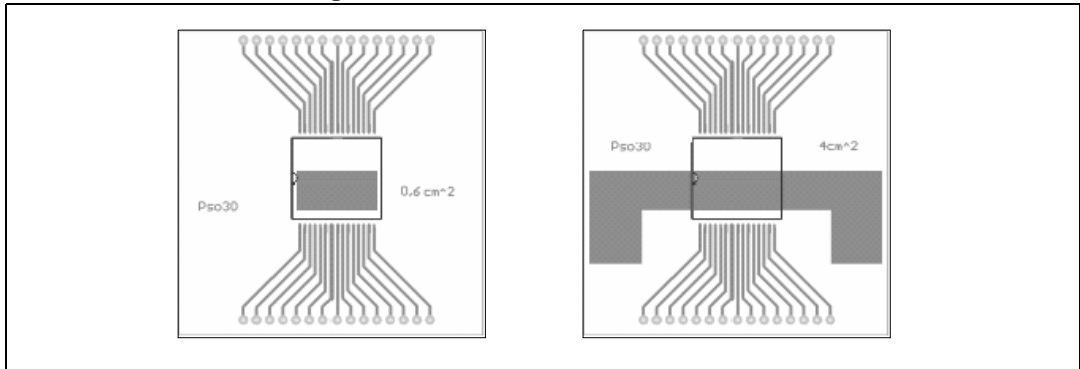
- A: $T_{jstart} = 150\text{ }^{\circ}\text{C}$ single pulse
- B: $T_{jstart} = 100\text{ }^{\circ}\text{C}$ repetitive pulse
- C: $T_{jstart} = 125\text{ }^{\circ}\text{C}$ repetitive pulse

1. Values are generated with $R_{\theta} = 0\text{ }\Omega$.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 MultiPowerSO-30 thermal data

Figure 35. MultiPowerSO-30 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 70 μ m (front and back side), copper areas: from minimum pad lay-out to 16 cm²).

Figure 36. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

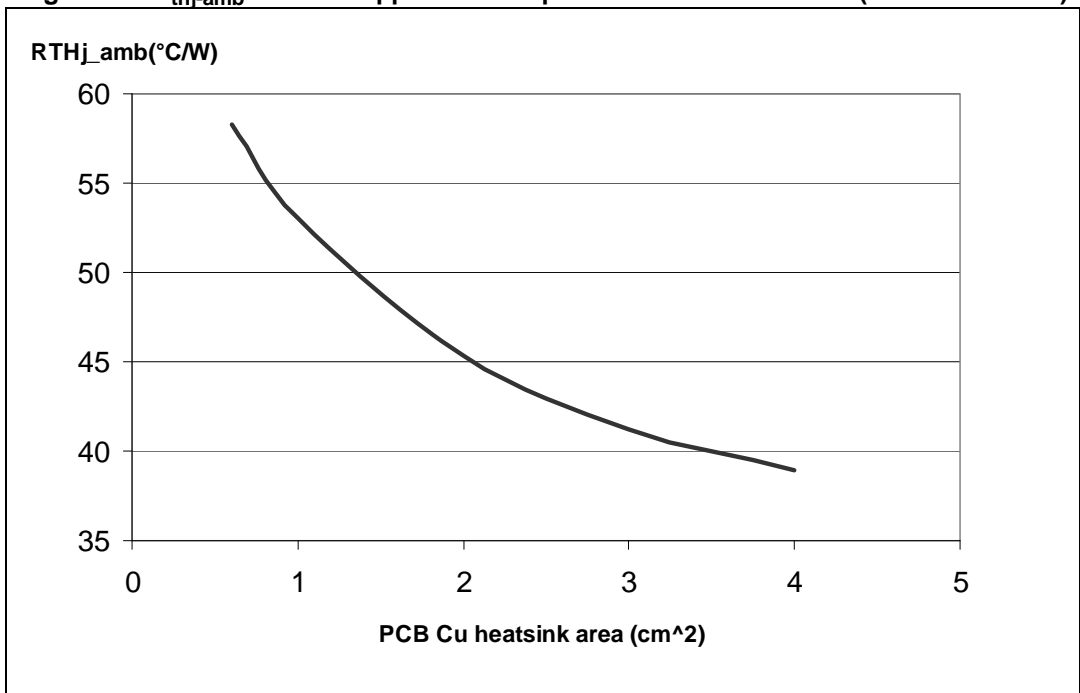


Figure 37. MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)

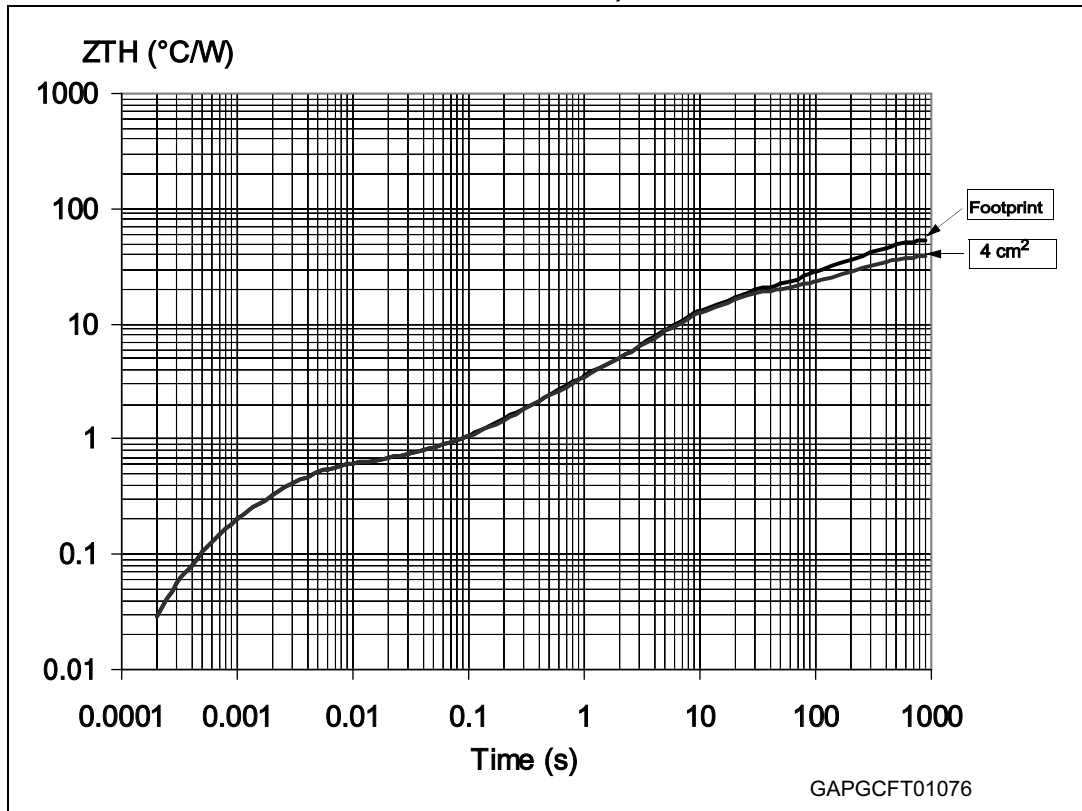
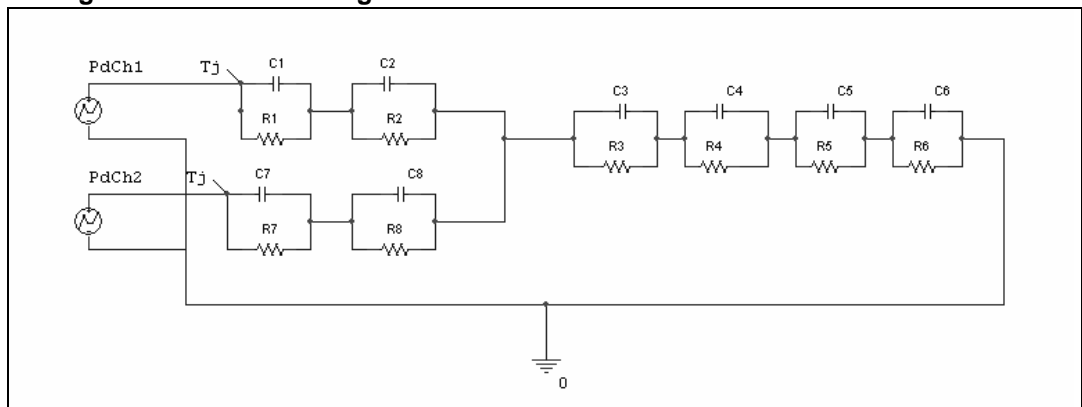


Figure 38. Thermal fitting model of a double channel HSD in MultiPowerSO-30



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protection functions (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameters for MultiPowerSO-30

Area/island (cm ²)	Footprint	4
R1 (°C/W)	0.05	
R2 (°C/W)	0.3	
R3 (°C/W)	0.5	
R4 (°C/W)	1.3	
R5 (°C/W)	14	
R6 (°C/W)	44.7	23.7
R7 (°C/W)	0.05	
R8 (°C/W)	0.3	
C1 (W.s/°C)	0.005	
C2 (W.s/°C)	0.008	
C3 (W.s/°C)	0.01	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.6	
C6 (W.s/°C)	5	11
C7 (W.s/°C)	0.005	
C8 (W.s/°C)	0.008	

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 MultiPowerSO-30 mechanical data

Figure 39. MultiPowerSO-30 outline

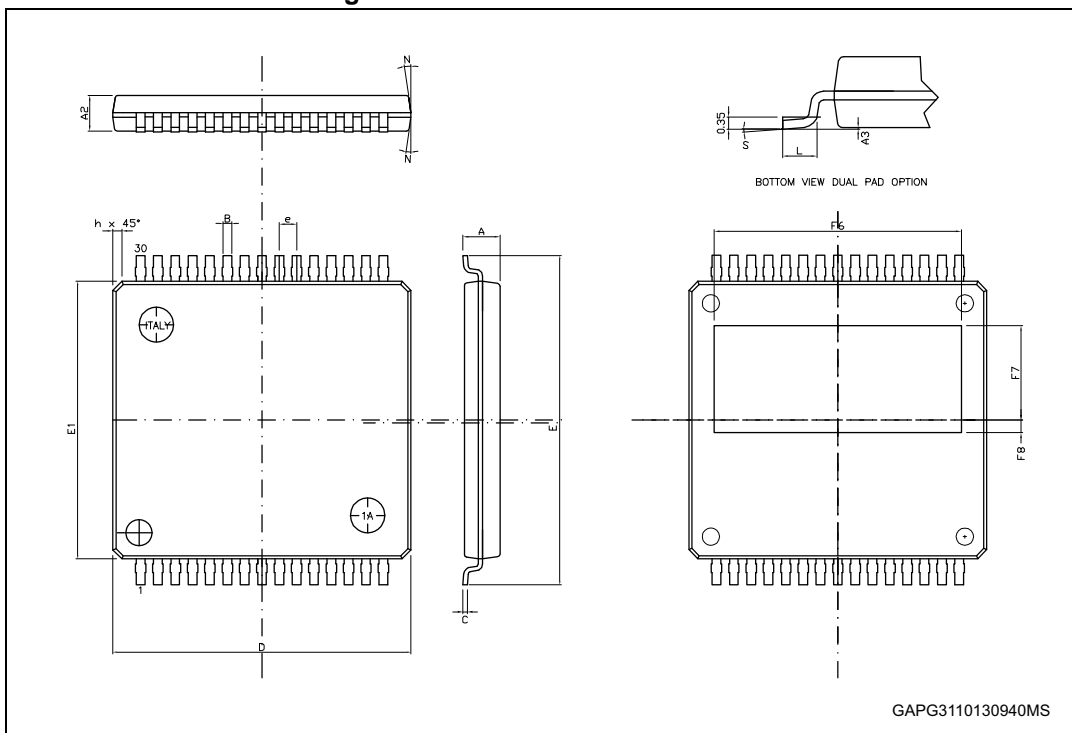


Table 16. MultiPowerSO-30 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1

Table 16. MultiPowerSO-30 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
"e"	1		
F6		14.3	
F7		5.45	
F8		0.73	
L	0.8		1.15
N			10 Deg
S	0 Deg		7 Deg

5.2 MultiPowerSO-30 packing information

The devices can be packed in tube or tape and reel shipments (see [Table 17: Device summary](#)).

Figure 40. MultiPowerSO-30 tube shipment (no suffix)

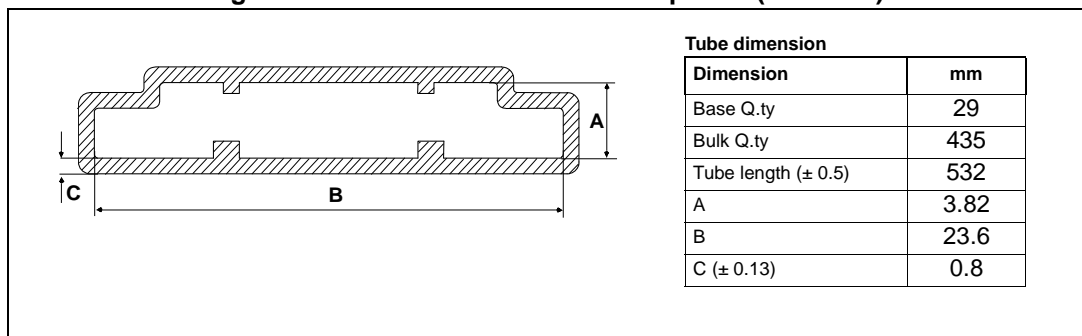
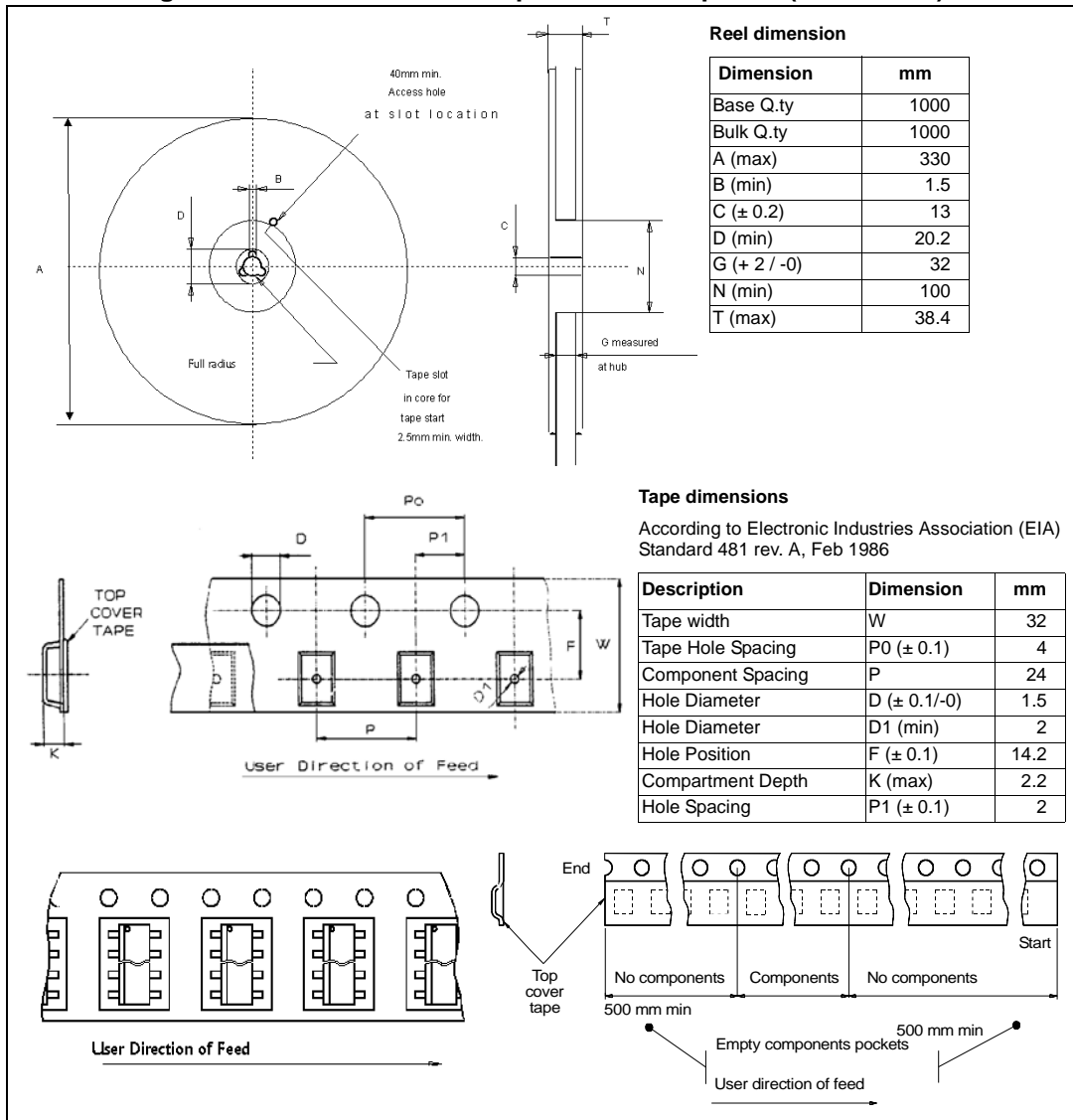


Figure 41. MultiPowerSO-30 tape and reel shipment (suffix "TR")



6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
MultiPowerSO-30	VND5E004C30-E	VND5E004C30TR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
09-Jun-2015	1	Initial release.
02-Nov-2015	2	Updated Table 17: Device summary

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