

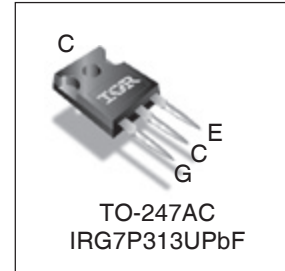
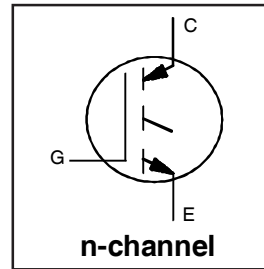
**PDP TRENCH IGBT**

# IRG7P313UPbF

**Features**

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low  $V_{CE(on)}$  and Energy per Pulse ( $E_{PULSE}^{TM}$ ) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters		
$V_{CE\ min}$	330	V
$V_{CE(ON)}\ typ.\ @\ I_C = 20A$	1.35	V
$I_{RP}\ max\ @\ T_C = 25^\circ C$	200	A
$T_J\ max$	150	°C



G	C	E
Gate	Collector	Emitter

**Description**

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low  $V_{CE(on)}$  and low  $E_{PULSE}^{TM}$  rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GE}$	Gate-to-Emitter Voltage	±30	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE} @ 15V$	40	A
$I_C @ T_C = 100^\circ C$	Continuous Collector, $V_{GE} @ 15V$	20	
$I_{RP} @ T_C = 25^\circ C$	Repetitive Peak Current ①	200	
$P_D @ T_C = 25^\circ C$	Power Dissipation	89	W
$P_D @ T_C = 100^\circ C$	Power Dissipation	36	
	Linear Derating Factor	0.71	W/°C
$T_J$	Operating Junction and Storage Temperature Range	-40 to + 150	°C
$T_{STG}$			
	Soldering Temperature for 10 seconds	300	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.4	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{CES}$	Collector-to-Emitter Breakdown Voltage	330	—	—	V	$V_{GE} = 0V, I_{CE} = 250\mu A$
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.4	—	V/°C	Reference to $25^\circ\text{C}, I_{CE} = 1\text{mA}$
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.21	1.45	V	$V_{GE} = 15V, I_{CE} = 12A$ ③
		—	1.35	—		$V_{GE} = 15V, I_{CE} = 20A$ ③
		—	1.75	—		$V_{GE} = 15V, I_{CE} = 40A$ ③
		—	2.14	—		$V_{GE} = 15V, I_{CE} = 60A$ ③
		—	1.41	—		$V_{GE} = 15V, I_{CE} = 20A, T_J = 150^\circ\text{C}$ ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	$V_{CE} = V_{GE}, I_{CE} = 1.0\text{mA}$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
$I_{CES}$	Collector-to-Emitter Leakage Current	—	1.0	10	$\mu A$	$V_{CE} = 330V, V_{GE} = 0V$
		—	25	150		$V_{CE} = 330V, V_{GE} = 0V, T_J = 125^\circ\text{C}$
		—	75	—		$V_{CE} = 330V, V_{GE} = 0V, T_J = 150^\circ\text{C}$
$I_{GES}$	Gate-to-Emitter Forward Leakage	—	—	100	nA	$V_{GE} = 30V$
	Gate-to-Emitter Reverse Leakage	—	—	-100		$V_{GE} = -30V$
$g_{fe}$	Forward Transconductance	—	47	—	S	$V_{CE} = 25V, I_{CE} = 12A$
$Q_g$	Total Gate Charge	—	33	—	nC	$V_{CE} = 240V, I_C = 12A, V_{GE} = 15V$ ③
$Q_{gc}$	Gate-to-Collector Charge	—	12	—		
$t_{d(on)}$	Turn-On delay time	—	11	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 210\mu H$ $T_J = 25^\circ\text{C}$
$t_r$	Rise time	—	13	—		
$t_{d(off)}$	Turn-Off delay time	—	75	—		
$t_f$	Fall time	—	68	—		
$t_{d(on)}$	Turn-On delay time	—	11	—	ns	$I_C = 12A, V_{CC} = 196V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150\text{nH}$ $T_J = 150^\circ\text{C}$
$t_r$	Rise time	—	14	—		
$t_{d(off)}$	Turn-Off delay time	—	86	—		
$t_f$	Fall time	—	190	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{CC} = 240V, V_{GE} = 15V, R_G = 5.1\Omega$
$E_{PULSE}$	Energy per Pulse	—	480	—	$\mu J$	$L = 220\text{nH}, C = 0.20\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 25^\circ\text{C}$
		—	570	—		$L = 220\text{nH}, C = 0.20\mu F, V_{GE} = 15V$ $V_{CC} = 240V, R_G = 5.1\Omega, T_J = 100^\circ\text{C}$
ESD	Human Body Model	Class 1C (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
$C_{ies}$	Input Capacitance	—	880	—	pF	$V_{GE} = 0V$
$C_{oes}$	Output Capacitance	—	47	—		$V_{CE} = 30V$
$C_{res}$	Reverse Transfer Capacitance	—	26	—		$f = 1.0\text{MHz}$
$L_C$	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
$L_E$	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

### Notes:

- ① Half sine wave with duty cycle = 0.05,  $t_{on} = 2\mu\text{sec}$ .
- ②  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

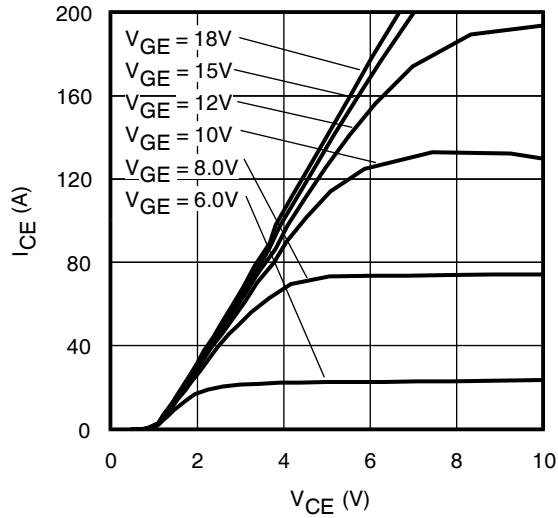


Fig 1. Typical Output Characteristics @ 25°C

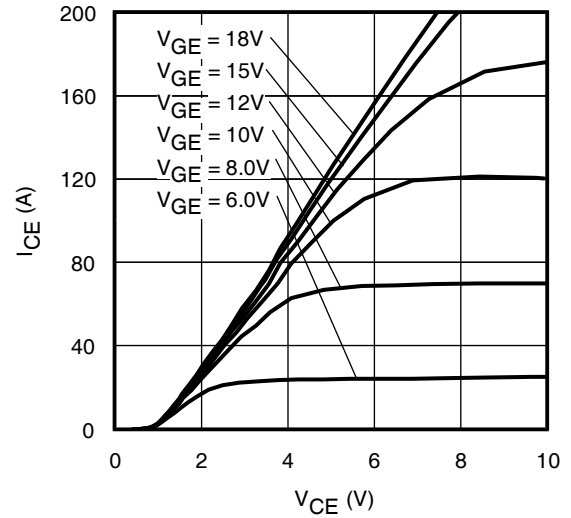


Fig 2. Typical Output Characteristics @ 75°C

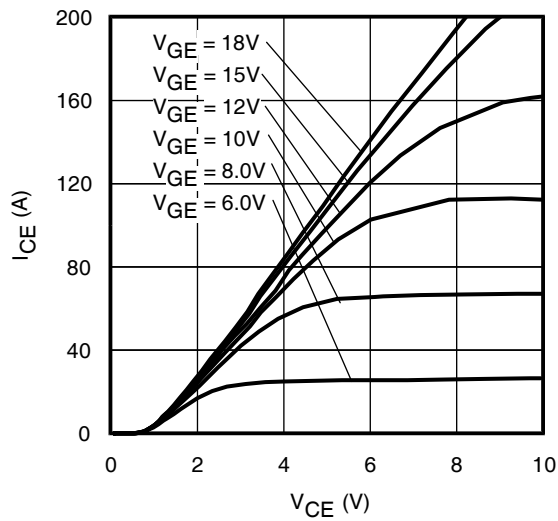


Fig 3. Typical Output Characteristics @ 125°C

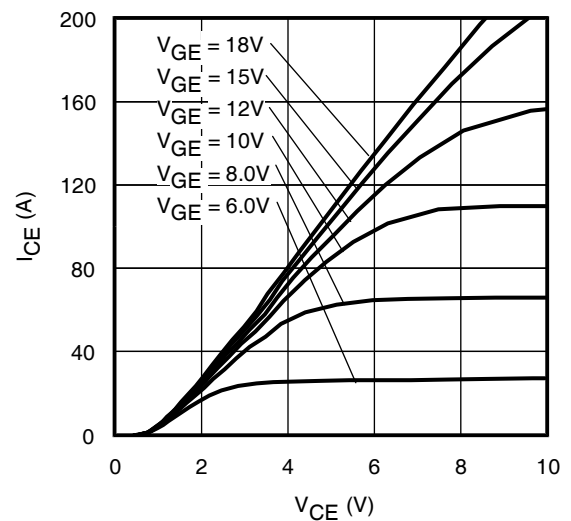


Fig 4. Typical Output Characteristics @ 150°C

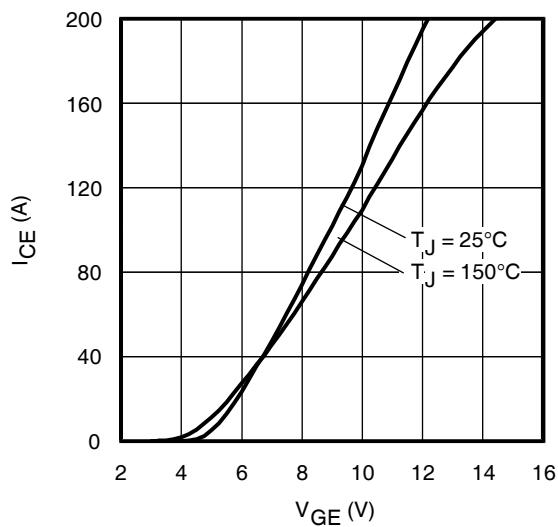


Fig 5. Typical Transfer Characteristics

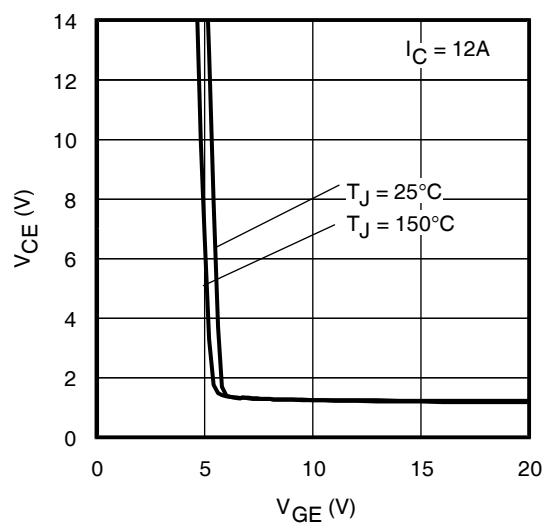


Fig 6.  $V_{CE(ON)}$  vs. Gate Voltage

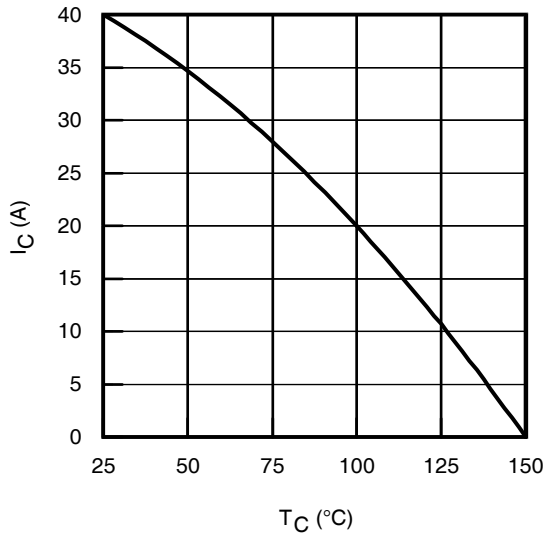


Fig 7. Maximum Collector Current vs. Case Temperature

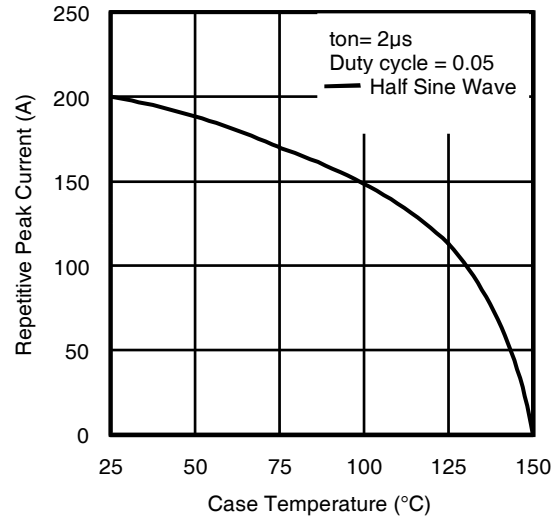


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

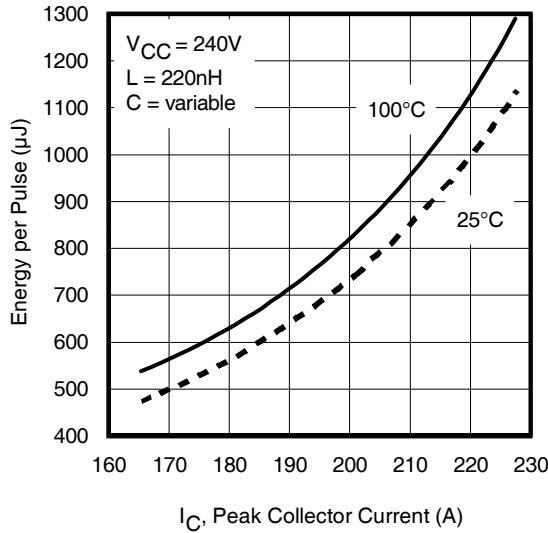


Fig 9. Typical  $E_{PULSE}$  vs. Collector Current

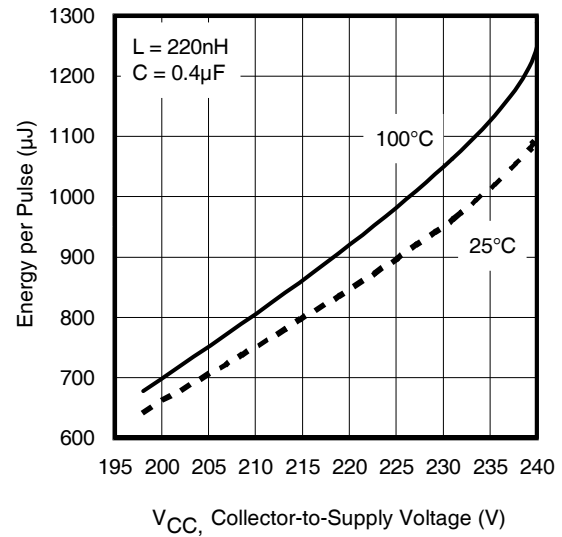


Fig 10. Typical  $E_{PULSE}$  vs. Collector-to-Supply Voltage

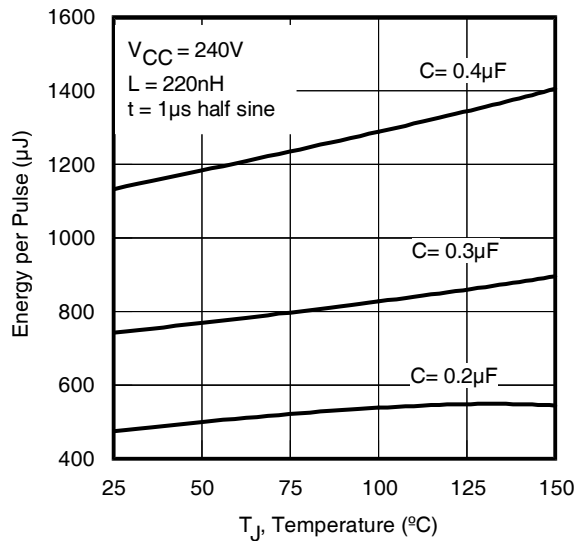


Fig 11.  $E_{PULSE}$  vs. Temperature

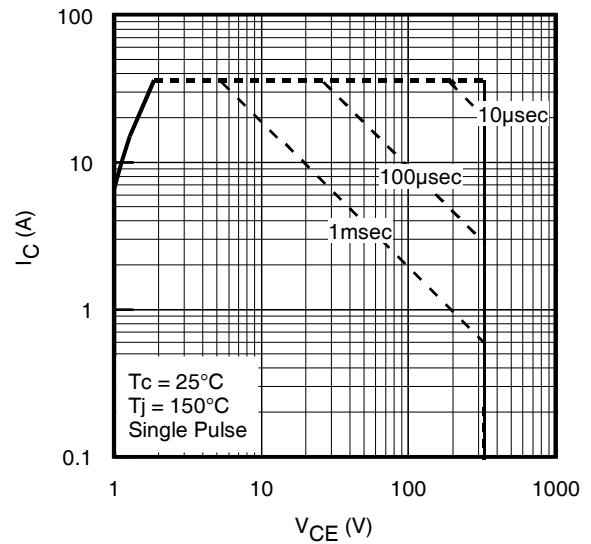


Fig 12. Forward Bias Safe Operating Area

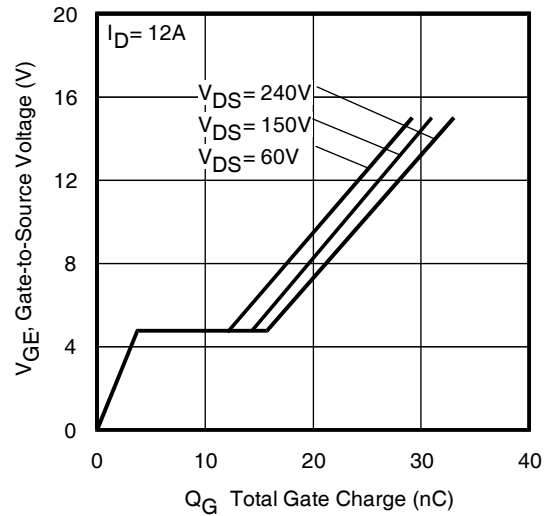
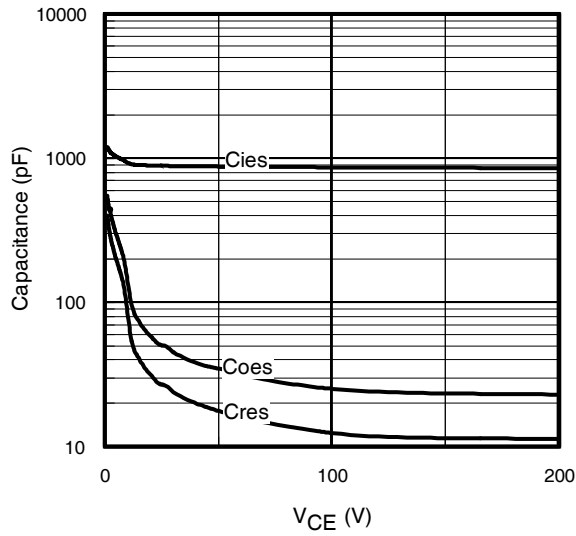


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

Fig 14. Typical Gate Charge vs. Gate-to-Source Voltage

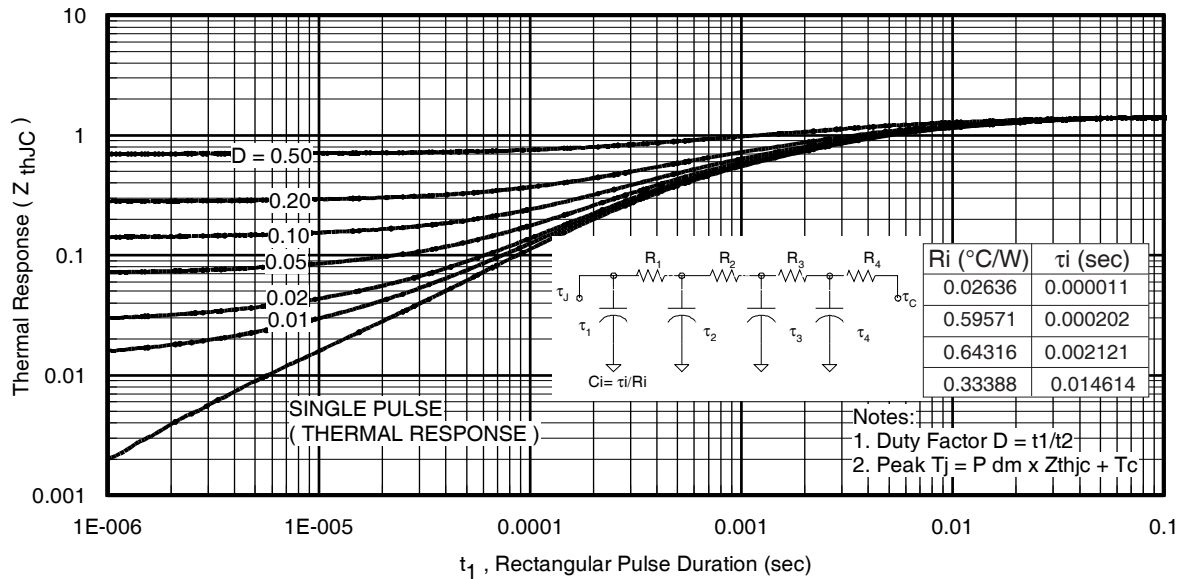
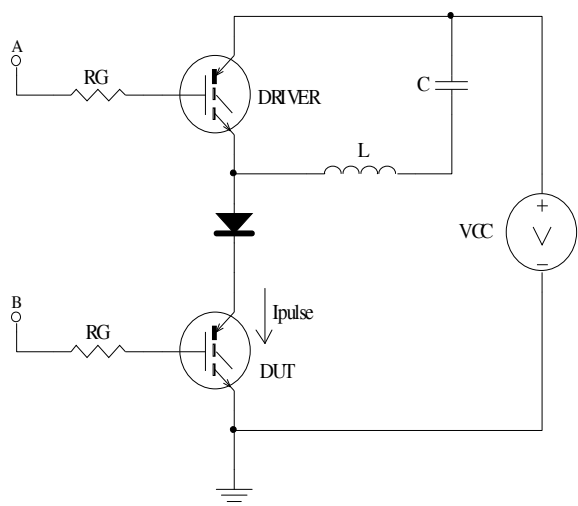
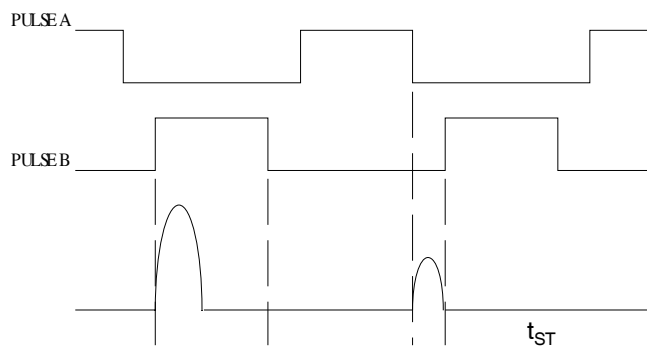


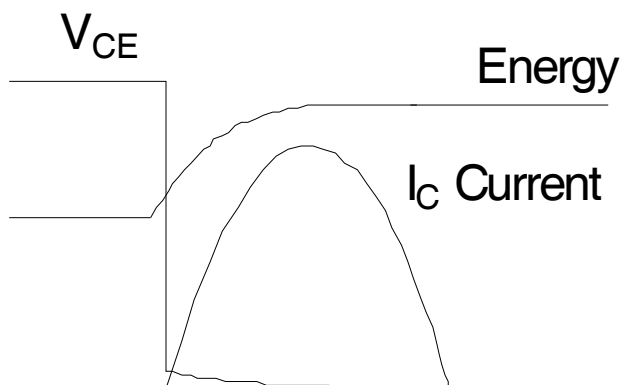
Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case



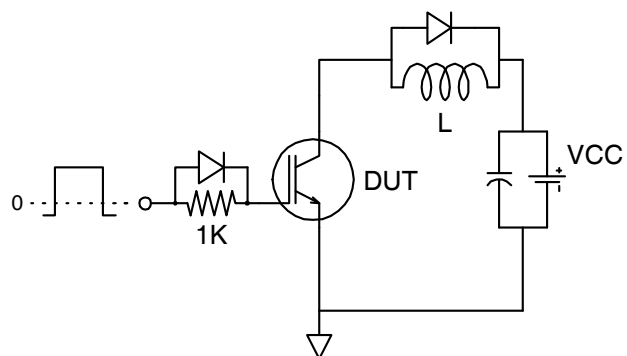
**Fig 16a.**  $t_{st}$  and  $E_{PULSE}$  Test Circuit



**Fig 16b.**  $t_{st}$  Test Waveforms



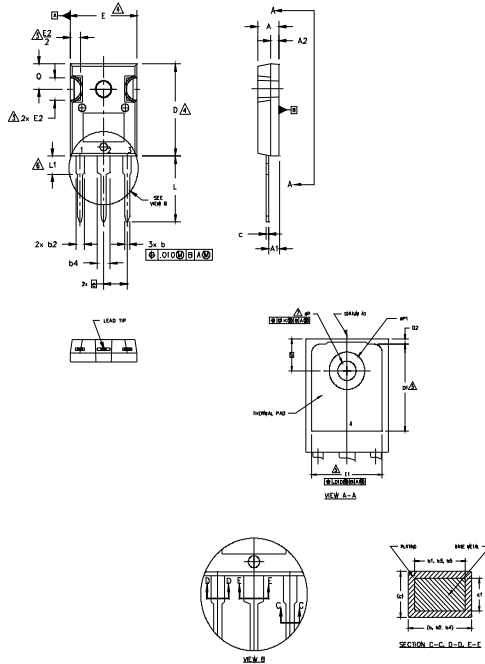
**Fig 16c.**  $E_{PULSE}$  Test Waveforms



**Fig. 17 -** Gate Charge Circuit (turn-off)

## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
  2. DIMENSIONS ARE SHOWN IN INCHES.
  3. CONTOUR OF SLOT OPTIONAL.
  4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  6. LEAD FINISH UNCONTROLLED IN L1.
  7. #P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.035	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
ek	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
#P	.140	.144	3.56	3.66	
#P1	-	.291	-	7.39	
O	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFEEET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, COPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

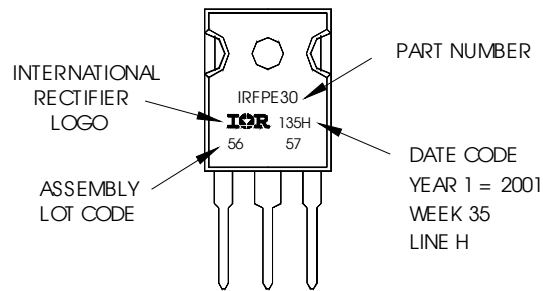
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed for the Industrial market.  
Qualification Standards can be found on IR's Web site.