



L8401

Preliminary

LINEAR INTEGRATED CIRCUIT

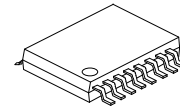
FET BIAS CONTROLLER

DESCRIPTION

The UTC **L8401** is designed to bias the MOSFETs that are commonly used in LNBS that can implies minimum external components requires.

FEATURES

- * Can Bias up to 4 FETs
- * Drain Current Adjustable by Two External Resistors.
- * Two Sets of Drain Current can be Setted.



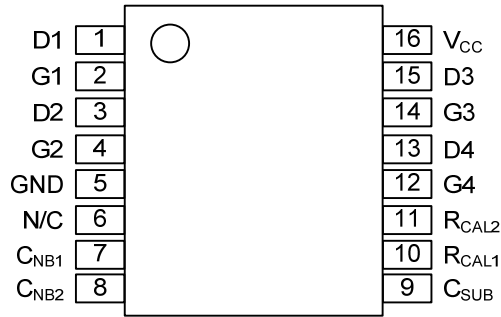
SSOP-16(150mil)

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8401L-R16-T	L8401G-R16-T	SSOP-16	Tube
L8401L-R16-R	L8401G-R16-R	SSOP-16	Tape Reel

<p>L8401L-R16-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel (2) R16: SSOP-16 (3) L: Lead Free, G: Halogen Free</p>
---------------------------------------------------------------------------------	---------------------------------------------------------------------------------------------

■ PIN CONFIGURATION



■ FUNCTIONAL DIAGRAM

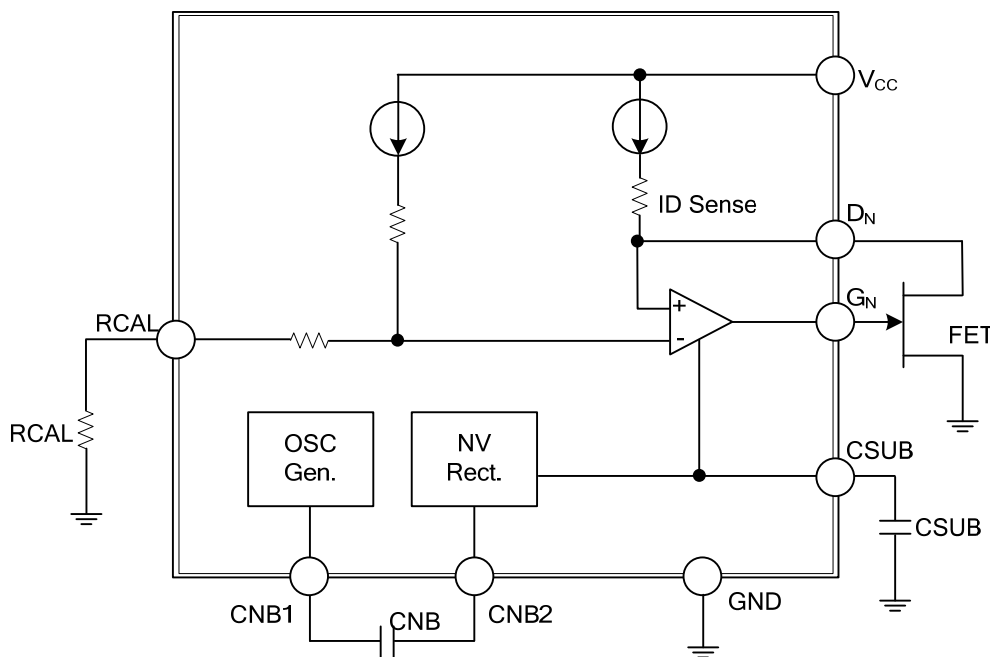


Fig.1

■ FUNCTIONAL DESCRIPTION

The UTC **L8401** includes one negative supply required for gate biasing from the single supply voltage, and all the other bias requirements for external FETs.

A low current negative supply voltage includes an internal OSC and two 47nF external cap. The negative rail generator is common to all devices. This negative supply voltage used to drive the FET's gate to obtain the required drain current because of the FET is a depletion mode transistor.

There are four stages in the IC to biasing the four external FETs. The drain voltage of the external FET FET1~4 is 2.2 volts set by the UTC **L8401**.

The drain current of external FET is determined by the external resistor R_{CAL1} or R_{CAL2} . External resistor R_{CAL1} sets the drain current of FET1 and FET 2, and resistor R_{CAL2} sets the drain current of FET3 and FET4.

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.6~8	V
Supply Current	I_{CC}	100	mA
Maximum Drain Current		15	mA
Maximum CSUB Sink Current		-500	uA
Operating Temperature	T_{OPR}	-40~80	°C
Storage Temperature	T_{STG}	-50~150	°C

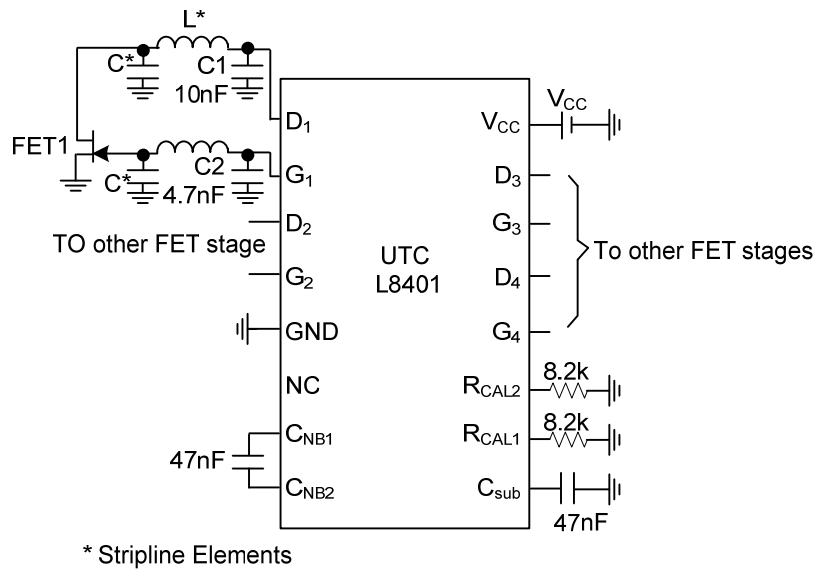
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=3.3V$, $I_D=10mA$, $R_{CAL1}=8.2K\Omega$, $R_{CAL2}=8.2K\Omega$, $T_A=25^\circ C$, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		3.3		6	V
Supply Current	I_{CC}	No FET			10	mA
Negative Voltage	V_{SUB}	$I_{SUB}=0uA$, $V_{CC}=6V$	-3.0	-2.5	-1	V
		$I_{SUB}=-200uA$			-1	V
Oscillator Freq.	f_O		200	350	800	KHz
Drain Current	I_D		8	10	12	mA
Drain Current Change with V_{CC}	ΔI_{DV}	$V_{CC}=3.3\sim 6V$		0.2		%/V
VD1/VD2(VD3/VD4) Drain Offset Current	ΔI_{DC}			0.2		mA
Drain Current Change with Temp.	ΔI_{DT}	$T=-40\sim 80^\circ C$		0.1		%/°C
Drain Voltage	V_D	$I_D=10mA$	1.8	2	2.2	V
Drain Voltage Change with V_{CC}	ΔV_{DV}	$V_{CC}=3.3\sim 6V$		0.5		%/V
Drain Voltage Change	ΔV_{DT}	$T=-40\sim 80^\circ C$		50		ppm
Dynamic Gate Voltage Range	V_G	Csub without loading	-2.5		0.7	V
Drain Output Noise Voltage	V_{dn}	With drain bypass capacitor=10nF			0.05	V_{PP}
Gate Output Noise Voltage	V_{GN}	With gate bypass capacitor=10nF			0.03	V_{PP}

■ TYPICAL APPLICATION CIRCUIT



* Stripline Elements

Fig.2

■ APPLICATIONS INFORMATION

It is application circuit of UTC **L8401** in figure 2, the bias circuits is stable fully in -40°C ~80°C.

CNB and C_{SUB} are used to generated the negative supply on pin C_{SUB} (about -2.5V), which can be used to power other external circuits, but it is low load current is noticeable.

C1 and C2 are used to suppress noise or RF interference in each stage of the IC or other external circuits in application circiut system. Value of C1 and C2 could be used in 1nF to 100nF as design dependent.

R_{CAL1} and R_{CAL2} are used to set the drain current of FETs 1 & 2 and FETS 3 & 4. If the same drain current is required for all FETs on UTC **L8401**, then the pin R_{CAL1} and R_{CAL2} can be connected to GND through only one res of half normal value.

There are full protection for external FETs on chip: The gate output voltage is limited in -2.5V~0.7V in any conditions including powerup and powerdown transients; If the negative bias generator be shorted or overloaded, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

The fig.3 is typical applications of UTC **L8401** in LNB.

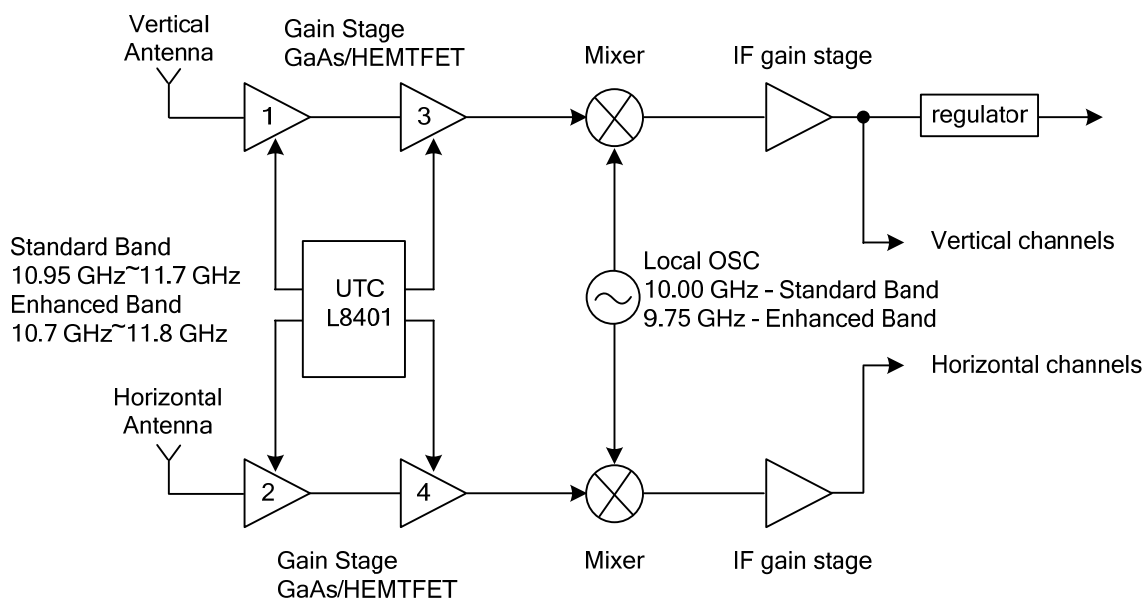


Fig.3

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.