

SOJ, TSOP, FP-BGA
Commercial Temp
Industrial Temp

256K x 16

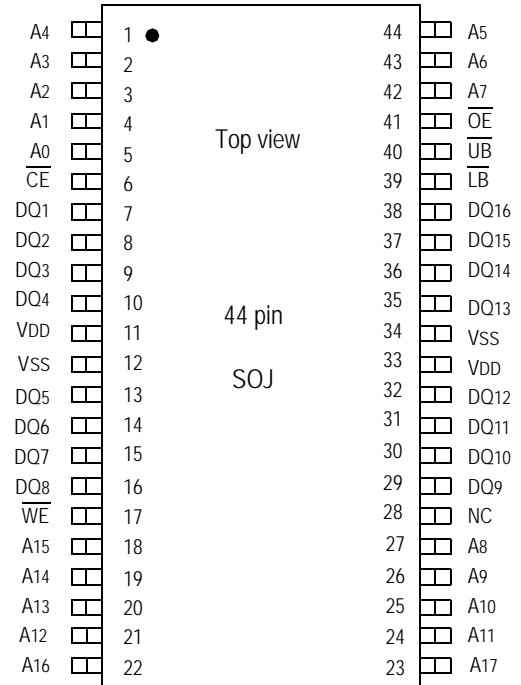
4Mb Asynchronous SRAM

8, 10, 12, 15ns
3.3V V_{DD}
Center V_{DD} & V_{SS}

Features

- Fast access time: 8, 10, 12, 15ns
- CMOS low power operation: 170/145/130/110 mA at min.cycle time.
- Single 3.3V ± 0.3V power supply
- All inputs and outputs are TTL compatible
- Byte control
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- Package line up
 - J: 400mil, 44 pin SOJ package
 - TP: 400mil, 44 pin TSOP Type II package
 - U: 7.20mm x 11.65mm Fine Pitch Ball Grid Array package

SOJ 256K x 16 Pin Configuration



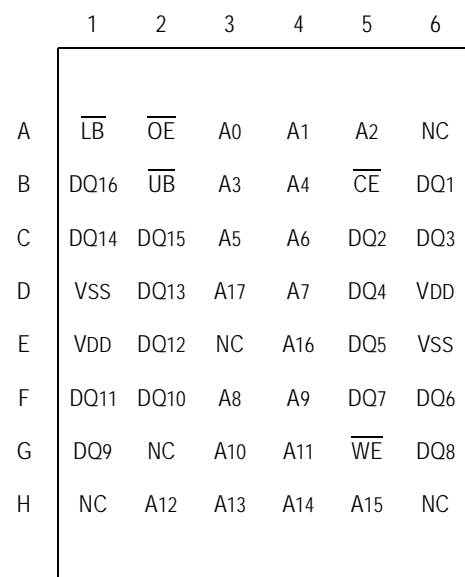
Description

The GS74116 is a high speed CMOS static RAM organized as 262,144-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS74116 is available in a 7.2x11.65 mm Fine Pitch BGA package, 400 mil SOJ and 400 mil TSOP Type-II packages.

Pin Descriptions

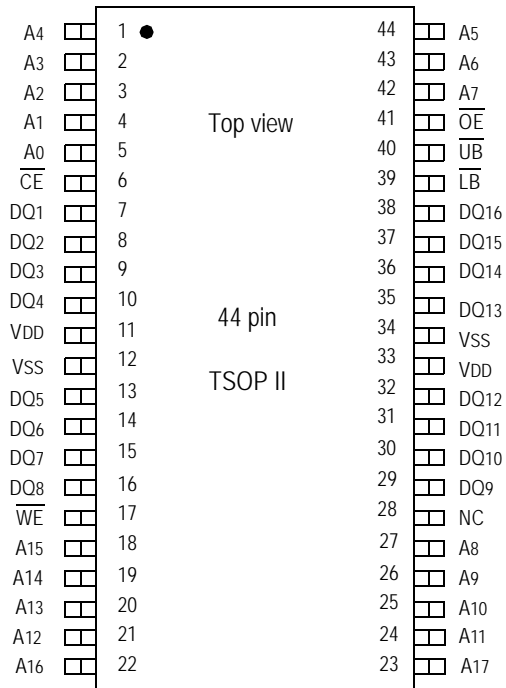
| Symbol | Description |
|-------------------------------------|--|
| A ₀ to A ₁₇ | Address input |
| DQ ₁ to DQ ₁₆ | Data input/output |
| \overline{CE} | Chip enable input |
| \overline{LB} | Lower byte enable input (DQ ₁ to DQ ₈) |
| \overline{UB} | Upper byte enable input (DQ ₉ to DQ ₁₆) |
| \overline{WE} | Write enable input |
| \overline{OE} | Output enable input |
| V _{DD} | +3.3V power supply |
| V _{SS} | Ground |
| NC | No connect |

Fine Pitch BGA 256K x 16 Bump Configuration

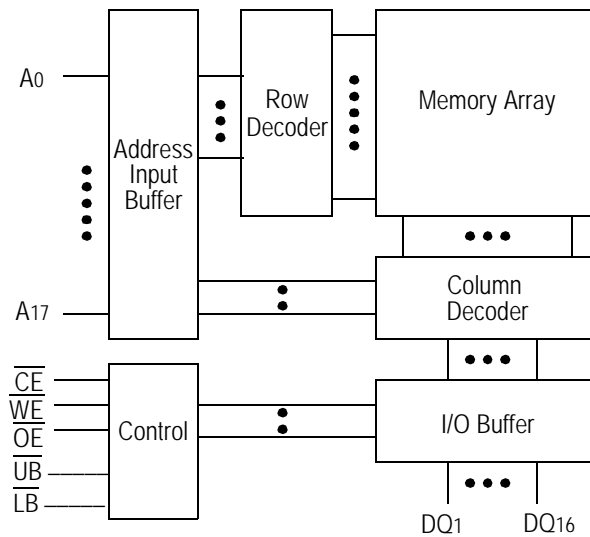


7.2x11.65mm 0.75mm Bump Pitch
Top View

TSOP-II 256K x 16 Pin Configuration



Block Diagram



Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{UB} | DQ1 to DQ8 | DQ9 to DQ16 | VDD Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-------------------|-----------------|
| H | X | X | X | X | Not Selected | Not Selected | ISB1, ISB2 |
| L | L | H | L | L | Read | Read | I _{DD} |
| | | | L | H | Read | High Z | |
| | | | H | L | High Z | Read | |
| L | X | L | L | L | Write | Write | |
| | | | L | H | Write | Not Write, High Z | |
| | | | H | L | Not Write, High Z | Write | |
| L | H | H | X | X | High Z | High Z | |
| L | X | X | H | H | High Z | High Z | |

Note: X: "H" or "L"

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-----------------------------|------------------|---|------|
| Supply Voltage | V _{DD} | -0.5 to +4.6 | V |
| Input Voltage | V _{IN} | -0.5 to V _{DD} +0.5 (≤ 4.6V max.) | V |
| Output Voltage | V _{OUT} | -0.5 to V _{DD} +0.5 (≤ 4.6V max.) | V |
| Allowable power dissipation | PD | 0.7 | W |
| Storage temperature | T _{STG} | -55 to 150 | °C |

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------------|-----------------|-------|-----|----------------------|------|
| Supply Voltage for -10/12/15 | V _{DD} | 3.0 | 3.3 | 3.6 | V |
| Supply Voltage for -8 | V _{DD} | 3.135 | 3.3 | 3.6 | V |
| Input High Voltage | V _{IH} | 2.0 | - | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | -0.3 | - | 0.8 | V |
| Ambient Temperature, Commercial Range | T _{Ac} | 0 | - | 70 | °C |
| Ambient Temperature, Industrial Range | T _{AI} | -40 | - | 85 | °C |

Note:

1. Input overshoot voltage should be less than V_{DD}+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

| Parameter | Symbol | Test Condition | Max | Unit |
|--------------------|------------------|----------------------|-----|------|
| Input Capacitance | C _{IN} | V _{IN} =0V | 5 | pF |
| Output Capacitance | C _{OUT} | V _{OUT} =0V | 7 | pF |

Notes:

1. Tested at T_A=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|------------------------|-----------------|--|------|------|
| Input Leakage Current | I _{IL} | V _{IN} = 0 to V _{DD} | -1uA | 1uA |
| Output Leakage Current | I _{LO} | Output High Z V _{OUT} = 0 to V _{DD} | -1uA | 1uA |
| Output High Voltage | V _{OH} | I _{OH} = - 4mA | 2.4 | |
| Output Low Voltage | V _{OL} | I _{LO} = + 4mA | | 0.4V |

Power Supply Currents

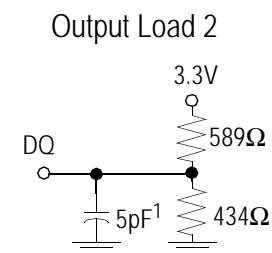
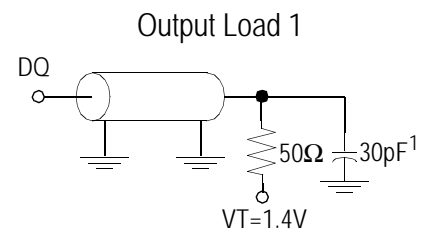
| Parameter | Symbol | Test Conditions | 0 to 70°C | | | | -40 to 85°C | | |
|--------------------------|------------------|--|-----------|-------|-------|-------|-------------|-------|-------|
| | | | 8ns | 10ns | 12ns | 15ns | 10ns | 12ns | 15ns |
| Operating Supply Current | I _{DD} | $\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time I _{OUT} = 0 mA | 170mA | 145mA | 130mA | 110mA | 155mA | 140mA | 120mA |
| Standby Current | I _{SB1} | $\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time | 70mA | 65mA | 60mA | 55mA | 75mA | 70mA | 65mA |
| Standby Current | I _{SB2} | $\overline{CE} \geq V_{DD} - 0.2V$ All other inputs $\geq V_{DD} - 0.2V$ or $\leq 0.2V$ | 30mA | | | | 40mA | | |

AC Test Conditions

| Parameter | Conditions |
|------------------------|-----------------------|
| Input high level | V _{IH} =2.4V |
| Input low level | V _{IL} =0.4V |
| Input rise time | t _r =1V/ns |
| Input fall time | t _f =1V/ns |
| Input reference level | 1.4V |
| Output reference level | 1.4V |
| Output load | Fig. 1 & 2 |

Note:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OZH}.



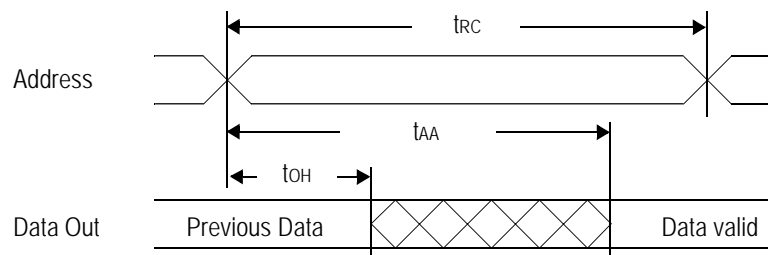
AC Characteristics

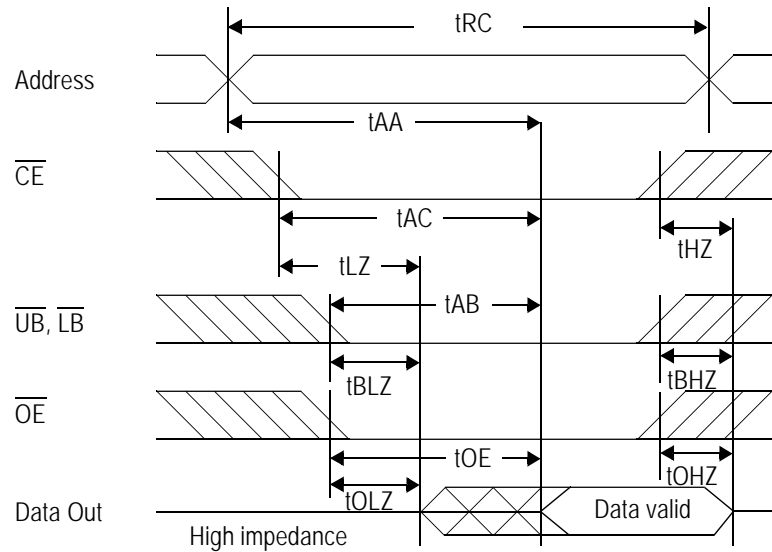
Read Cycle

| Parameter | Symbol | -8 | | -10 | | -12 | | -15 | | Unit |
|--|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read cycle time | t_{RC} | 8 | --- | 10 | --- | 12 | --- | 15 | --- | ns |
| Address access time | t_{AA} | --- | 8 | --- | 10 | --- | 12 | --- | 15 | ns |
| Chip enable access time (\overline{CE}) | t_{AC} | --- | 8 | --- | 10 | --- | 12 | --- | 15 | ns |
| Byte enable access time (\overline{UB} , \overline{LB}) | t_{AB} | --- | 3.5 | --- | 4 | --- | 5 | --- | 6 | ns |
| Output enable to output valid (\overline{OE}) | t_{OE} | --- | 3.5 | --- | 4 | --- | 5 | --- | 6 | ns |
| Output hold from address change | t_{OH} | 3 | --- | 3 | --- | 3 | --- | 3 | --- | ns |
| Chip enable to output in low Z (\overline{CE}) | t_{LZ}^* | 3 | --- | 3 | --- | 3 | --- | 3 | --- | ns |
| Output enable to output in low Z (\overline{OE}) | t_{OLZ}^* | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Byte enable to output in low Z (\overline{UB} , \overline{LB}) | t_{BLZ}^* | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Chip disable to output in High Z (\overline{CE}) | t_{HZ}^* | --- | 4 | --- | 5 | --- | 6 | --- | 7 | ns |
| Output disable to output in High Z (\overline{OE}) | t_{OHZ}^* | --- | 3.5 | --- | 4 | --- | 5 | --- | 6 | ns |
| Byte disable to output in High Z (\overline{UB} , \overline{LB}) | t_{BHZ}^* | --- | 3.5 | --- | 4 | --- | 5 | --- | 6 | ns |

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} and, or $\overline{LB} = V_{IL}$

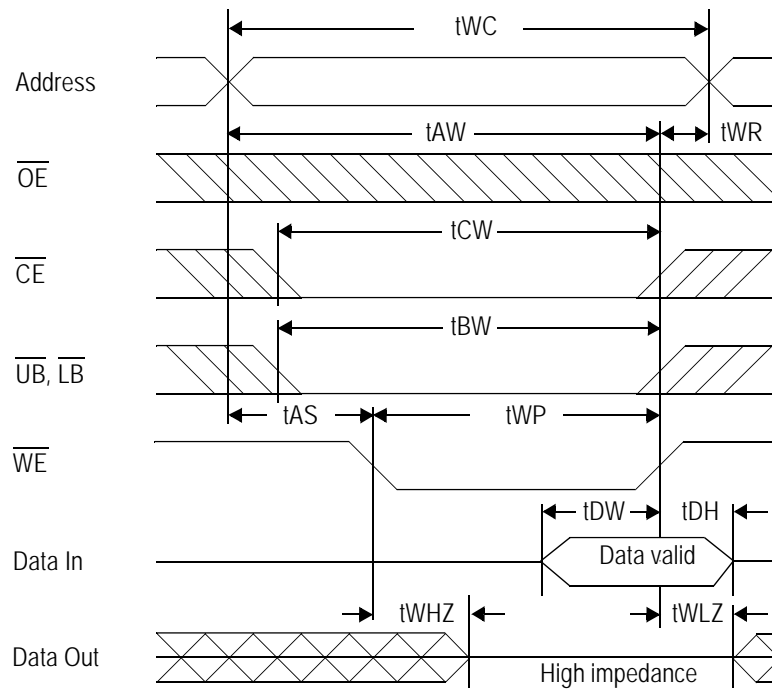
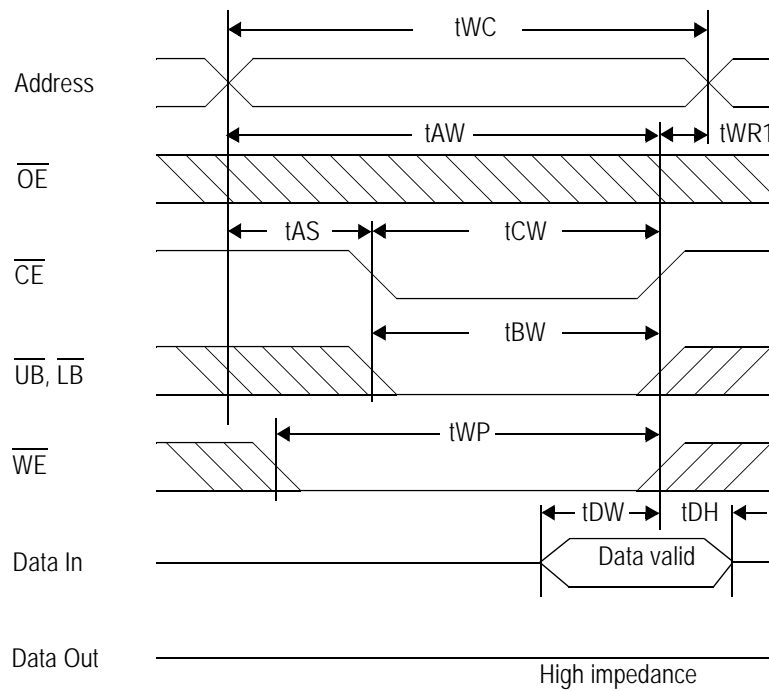


Read Cycle 2: $\overline{WE} = V_{IH}$


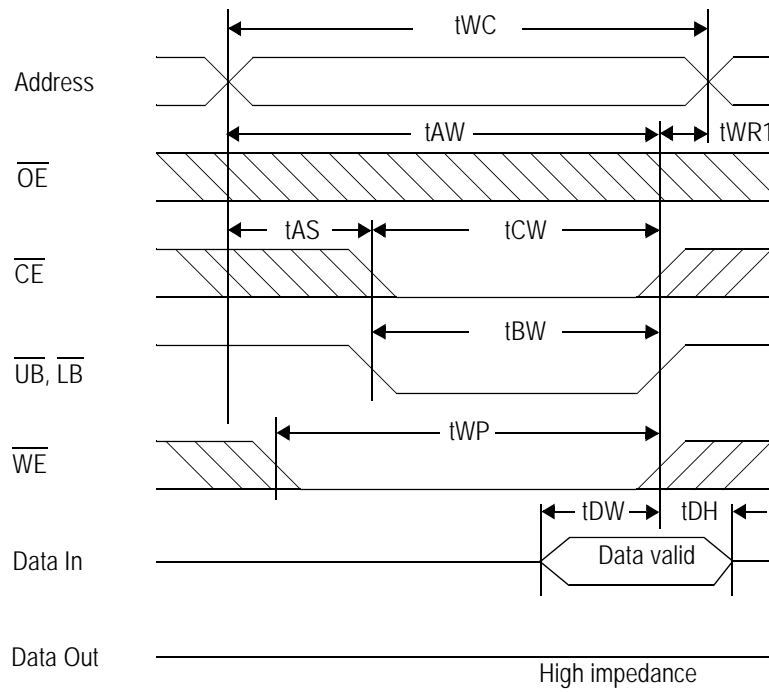
Write Cycle

| Parameter | Symbol | -8 | | -10 | | -12 | | -15 | | Unit |
|---|-------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 8 | --- | 10 | --- | 12 | --- | 15 | --- | ns |
| Address valid to end of write | t_{AW} | 5.5 | --- | 7 | --- | 8 | --- | 10 | --- | ns |
| Chip enable to end of write | t_{CW} | 5.5 | --- | 7 | --- | 8 | --- | 10 | --- | ns |
| Byte enable to end of write | t_{BW} | 5.5 | --- | 7 | --- | 8 | --- | 10 | --- | ns |
| Data set up time | t_{DW} | 4 | --- | 5 | --- | 6 | --- | 7 | --- | ns |
| Data hold time | t_{DH} | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Write pulse width | t_{WP} | 5.5 | --- | 7 | --- | 8 | --- | 10 | --- | ns |
| Address set up time | t_{AS} | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time (\overline{WE}) | t_{WR} | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Write recovery time (\overline{CE}) | t_{WR1} | 0 | --- | 0 | --- | 0 | --- | 0 | --- | ns |
| Output Low Z from end of write | t_{WLZ}^* | 3 | --- | 3 | --- | 3 | --- | 3 | --- | ns |
| Write to output in High Z | t_{WHZ}^* | --- | 3.5 | --- | 4 | --- | 5 | --- | 6 | ns |

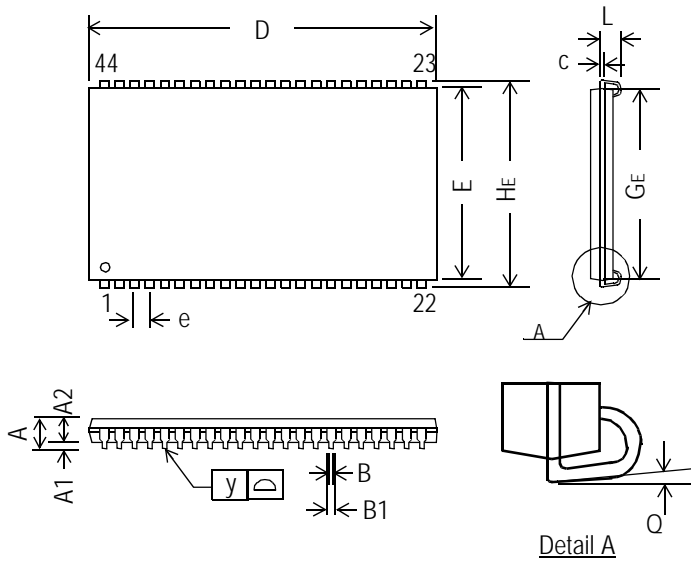
* These parameters are sampled and are not 100% tested

Write Cycle 1: \overline{WE} control

 Write Cycle 2: \overline{CE} control


Write Cycle 3: \overline{UB} , \overline{LB} control



44 Pin, 400 mil SOJ

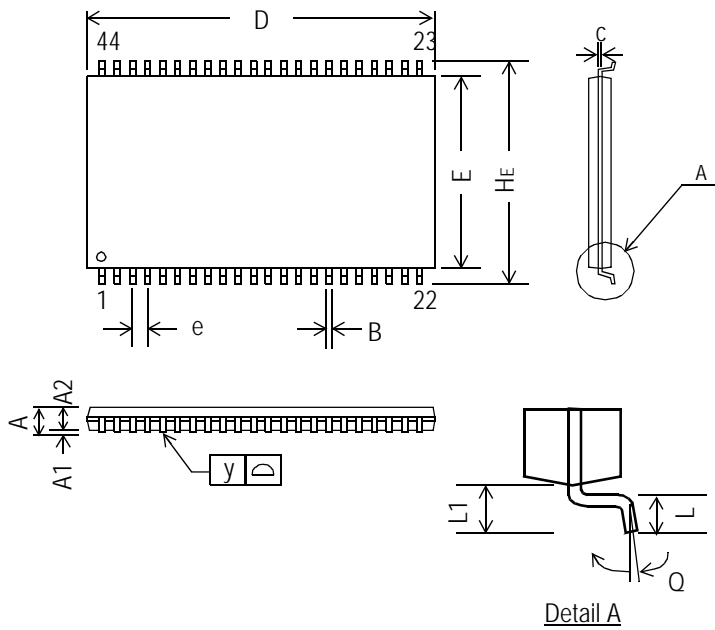


| Symbol | Dimension in inch | | | Dimension in mm | | |
|--------|-------------------|-------|-------|-----------------|--------|--------|
| | min | nom | max | min | nom | max |
| A | - | - | 0.148 | - | - | 3.759 |
| A1 | 0.025 | - | - | 0.635 | - | - |
| A2 | 0.105 | 0.110 | 0.115 | 2.667 | 2.794 | 2.921 |
| B | - | 0.018 | - | - | 0.457 | - |
| B1 | 0.026 | 0.028 | 0.032 | 0.660 | 0.711 | 0.813 |
| c | - | 0.008 | - | - | 0.203 | - |
| D | 1.120 | 1.125 | 1.130 | 28.44 | 28.58 | 28.70 |
| E | 0.395 | 0.400 | 0.405 | 10.033 | 10.160 | 10.287 |
| e | - | 0.05 | - | - | 1.27 | - |
| HE | 0.435 | 0.440 | 0.445 | 11.049 | 11.176 | 11.303 |
| GE | 0.360 | 0.370 | 0.380 | 9.144 | 9.398 | 9.652 |
| L | 0.082 | 0.087 | 0.106 | 2.083 | 2.210 | 2.70 |
| y | - | - | 0.004 | - | - | 0.102 |
| Q | 0° | - | 7° | 0° | - | 7° |

Note:

1. Dimension D & E do not include interlead flash
2. Dimension B1 does not include dambar protrusion / intrusion

44 Pin, 400 mil TSOP-II

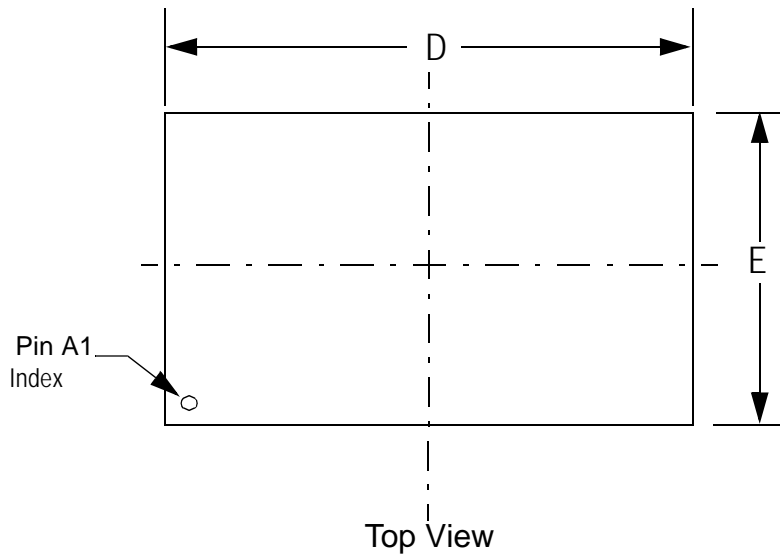


| Symbol | Dimension in inch | | | Dimension in mm | | |
|--------|-------------------|-------|-------|-----------------|-------|-------|
| | min | nom | max | min | nom | max |
| A | - | - | 0.047 | - | - | 1.20 |
| A1 | 0.002 | - | - | 0.05 | - | - |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| B | 0.01 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | - | 0.006 | - | - | 0.15 | - |
| D | 0.721 | 0.725 | 0.729 | 18.31 | 18.41 | 18.51 |
| E | 0.396 | 0.400 | 0.404 | 10.06 | 10.16 | 10.26 |
| e | - | 0.031 | - | - | 0.80 | - |
| HE | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| L1 | - | 0.031 | - | - | 0.80 | - |
| y | - | - | 0.004 | - | - | 0.10 |
| Q | 0° | - | 5° | 0° | - | 5° |

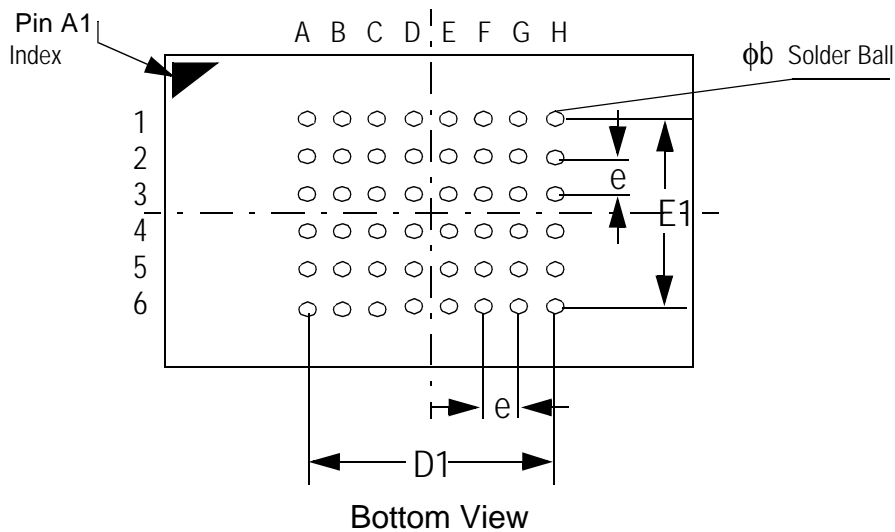
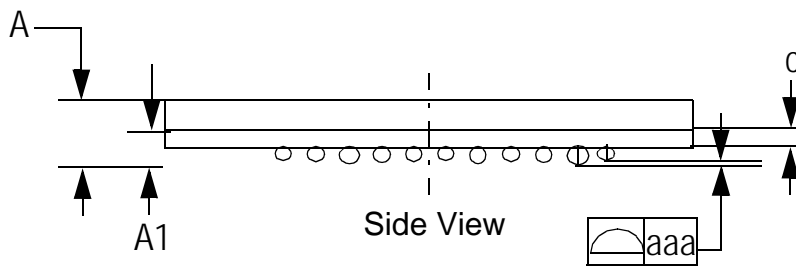
Note:

1. Dimension D & E do not include interlead flash
2. Dimension B does not include dambar protrusion / intrusion
3. Controlling dimension: mm

7.2mmx11.65mm FP-BGA



| Symbol | Unit: mm |
|--------|------------|
| A | 1.10±0.10 |
| A1 | 0.22±0.05 |
| φb | φ0.35 |
| c | 0.36(TYP) |
| D | 11.65±0.10 |
| D1 | 5.25 |
| E | 7.20±0.10 |
| E1 | 3.75 |
| e | 0.75(TYP) |
| aaa | 0.10 |



Ordering Information

| Part Number * | Package | Access Time | Temp. Range | Status |
|---------------|-----------------|-------------|-------------|--------|
| GS74116TP-8 | 400 mil TSOP-II | 8 ns | Commercial | |
| GS74116TP-10 | 400 mil TSOP-II | 10 ns | Commercial | |
| GS74116TP-12 | 400 mil TSOP-II | 12 ns | Commercial | |
| GS74116TP-15 | 400 mil TSOP-II | 15 ns | Commercial | |
| GS74116TP-8I | 400 mil TSOP-II | 8 ns | Industrial | |
| GS74116TP-10I | 400 mil TSOP-II | 10 ns | Industrial | |
| GS74116TP-12I | 400 mil TSOP-II | 12 ns | Industrial | |
| GS74116TP-15I | 400 mil TSOP-II | 15 ns | Industrial | |
| GS74116J-8 | 400 mil SOJ | 8 ns | Commercial | |
| GS74116J-10 | 400 mil SOJ | 10 ns | Commercial | |
| GS74116J-12 | 400 mil SOJ | 12 ns | Commercial | |
| GS74116J-15 | 400 mil SOJ | 15 ns | Commercial | |
| GS74116J-8I | 400 mil SOJ | 8 ns | Industrial | |
| GS74116J-10I | 400 mil SOJ | 10 ns | Industrial | |
| GS74116J-12I | 400 mil SOJ | 12 ns | Industrial | |
| GS74116J-15I | 400 mil SOJ | 15 ns | Industrial | |
| GS74116U-8 | Fine Pitch BGA | 8 ns | Commercial | |
| GS74116U-10 | Fine Pitch BGA | 10 ns | Commercial | |
| GS74116U-12 | Fine Pitch BGA | 12 ns | Commercial | |
| GS74116U-15 | Fine Pitch BGA | 15 ns | Commercial | |
| GS74116U-8I | Fine Pitch BGA | 8 ns | Industrial | |
| GS74116U-10I | Fine Pitch BGA | 10 ns | Industrial | |
| GS74116U-12I | Fine Pitch BGA | 12 ns | Industrial | |
| GS74116U-15I | Fine Pitch BGA | 15 ns | Industrial | |

* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS74116TP-10T

Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page #/Revisions/Reason |
|--|---------------------------------------|--|
| Rev1.03c 3/1999; 1.04d 6/1999 | Format/Typos | Document/Changed format of subscripts on pins to small caps. |
| | Content | 13/Changed Tape and Reel Note at end of Ordering info./Enhancement |
| 1.04d 6/1999; 2.00 8/1999 | Format/Typos | None |
| | Content | 1. Added Fine Pitch BGA package to datasheet. 2. 10/Added Dimension "D" to SOJ package diagram/Was missing 3. 11/Added Dimension "D" to TSOP package diagram/Was missing |
| GS741Rev2.01KRev 21 2/2000L | Format/Content | 1. GSI Logo 2. |
| GS74116 Rev2.01 2/2000L; Rev 2.02 3/2000N | Content | 1. Changed Pin A17 from 3E to 3D. |