Low noise Quasi-PWM/PFM Asynchronous Step Down Converter

Features

- **+2.8V to +6V Input Range**
- **Adjustable Output from 0.5V to V_{CC}−1V**
- **3A Guaranteed Output Current**
- **95% Efficiency**
- **Very Low Quiescent Current: 30uA(Typ.)**
- **100% Duty Cycle for low dropout mode**
- **600kHz +-30% Quasi PWM Operation.**
- **Small, 6-Pin SOT23 Package**

Applications

- **Desktop and Notebook Computers**
- **LAN Servers**
- **Industrial Controls**
- **PDA**
- **Digital Still Camera**
- **Central Office Telecom Equipment**

General Description

The G5410 is a low-noise, Quasi PWM/PFM, DC-DC step-down converter. It powers low voltage logic and core in small portable systems such as cellular phones, communicating PDAs, and handy-terminals.

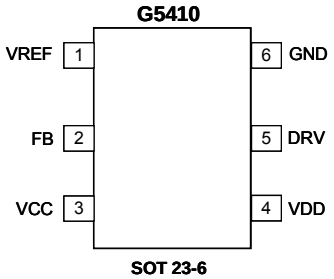
The device features an internal MOSFET driver to be high efficiency buck DC/DC converter. Excellent noise characteristics and near fixed frequency operation provide easy post-filtering. The G5410 is ideally suited for Li-Ion battery applications. It is also useful for +3V or +5V fixed input applications. The device automatic operates in two modes for higher efficiency. PWM mode operates at a fixed frequency regardless of the load. PFM Mode extends battery life by switching to a pulse-skipping mode during light loads, it reducing quiescent supply current to under 30μA.

The G5410 can deliver over 3A. The output voltage can be adjusted from 0.5V to V_{CC}-1V by external reference with the input range of +2.8V to +6V. Other features of the G5410 include high efficiency, low dropout mode (100% duty) at input low voltage stage. It is available in a space-saving 6-pin SOT23-6 package

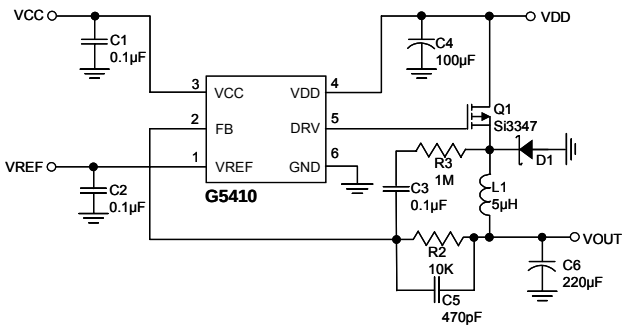
Ordering Information

Part*	Temp. range	Pin-package
G5410	-40°C to +85°C	SOT23-6

Pin Configuration



Typical Operating Circuit



Absolute Maximum Ratings

V_{CC} to GND……-0.3V to +7V
Output Short-Circuit Duration……Infinite
V_{DD} to GND……-0.3V to +7V
V_{FB} to GND……-0.3V to +7V
V_{REF} to GND……-0.3V to +7V
V_{DRV} to GND……-0.3V to +7V
Junction Temperature……+150°C
Storage Temperature Range……-65°C to +160°C
Lead Temperature (soldering, 10sec)……+300°C

Recommend Operating Range

Supply Voltage (V_{CC}) ……+2.8V to +6.0V
Driver Voltage (V_{DD}). ……+2.5V to +V_{CC}
Continuous Power Dissipation (T_A = +25°C)
SOT23-6……520 mW
SOT23-6 Thermal Resistance θ_{JA}……240°C/Watt

Electrical Characteristics (V_{CC} = 5V; V_{DD} = 5V, V_{REF}=1.8V, T_A=25°C, unless otherwise noted.) (Note1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
V_{CC} Input Voltage Range	V_{CC}		2.8		6.0	V
V_{DD} Driver Voltage Range	V_{DD}		2.5		V_{CC}	V
Quiescent Supply Current (I_{CC})	I_{CC}			30		µA
Quiescent Supply Current (I_{DD})	I_{DD}			0.2		µA
Input Pin Bias Current	I_{REF}	V_{REF}=1.8V		0.3		nA
	I_{FB}	V_{FB}=1.8V		0.3		
Input Offset Voltage	V_{IOS}	V_{REF}=1.8V	-10		10	mV
V_{REF} Operating Range	V_{REF}		-0.3		V_{CC}-1.6	V
Driver Pin High Level	V_{OH}	I_{OH}=10mA	V_{DD}-0.1			V
Driver Pin Low Level	V_{OL}	I_{OL}=10mA			0.01	V
Driver Resistance	R_{ONH}	Source I_{Source}=10mA		7.9		Ω
	R_{ONL}	Sink I_{Sink}=10mA		6.1		
Propagation Delay	t_{PGDH}	V_{REF}=1.8V V_{FB}=V_{REF}+50Mv C_{DRV}=2200pF		1.2		µS
	t_{PGDL}	V_{FB} =1.8V V_{REF} =V_{RB}+50mV C_{DRV}=2200pF		0.6		

Note 1: Limits is 100% production tested at T_A= +25°C. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Overview

The G5410 is buck (step-down) DC-DC controller that uses a Q-PWM control scheme. The control scheme is designed to quick response to output loading change at the FB pin, the gate drive (DRV pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9μs. The Q-PWM control does not provide an internal oscillator. Switching frequency depends on the external components and operating conditions. Operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures. Two external resistors can easily program the output voltage. The output can be set in a wide range from 0.5V to V_{IN}.

Quasi-PWM/PFM Control Circuit

The G5410 operates in discontinuous conduction mode at light load current or continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. Next cycle starts when the FB voltage reaches the internal voltage. Until then, the inductor current remains zero. Operating frequency is lower and switching losses reduce. In continuous conduction mode, current always flows through the inductor and never ramps down to zero. The output voltage (V_{OUT}) can be programmed by 2 external resistors. It can be calculated as following.

V_{OUT} = Vref x (R1 +R2)/R2

Functional Description

For example, with V_{OUT} set to 3.3V, V_{OUT_PP} is 26.6mV

V_{RIPPLE} = 0.01 x (33K + 20K) / 20K = 0.0266V

Operating frequency is determined by knowing the input voltage, output voltage, inductor, VHYST, ESR (Equivalent Series Resistance) of output capacitor, and the delay. It can be approximately calculated using the formula:

$$F = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN}-V_{OUT}) \times ESR}{V_{HYST} \times \alpha \times L)+(V_{IN} \times delay \times ESR)}$$

α : (R1+R2) / R2

delay: It includes the G5410 propagation delay time and the PFET delay time.

The operating frequency and output ripple voltage can also be significantly influenced by the speed up capacitor (Cff). Cff is connected in parallel with the high side feedback resistor, R1. The location of this capacitor is similar to where a feed forward capacitor would be located in a PWM control scheme. However it's effect on hysteretic operation is much different. The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Since the input to the feedback pin, FB, is a high impedance node, the current flows through R2. The end result is a reduction in output ripple and an increase in operating frequency. When adding Cff, calculate the formula above with α = 1. The value of Cff depend on the desired operating frequency and the value of R2. A good starting point is 470pF ceramic at 100kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 2.5V, the effect of Cff will decrease significantly.

Design Information

Hysteretic control is a simple control scheme. However the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, V_{IN}, or Cff is changed, there will be a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and C_{OUT} ESR.

Inductor Selection (L1)

The important parameters for the inductor are the inductance and the current rating. The G5410 operates over a wide frequency range and can use a wide range of inductance values. A good rule of thumb is to use the equations used for National's **Simple Switchers**®

The equation for inductor ripple as a function of output current is:

for i_{out} < 2.0Amps

$Di \leq i_{out} \times 0.386827 \times i_{out\ -.366726}$

for i_{out} > 2.0Amps

$Di \leq i_{out} \bullet 0.3$

The inductance can be calculated based upon the desired operating frequency where:

$$L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\triangle i} \times \frac{D}{f}$$

and

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{DS} - V_D}$$

where V_D is diode forward voltage.

The inductor should be rated to the following:

$I_{pk} = (I_{out}+Di/2)*1.1$

$$I_{RMS} = \sqrt{Iout^2 + \frac{\Delta i^2}{3}}$$

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the ESR.

Output Capacitor Selection (C_{OUT})

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the V_{HYST} sets the first order value of this ripple. As ESR is increased with a given inductance, then operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common de-sire of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor should be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provide highly accurate control over the output voltage ripple. The other types capacitor, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, Nichicon 'NA' series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

Input Capacitor Selection (C_{IN})

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on. The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manu-facturer's recommended voltage derating. For high input voltage application, low ESR electrolytic capacitor, the Nichicon 'UD' series or the Panasonic 'FK' series, is available. The RMS current in the input capacitor can be calculated.

$$I_{RMS\_CIN} = I_{OUT} \times \frac{V_{OUT} \times (V_{IN}-V_{OUT}))^{1/2}}{V_{IN}}$$

The input capacitor power dissipation can be calculated as follows.

$P_{D(CIN)} = I_{RMS\_CIN2} \times ES_{RCIN}$

The input capacitor must be able to handle the RMS current and the P_D. Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low ESR, high performance capacitor such as OS-CON or Tantalum. The capacitance value should be selected such that the ripple voltage created by the charge and discharge of the capacitance is less than 10% of the total ripple across the capacitor.

Catch Diode Selection

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated as following.

$I_{D\_AVE} = I_{OUT} \times (1 - D)$

The off state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a shottky diode is recommended. In low output voltage applications a low forward voltage provides improved efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

P-Channel MOSFET Selection (Q1)

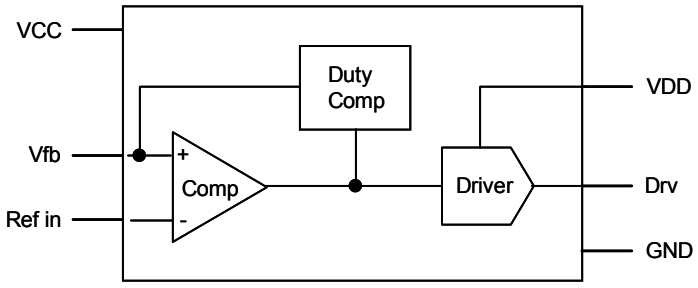
The important parameters for the PFET are the maximum Drain-Source voltage (V_{DS}), the on resistance (R_{DSON}), Current rating, and the input capacitance. The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage. DRV swings the PFET's gate from V_{IN} to V_{IN} - 5V when the input voltage is greater than 7V. At less than 7V input, the DRV voltage swing is smaller. At 4.5V input the DRV swings from V_{IN} to V_{IN} - 3.3V. To insure that the PFET turns on completely, a low threshold PFET should be used when the input voltage is less than 7V. RDSON and package size must be used to determine the appropriate FET for a given current as well as peak current capability. Switching losses also must be considered.

The first order losses in the FET are approximately:
PDswitch = R_{DSON} x I_{OUT} 2 x D +f x I_{OUT} x V_{IN} x (ton + toff) / 2
Where:
t_{on} = FET turn on time
t_{off} = FET turn off time
A value of 10ns to 20ns is typical for ton and t_{off}. The R_{DSON} is used in determining the current limit resistor value, R_{ADJ}. Note that the R_{DSON} has a positive temperature coefficient. At 100°C, the RDSON may be as much as 150% higher than the 25°C value. This increase in RDSON must be considered it when determining RADJ in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature. Keeping the gate capacitance below 2000pF is recommended to keep switching losses and transition times low. As gate capacitance increases, operating frequency should be reduced and as gate capacitance decreases operating frequency can be increased.

PCB Layout

The PC board layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and general EMI problems. For minimal inductance, the wires indicated by heavy lines should be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor, and FET drain, should be kept short. This node is one of the main sources for radiated EMI since it is an AC voltage at the switching frequency. It is always good practice to use a ground plane in the design, particularly at high currents. The gate pin of the external PFET should be located close to the DRV pin.
However, if a very small FET is used, a resistor may be required between DRV and the gate of the FET to reduce high frequency ringing. The feedback voltage signal line can be sensitive to noise. Make sure to avoid inductive coupling to the inductor or the switching node.

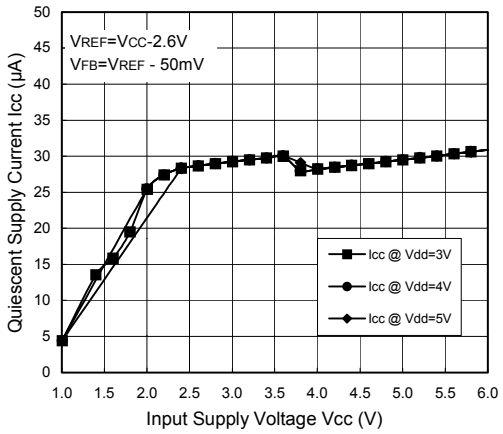
Block Diagram



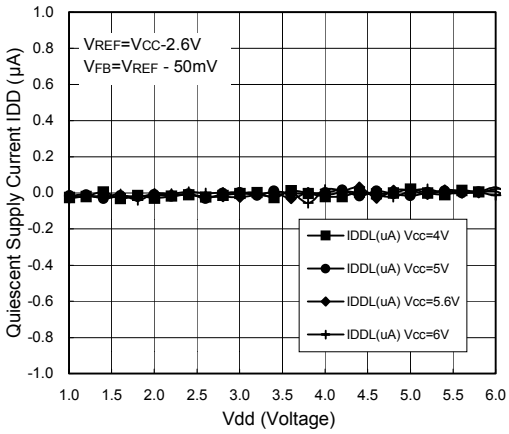
Typical Performance Characteristics

(V_{CC}= +5.0V, V_{DD}=+5.0V, C1=C2=0.1µF, C4=100µF, C6=150µF, V_{REF}=1.8V, T_A=25°C, unless otherwise noted.)

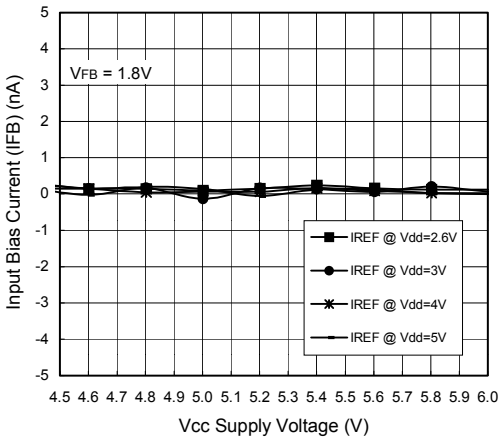
Quiescent Supply Current (ICC) vs. V_{CC}



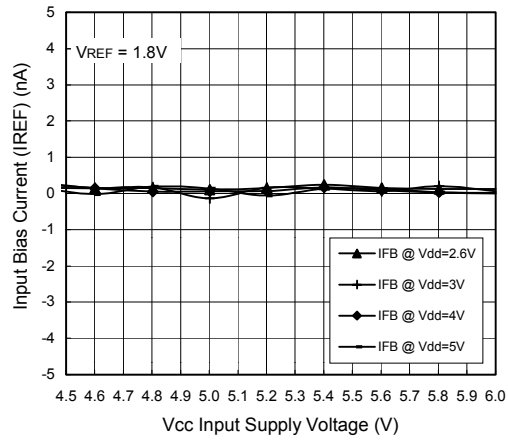
Quiescent Supply Current (IDD) vs. V_{DD}



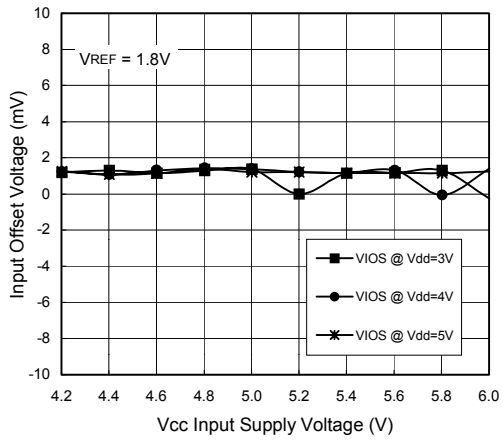
Input Bias Current (IFB) vs. V_{CC}



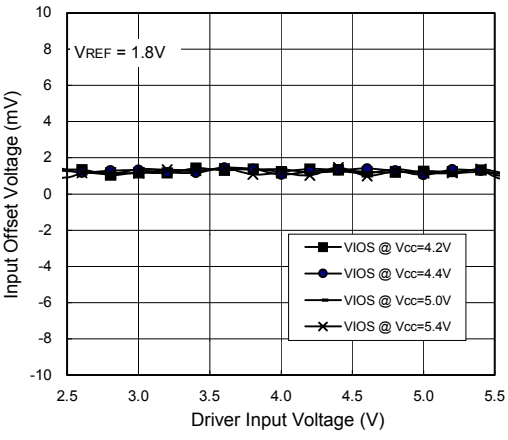
Input Bias Current (IREF) vs. V_{CC}



Input Offset Voltage vs. V_{CC}

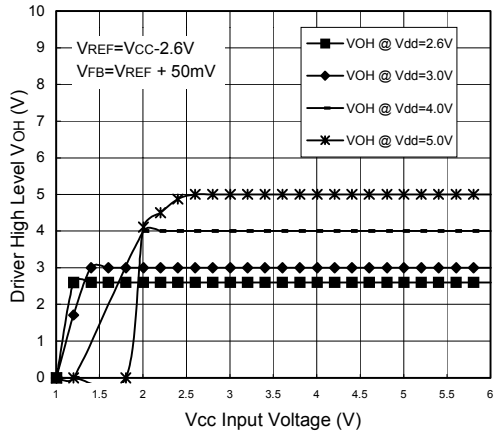


Input Offset Voltage vs. V_{DD}

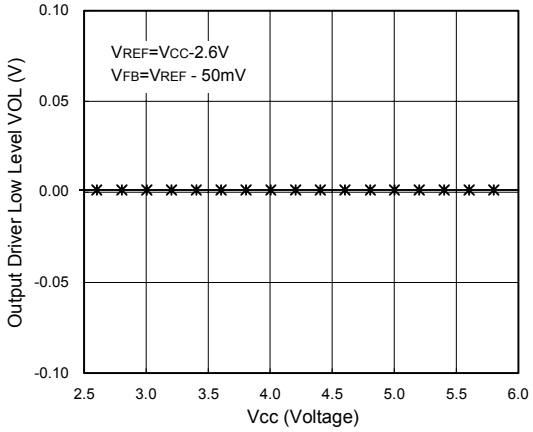


Typical Performance Characteristics (Continued)

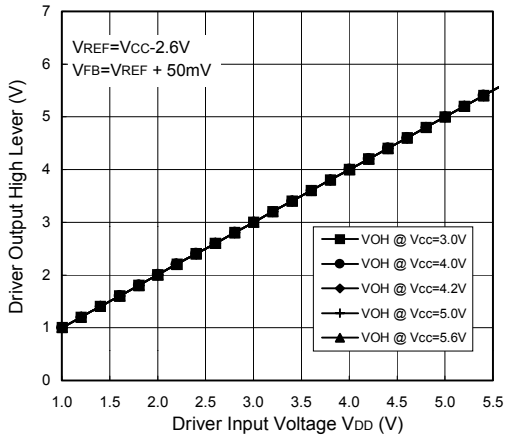
Driver High Level vs. Vcc



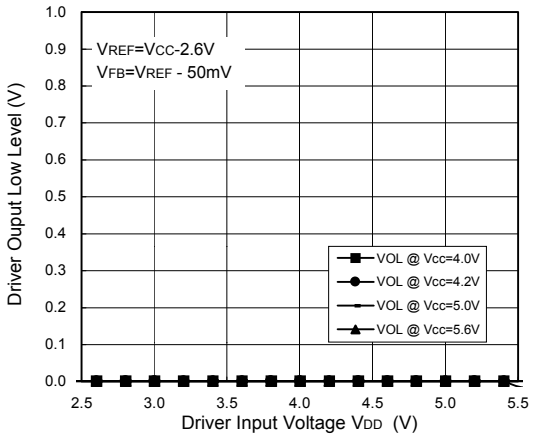
Driver Low Level vs. Vcc



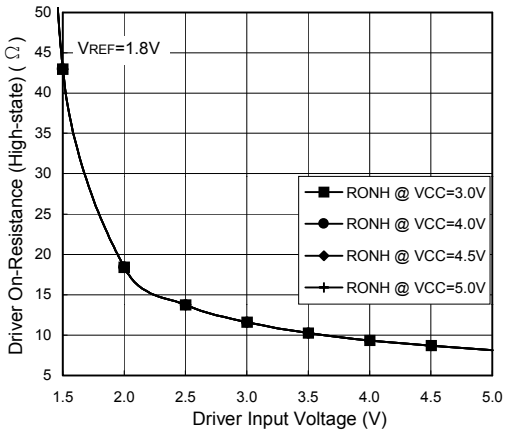
Driver High Level vs. V_{DD}



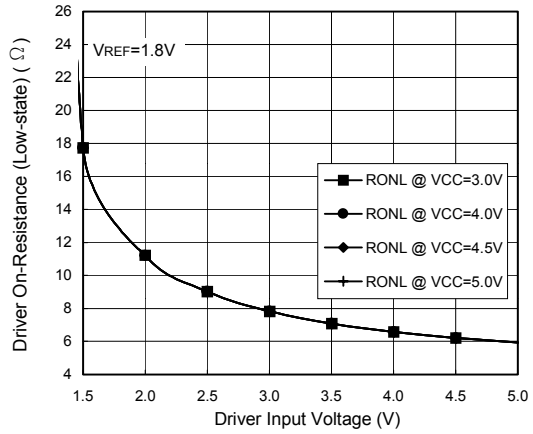
Driver Low Level vs. V_{DD}



Driver On-Resistance (High-state) vs. V_{DD}

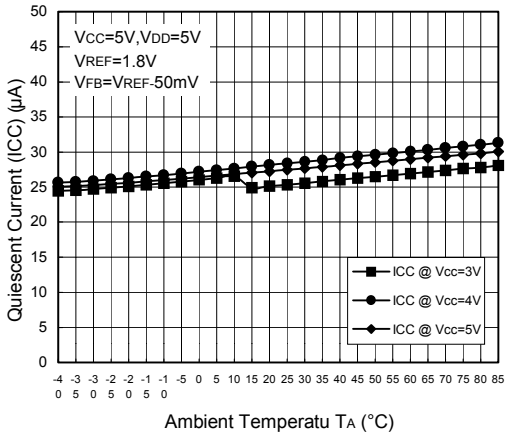


Driver On-Resistance (Low-state) vs. V_{DD}

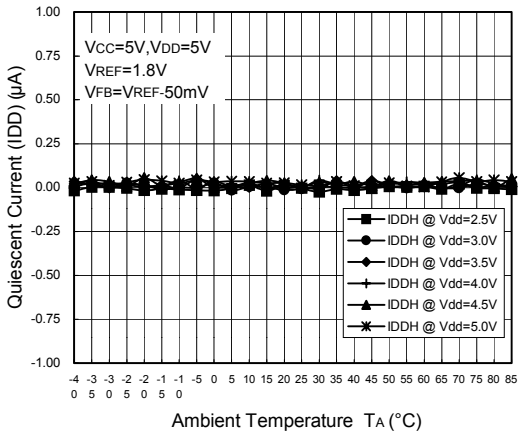


Typical Performance Characteristics (Continued)

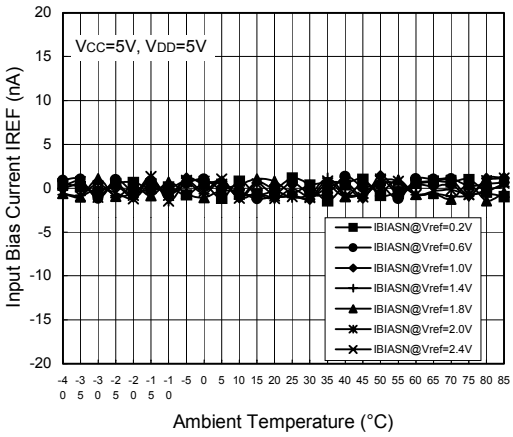
Quiescent Current (ICC) vs. Tempreature



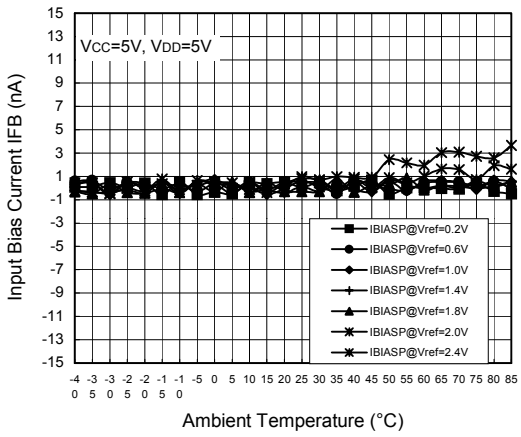
Quiescent Current (IDD) vs. Tempreature



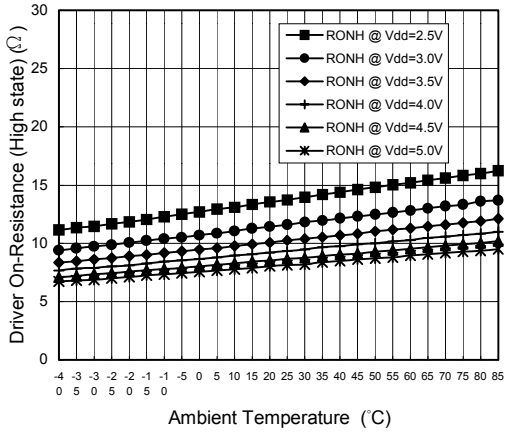
Input Bias Current (IREF) vs. Temperature



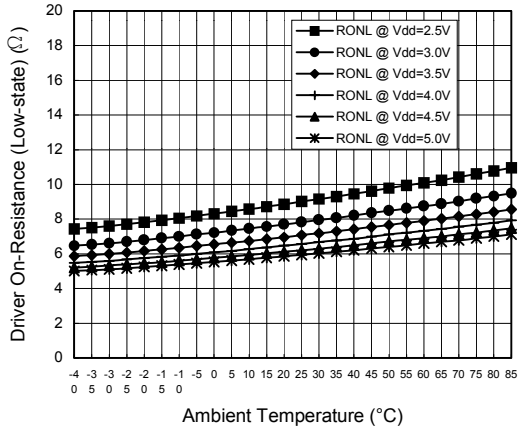
Input Bias Current (IFB) vs. Temperature



Driver On-Resistance (High-state) vs. Temperature

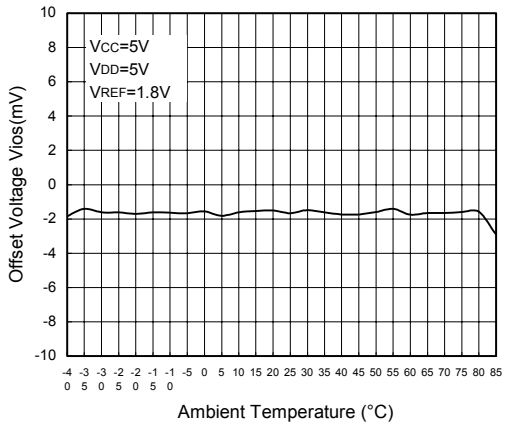


Driver On-Resistance (Low-state) vs. Temperature

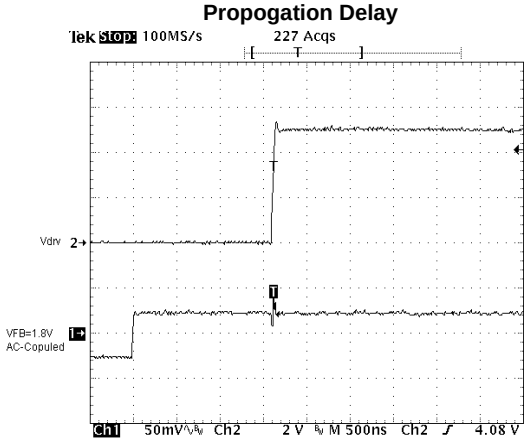


Typical Performance Characteristics (Continued)

Input Offset Voltage vs. Temperature

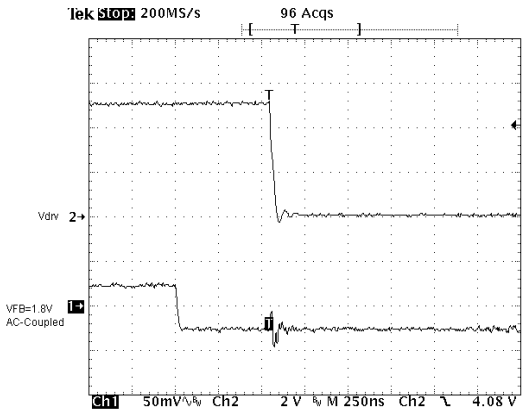


Propogation Delay



VCC=5V, Vdd=5V, VREF=1.8V, VFB=VREF+50mV input overdrive voltage,Cdrv=2200pF
Output driver into High

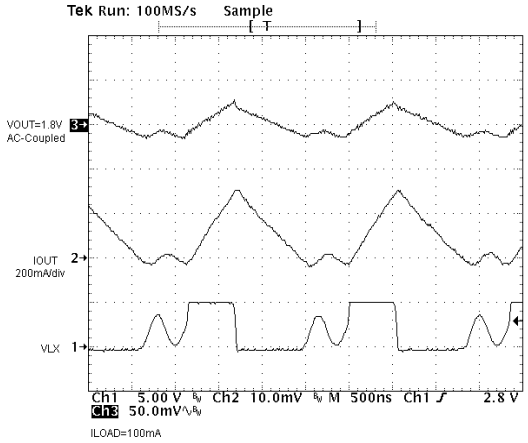
Propogation Delay



VCC=5V, VDD=5V, VFB=1.8V, VREF=VFB+50mV input overdrive voltage, Cdn=2200pF
Driver into Low

Discontinuous Mode Operation

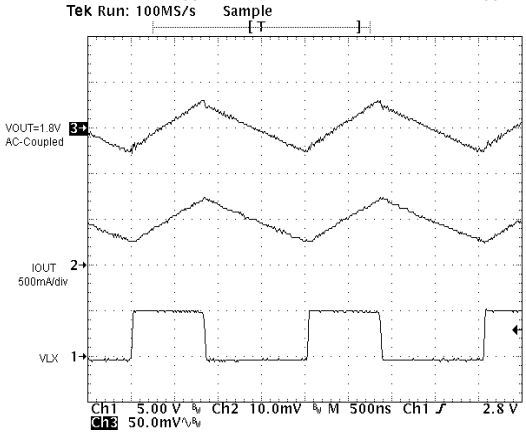
(V_{DD} 5V, V_{OUT} 1.8V, 100mA Load, 150µF tan C_{OUT})



ILOAD=100mA

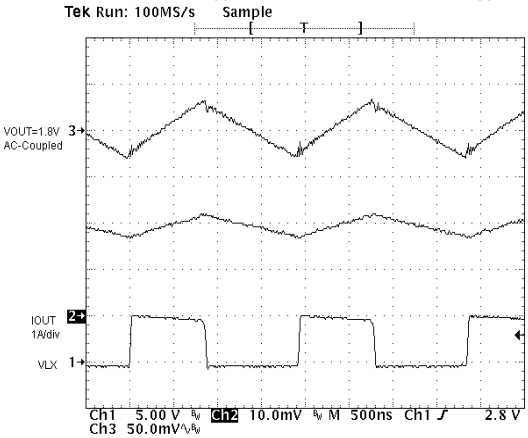
Continuous Mode Operation

(V_{DD} 5V, V_{OUT} 1.8V, 500mA Load, 150µF tan C_{OUT})



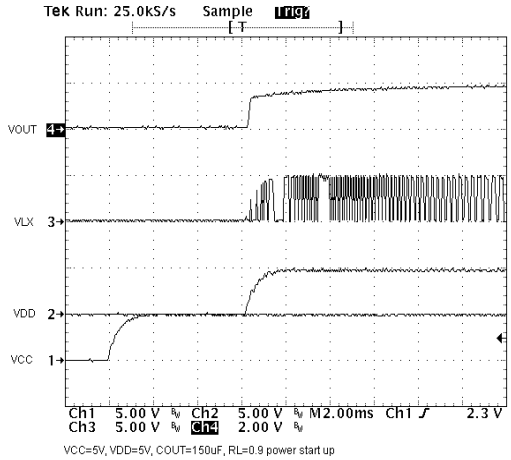
Continuous Mode Operation

(V_{DD} 5V, V_{OUT} 1.8V, 2A Load, 150µF tan C_{OUT})



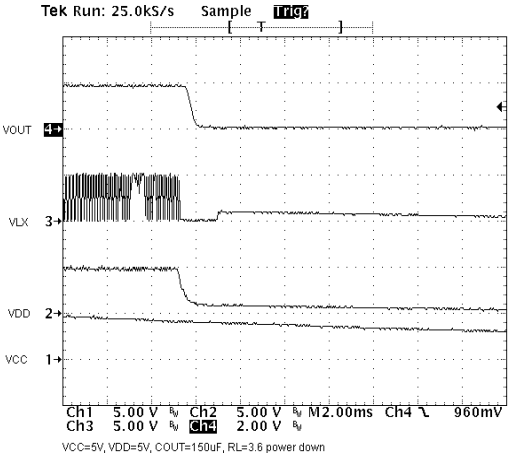
Typical Performance Characteristics (Continued)

Power Up Wafeworm



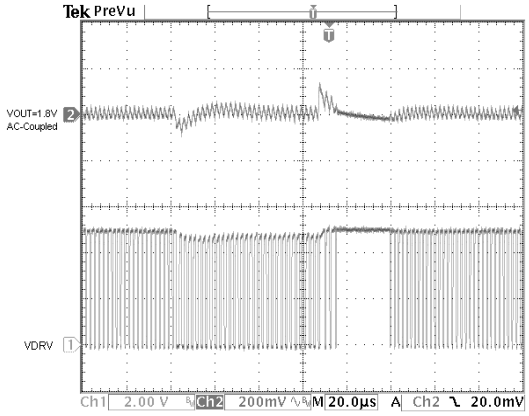
VCC=5V, VDD=5V, COUT=150uF, RL=0.9 power start up

Power Off Waveform



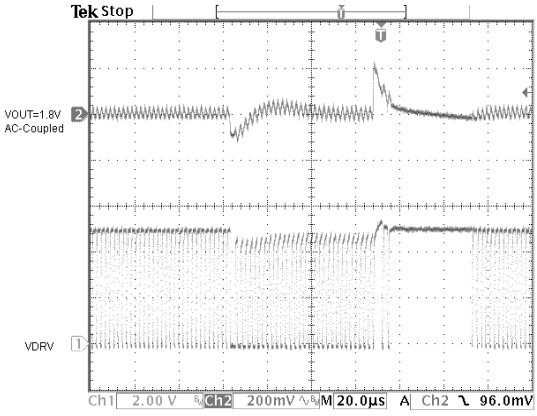
VCC=5V, VDD=5V, COUT=150uF, RL=3.6 power down

Load Transient Response (0.1A ⟷ 0.9A)



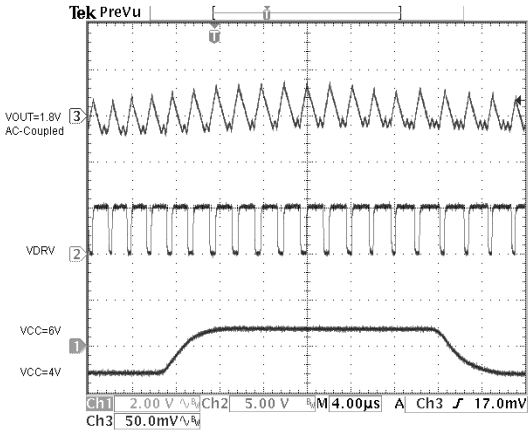
IOUT=100mA to 0.9A transient

Load Transient Response (0.1A ⟷ 2A)



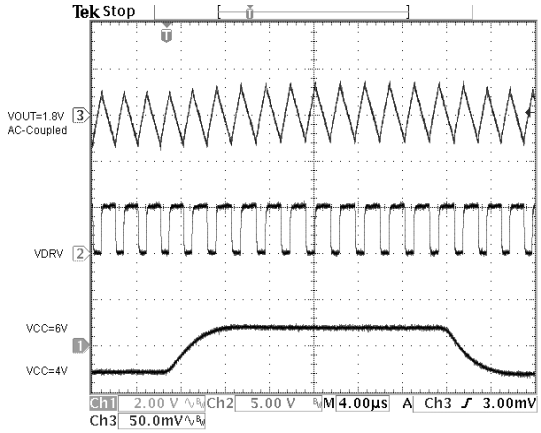
IOUT=100mA to 2A transient

V_{CC} Line Transient Response (I_{LOAD}=100mA)



VDD=5V, COUT=150uF, ILOAD=100mA

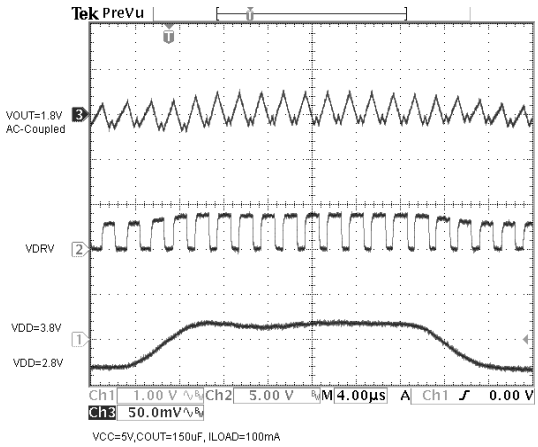
V_{CC} Line Transient Response (I_{LOAD}=500mA)



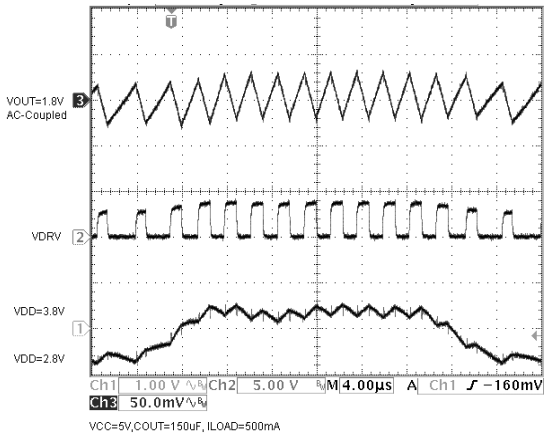
VDD=5V, COUT=150uF, ILOAD=500mA

Typical Performance Characteristics (Continued)

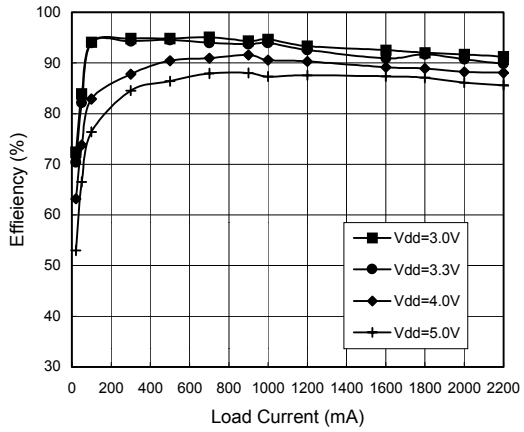
V_{DD} Line Transient Response (I_{LOAD}=100mA)



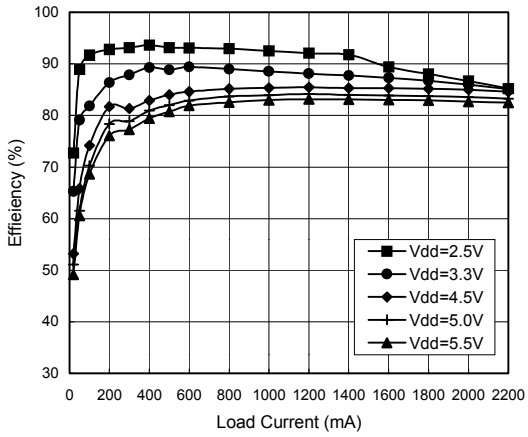
V_{DD} Line Transient Response (I_{LOAD}=500mA)



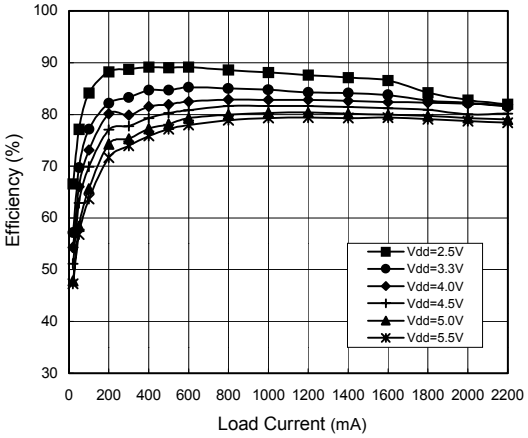
Efficiency vs. Load Current (V_{OUT}=2.5V)



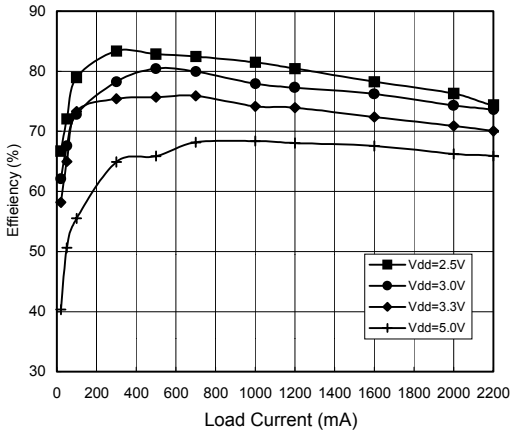
Efficiency vs. Load Current (V_{OUT}=1.8V)



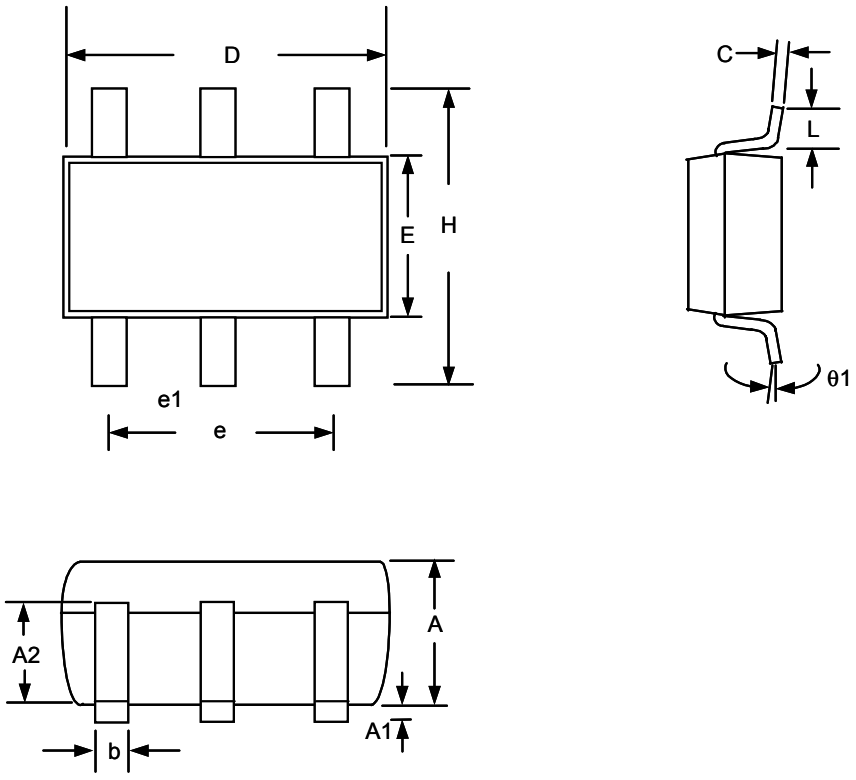
Efficiency vs. Load Current (V_{OUT}=1.5V)



Efficiency vs. Load Current (V_{OUT}=1.25V)



Package Information

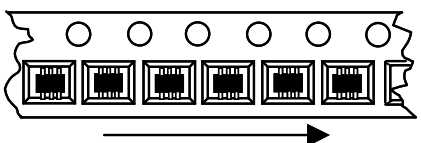


Note:

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1000 mm (4mil) unless otherwise specified
3. Coplanarity: 0.1000mm
4. Dimension L is measured in gage plane

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	-----	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.40	1.60	1.80
e	-----	1.90(TYP)	-----
H	2.60	2.80	3.00
L	0.37	------	-----
θ 1	1°	5°	9°

Taping Specification



Feed Direction

SOT 23-6 Package Orientation