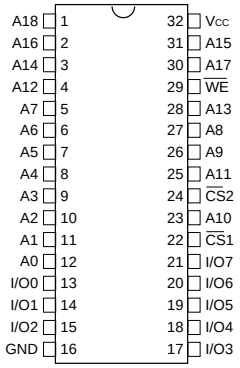
2x512Kx8 DUALITHIC™ SRAM

*ADVANCED**

PIN CONFIGURATION FOR WS1M8V-XCX

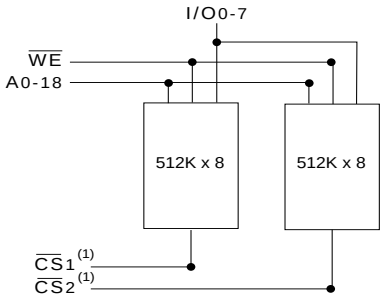
32 DIP
TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}_{1-2}$	Chip Selects
$\overline{WE}$	Write Enable
V_{CC}	+3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



NOTE:

1. $\overline{CS}_1$ and $\overline{CS}_2$ are used to select the lower and upper 512Kx8 of the device. $\overline{CS}_1$ and $\overline{CS}_2$ must not be enabled at the same time.

FEATURES

- Access Times 70, 85, 100ns
- Evolutionary, Corner Power/Ground Pinout
- Packaging:
  - 32 pin, Hermetic Ceramic DIP (Package 300)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Output Enable Internally tied to GND.

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	+4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	5.5	V

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	Standby	High Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE: $\overline{OE}$ is internally tied to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	28	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	28	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}[1]	$\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}[1]	$\overline{CS}$ = V_{IL}, f = 5MHz, Vcc = 3.6		25	mA
Standby Current	I_{SB}[1]	$\overline{CS}$ = V_{IH}, f = 5MHz, Vcc = 3.6		800	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V , V_{IL} = 0.3V

1. $\overline{OE}$ is internally tied to GND.

AC CHARACTERISTICS

(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		ns
Address Access Time	t_{AA}		70		85		100	ns
Output Hold from Address Change	t_{OH}	5		5		5		ns
Chip Select Access Time	t_{ACS}		70		85		100	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		25	ns

1. This parameter is guaranteed by design but not tested.

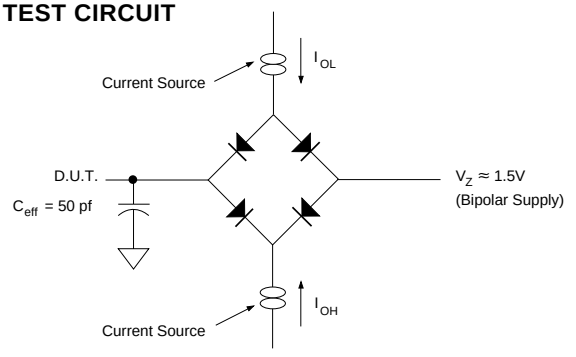
AC CHARACTERISTICS

(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		ns
Chip Select to End of Write	t_{CW}	60		75		80		ns
Address Valid to End of Write	t_{AW}	60		75		80		ns
Data Valid to End of Write	t_{DW}	30		30		40		ns
Write Pulse Width	t_{WP}	50		50		60		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

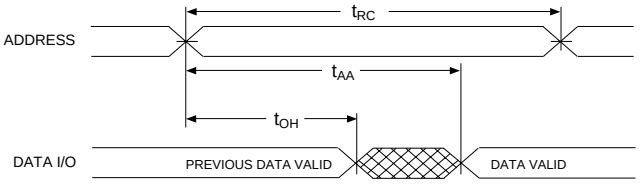


AC TEST CONDITIONS

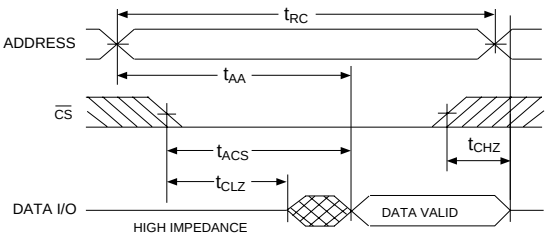
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75\ \Omega$.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE



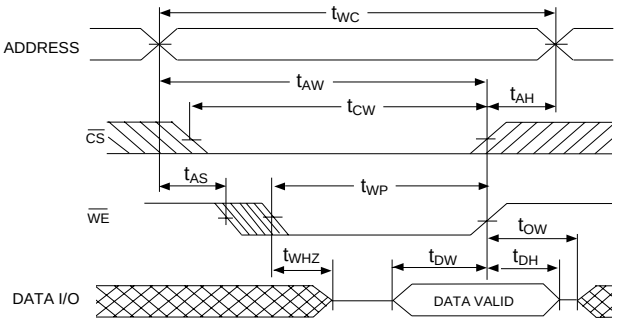
READ CYCLE 1 ($\overline{CS}$ = V_{IL}, $\overline{WE}$ = V_{IH})



READ CYCLE 2 ($\overline{WE}$ = V_{IH})

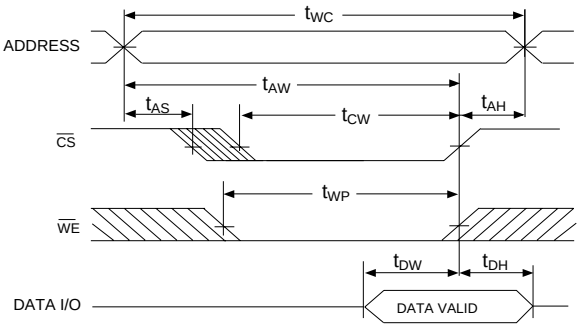
NOTE: $\overline{OE}$ is internally tied to GND.

WRITE CYCLE - $\overline{WE}$ CONTROLLED



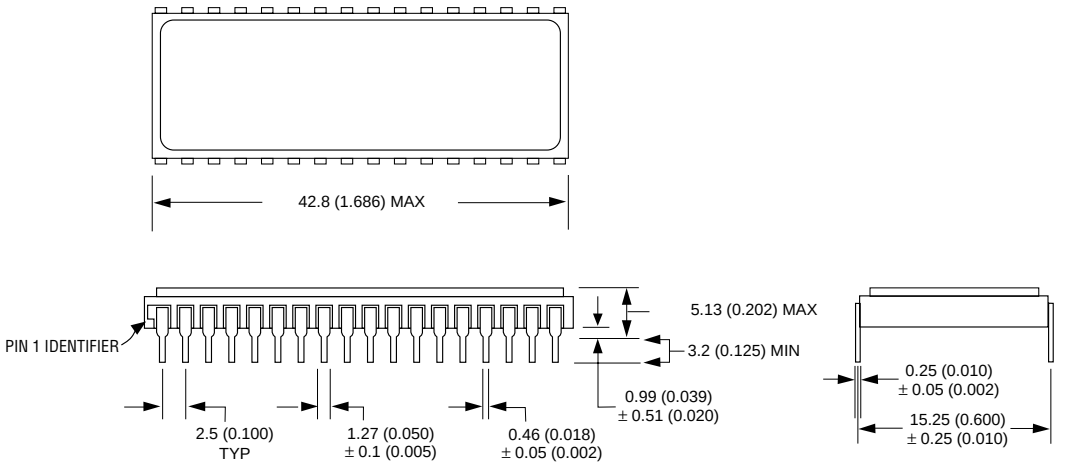
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 1M8 V - XXX C X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

M =	Military Screened	-55°C to +125°C
I =	Industrial	-40°C to +85°C
C =	Commercial	0°C to +70°C

PACKAGE:
C = Ceramic 0.600" DIP (Package 300)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, two banks of 512K x 8

SRAM

WHITE ELECTRONIC DESIGNS CORP.