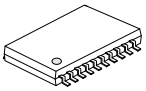
U74AHC377

CMOS IC

OCTAL D-TYPE FLIP-FLOPS WITH DATA ENABLE POSITIVE-EDGE TRIGGER



SOP-20

TSSOP-20

■ DESCRIPTION

The **U74AHC377** is a high-speed Si-gate CMOS device and is compatible with low-power Schottky TTL (LSTTL).

The **U74AHC377** has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock input (CLK) loads all flip-flops simultaneously when the data enable input ($\overline{EN}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. The $\overline{EN}$ input is only required to be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation.

■ FEATURES

* Balanced propagation delays
* All inputs have Schmitt-trigger actions
* Inputs accept voltages higher than V_{CC}
* Ideal for addressable register applications
* Data enable for address and data synchronization
* Eight positive-edge triggered D-type flip-flops

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC373L-S20-T	U74AHC373G-S20-T	SOP-20	Tube
U74AHC373L-S20-R	U74AHC373G-S20-R	SOP-20	Tape Reel
U74AHC373L-P20-T	U74AHC373G-P20-T	TSSOP-20	Tube
U74AHC373L-P20-R	U74AHC373G-P20-R	TSSOP-20	Tape Reel

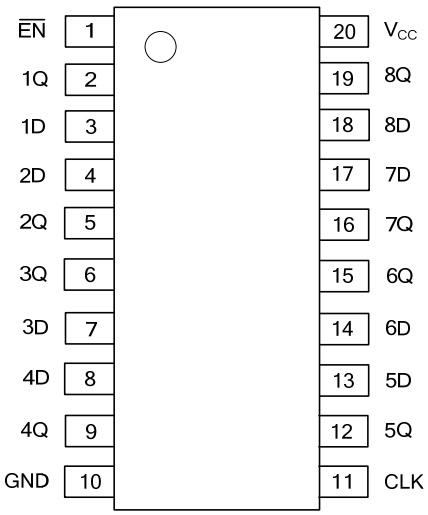
U74AHC377L-P20-T

(1)Packing Type — (1) T: Tube, R: Tape Reel

(2)Package Type — (2) P20: TSSOP-20, S20: SOP-20

(3)Lead Plating — (3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION



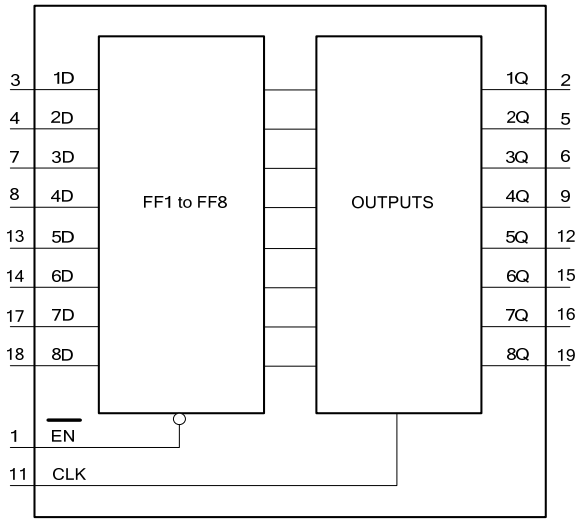
■ PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
$\overline{EN}$	1	Data Enable Input (Active low)
1Q	2	Flip-flop Output
1D	3	Data Input
2D	4	Data Input
2Q	5	Flip-flop Output
3Q	6	Flip-flop Output
3D	7	Data Input
4D	8	Data Input
4Q	9	Flip-flop Output
GND	10	Ground (0V)
CLK	11	Clock Input (Low-to-High, Edge Triggered)
5Q	12	Flip-flop Output
5D	13	Data Input
6D	14	Data Input
6Q	15	Flip-Flop Output
7D	16	Flip-Flop Output
7Q	17	Data Input
8D	18	Data Input
8Q	19	Flip-Flop Output
V_{CC}	20	Supply Voltage

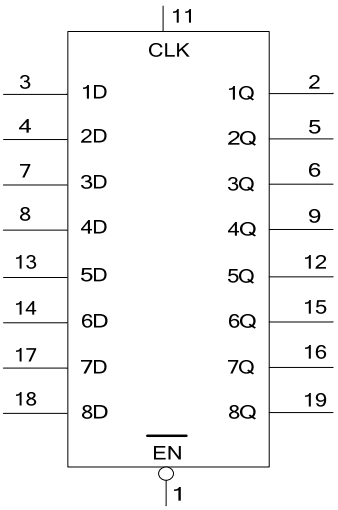
■ FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{EN}$	CLK	D	
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

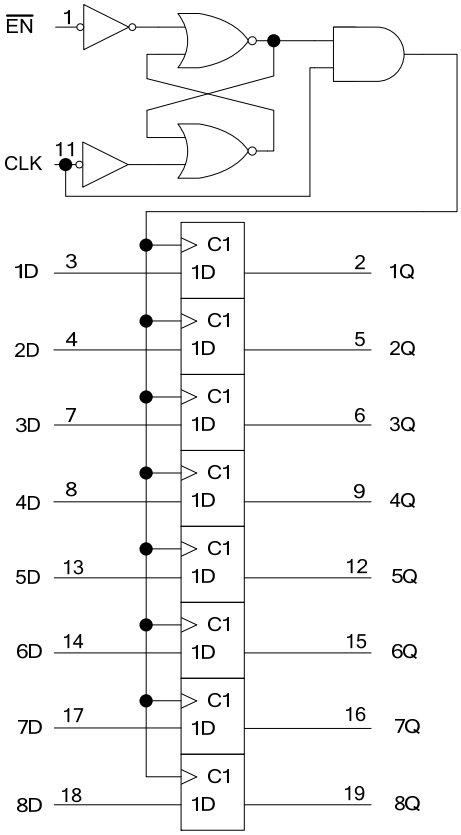
■ FUNCTIONAL DIAGRAM



■ LOGIC SYMBOL



■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		-0.5		7	V
Input Voltage	V_I		-0.5		7	V
V_{CC} or GND Current	I_{CC}		-75		+75	mA
Output Current	I_{OUT}	V_O=-0.5V to (V_{CC}+0.5V)	-25		+25	mA
Input Clamp Current	I_{IK}	V_I<-0.5V	-20			mA
Output Clamp Current	I_{OK}	V_O<-0.5V or V_O> V_{CC}+0.5V	-20		+20	mA
Storage Temperature	T_{STG}		-65		+150	°C

Note: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise and Fall Rate	Δt/Δv	V_{CC}=3V ~ 3.6V			100	ns/V
		V_{CC}=4.5V ~ 5.5V			20	
Ambient Temperature	T_A		-40	+25	+85	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-20	θ_{JA}	58	°C/W
	TSSOP-20		83	

■ ELECTRICAL CHARACTERISTICS (T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=3V	2.1			
		V_{CC}=5.5V	3.85			
Low-level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=3V			0.9	
		V_{CC}=5.5V			1.65	
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-50μA	1.9	2		V
		V_{CC}=3V, I_{OH}=-50μA	2.9	3		
		V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		
		V_{CC}=3V, I_{OH}=-4mA	2.58			
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OH}=50μA		0	0.1	V
		V_{CC}=3V, I_{OH}=50μA		0	0.1	
		V_{CC}=4.5V, I_{OH}=50μA		0	0.1	
		V_{CC}=3V, I_{OH}=4mA			0.36	
		V_{CC}=4.5V, I_{OH}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V to 5.5V, V_{IN}= 5.5V or GND			0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Input Capacitance	C_I	V_I=V_{cc} or GND		3	10	pF

■ DYNAMIC CHARACTERISTICS ($t_r = t_f \leq 3ns$, ground=0V, T_A =25°C, unless otherwise specified)

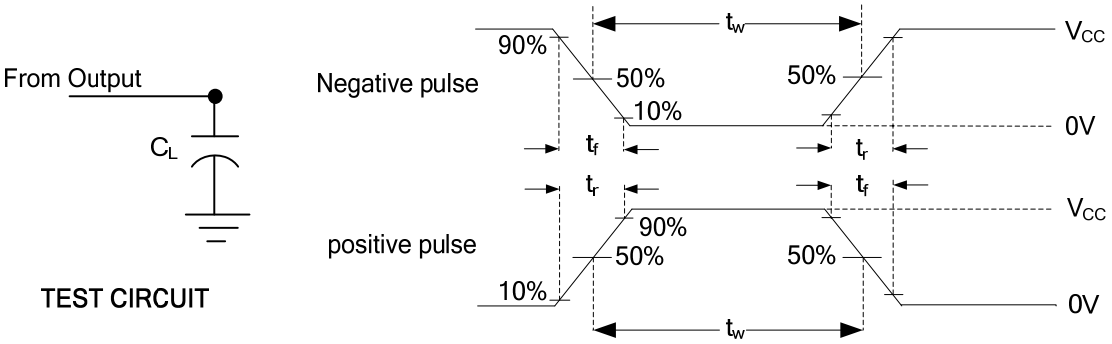
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
maximum frequency	f_{MAX}	V_{CC}=3V to 3.6V, C_L=15pF	80	125		ns
		V_{CC}=3V to 3.6V, C_L=50pF	50	75		
		V_{CC}=4.5V to 5.5V, C_L=15pF	125	175		
		V_{CC} =4.5V to 5.5V, C_L=50pF	85	120		
propagation delay, From CP to Qn	t_{PD}	V_{CC}=3V to 3.6V, C_L=15pF		5.6	12.8	ns
		V_{CC}=3V to 3.6V, C_L=50pF		8	16	
		V_{CC}=4.5V to 5.5V, C_L=15pF		3.9	9	
		V_{CC}=4.5V to 5.5V, C_L=50pF		5.6	10.5	
pulse width CP, From HIGH or LOW	t_W	V_{CC}=3V to 3.6V	5			ns
		V_{CC}=4.5V to 5.5V	5			
set-up time Dn, From $\overline{EN}$ to CP	t_{SU}	V_{CC}=3V to 3.6V	5			ns
		V_{CC}=4.5V to 5.5V	4.5			
hold time Dn, From $\overline{EN}$ to CP	t_H	V_{CC}=3V to 3.6V	1.5			ns
		V_{CC}=4.5V to 5.5V	2			

■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

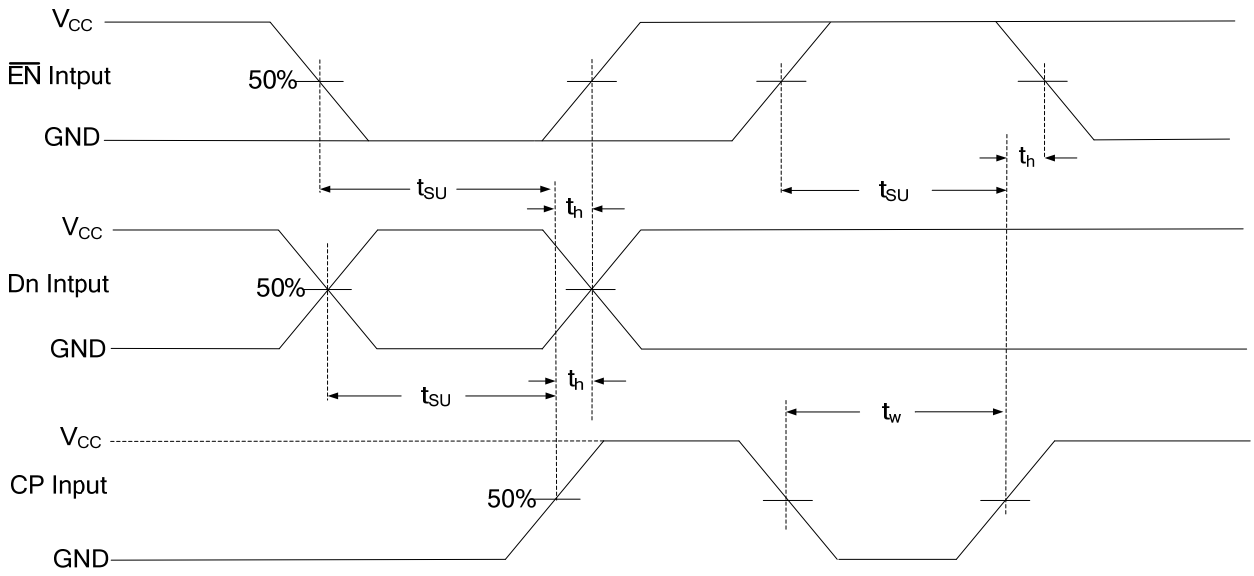
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	f=1MHz; V_I=GND to V_{CC}		20		pF

Note: t_{PLH} and t_{PHL} are the same as t_{PD}.

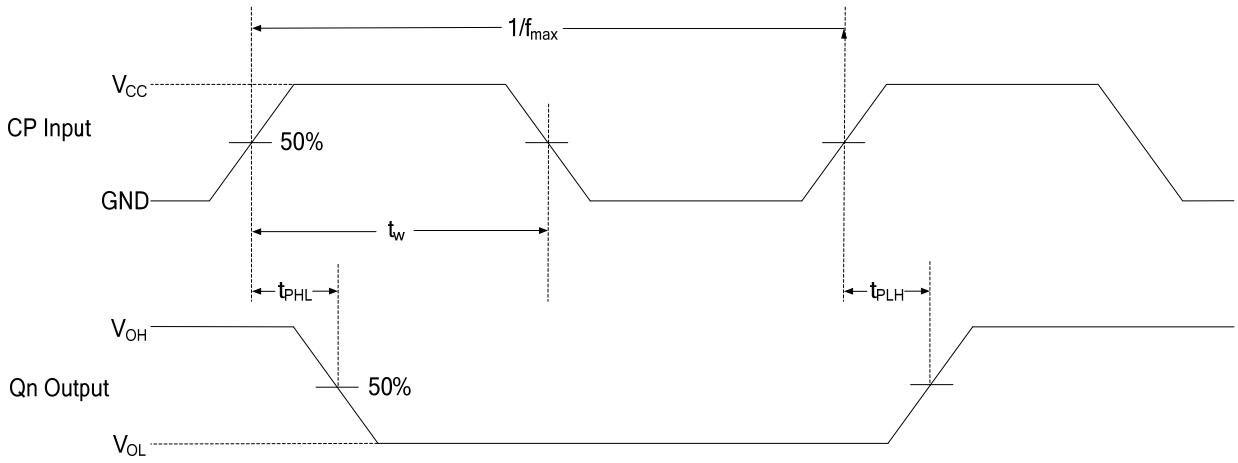
■ TEST CIRCUIT AND WAVEFORMS



LOAD CIRCUITRY FOR MEASURING SWITCHING TIMES



DATA SET-UP AND HOLD TIMES



CLOCK PULSE WIDTH, MAXIMUM FREQUENCY AND INPUT TO OUTPUT PROPAGATION DELAYS