

AN5342K

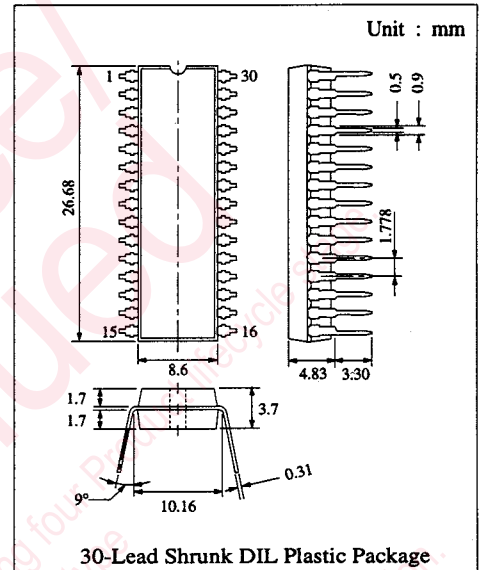
Video Aperture Compensation Circuit for Colour TV

■ Description

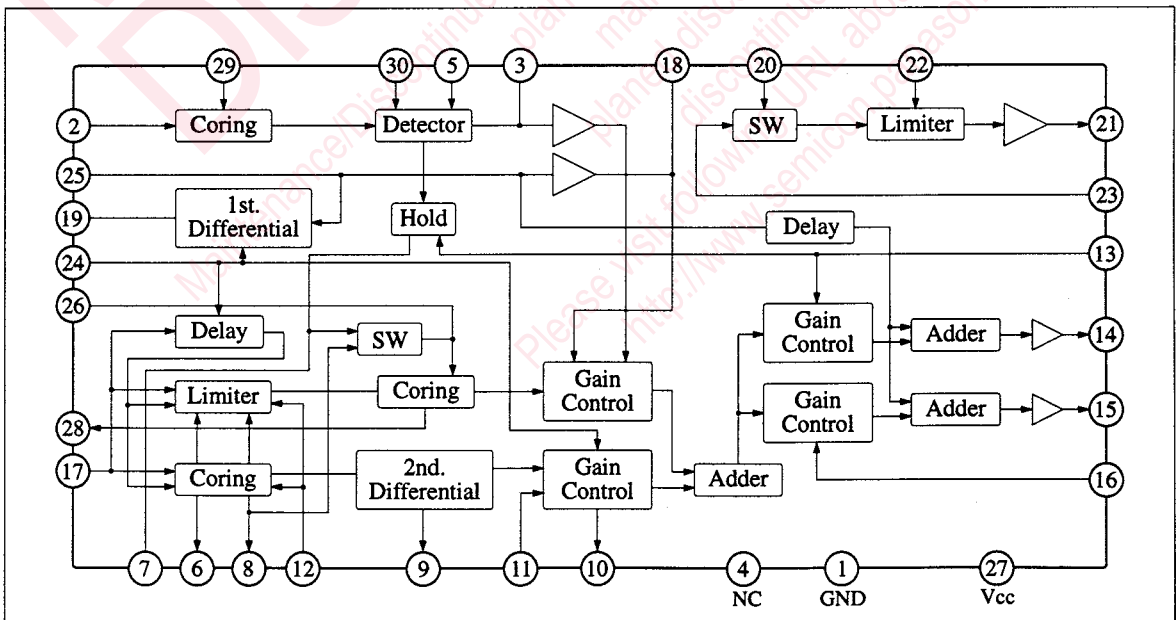
The AN5342K is an integrated circuit designed for TV's video aperture compensation. It corresponds to higher resolution TV image.

■ Features

- Built-in aperture compensation delay circuit
- Dynamic sharpness control function (brightness detection type) which contributes to compensate the detailed contours and creating a more profound, higher resolution image
- Noise elimination function using the coring circuit
- Coring level adjustment function.
- Built-in the amplification circuit for VM (Velocity Modulation)



■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	11	V
Supply Current	Icc	90	mA
Power Dissipation (Ta=70°C)	Pd	990	mW
Operating Ambient Temperature	Topr	-20 ~ +70	°C
Storage Temperature	Tstg	-55 ~ +150	°C

■ Recommended Operating Range (Ta=25°C)

Item	Symbol	Range
Operating Supply Voltage Range	Vcc	8.1V ~ 10.8V

■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Delaying Part						
Y-signal delay time	tDL(Y)	Delay time of Y-sig. IN/OUT at DL=100ns.	188	235	282	nsec
Y-signal frequency characteristics (1)	ef(Y1)	f=10MHz/f=1MHz at DL=100ns.	-6	-4		dB
Y-signal frequency characteristics (2)	ef(Y2)	f=10MHz/f=1MHz at DL=65ns.	-6	-3		dB
Primary differential signal delay time	tDL	DL=100ns.	80	100	120	nsec
Primary differential signal delay time variation	ΔtDL	Difference at delay time shifting	28	35	42	nsec
Aperture Part						
Video aperture compensation max. gain	A _{V(L)}	Output at f=2MHz and Vin=0.5Vp-p	0.7	0.9	1.3	Vp-p
Video aperture compensation coring characteristics (1)	e _{CO(L1)}	Output amplitude at f=4MHz, Vin=75mVp-p and V12=1V	100	130	160	mVp-p
Video aperture compensation coring characteristics (2)	e _{CO(L2)}	Output amplitude at f=4MHz, Vin=75mVp-p and V12=5V		25	50	mVp-p
Video aperture compensation secondary gain ratio	ΔA _{V'(L)}	f=4MHz/f=2MHz at V12=1V, Vin=0.5Vp-p	-6	-4	-2	dB
Coring Part						
Coring compensation signal max. gain	A _{V(S)}	Input/output ratio at f=4MHz, Vin=50mVp-p	16	18	21	dB
Coring compensation signal gain control (typ)	ΔA _{V(S)}	Output ratio at f=4MHz, Vin=50mVp-p, V3=5V→3V	-8.5	-6	-3.5	dB
Coring compensation signal coring characteristics	e _{CO(S)}	Output ratio at f=4MHz, Vin=50mVp-p, V26=5V→3V	-7	-4	-2	dB
Coring compensation signal limiter characteristics	Δe _{LT(S)}	Output ratio at f=4MHz, Vin=100mVp-p, V12=5V→3V		-5	-3	dB
Coring compensation signal sharpness control	ΔA _{V'(S)}	Output ratio at f=4MHz, Vin=50mVp-p, V16=5V→3V		-7	-4	dB
DSC Part						
DSC output voltage (1)	V _{LIM(DSC)}	Output DC at f=4MHz, Vin=27mVp-p	2	3	4	V
DSC output voltage (2)	V _{S(DSC)}	Output DC at f=4MHz, Vin=150mVp-p	7.5	8.8		V
DSC output voltage (3)	V _{L(DSC)}	Output DC at f=4MHz, Vin=840mVp-p		0.2	1.0	V
Noise reduction characteristics	V _{NR}	Bias voltage in pin (26) at f=4MHz, Vin=150mVp-p		0.2	1.0	V
VM Part						
VM signal max. gain	A _{V(VM)}	Output amplitude at f=4MHz, Vin=100mVp-p	0.6	0.9	1.4	Vp-p
VM signal limiter characteristics	ΔA _{V(VM)}	Output ratio at f=4MHz, Vin=100mVp-p, V22=5V→3V	2.5	4.0	5.5	dB
VM signal YS operating characteristics	e _{off(VM)}	Output ratio at f=4MHz, Vin=100mVp-p, V20=0V→2V		-40	-25	dB

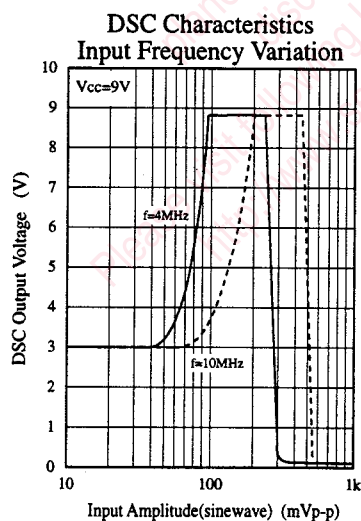
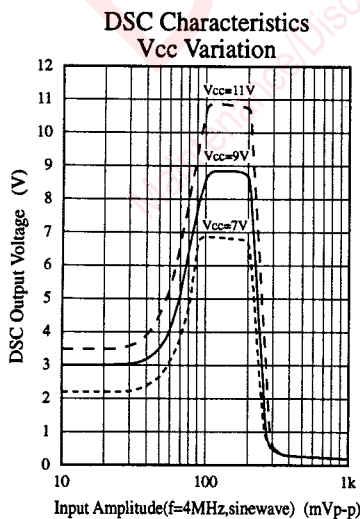
■ Electrical Characteristics Design Reference Values (Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Y-signal delay time variation	$\Delta t_{DL(Y)}$	Difference of delay time at delay time shifting		35		nsec
Primary differential signal pulse width (1)	$\Delta t_{(DL_1)}$	Pulse width (DL=100ns.) at 125ns. rising pulse input		190		nsec
Primary differential signal pulse width (2)	$\Delta t_{(DL_2)}$	Pulse width (DL=65ns.) at 125ns. rising pulse input		225		nsec
Primary differential signal output amplitude (1)	$A_{V(DL_1)}$	Output amplitude (DL=100ns.) at 125ns. rising pulse input		0.9		Vp-p
Primary differential signal output amplitude (2)	$A_{V(DL_2)}$	Output amplitude (DL=65ns.) at 125ns. rising pulse input		0.8		Vp-p
Aperture compensation signal, gain at delay time shifting	$\Delta A_{V(L)}$	Output ratio at f=2MHz, in=0.5Vp-p V24=0V→3V		-3		dB

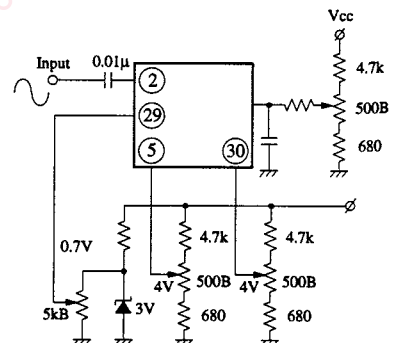
■ Pin Descriptions

Pin No.	Pin Name	Pin No.	Pin Name
1	GND	16	Sharpness Control
2	DSC Input	17	Prior-correction Primary Differential Input
3	DSC Detection Output	18	Luminance Detecting
4	NC	19	Prior-correction Primary Differential Output
5	DSC Major Signal Gain Control	20	YS-Input
6	Differential Signal Bias 1	21	VM Output
7	Noise Reduction Bias	22	VM Limiter Control
8	Differential Signal Bias 2	23	VM Input
9	Post-correction Primary Differential Output	24	Delay Time Shifting
10	Aperture Part Bias	25	Y Input
11	Secondary Differential Input	26	Coring Part Coring Control
12	Aperture Part/Coring Part Separation Level Control	27	Vcc
13	VM Peaking Control	28	Coring Bias
14	VM Y-Output	29	DSC Bias
15	Y-Output	30	DSC Minor Signal Gain Control

■ Characteristics Curve Diagram

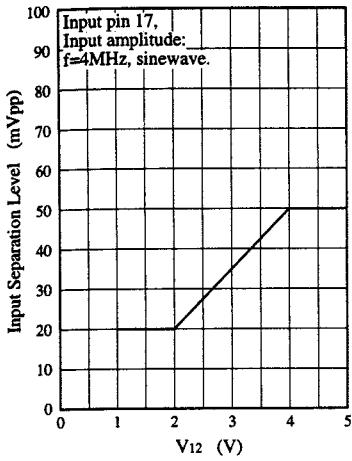


DSC Characteristics Circuit

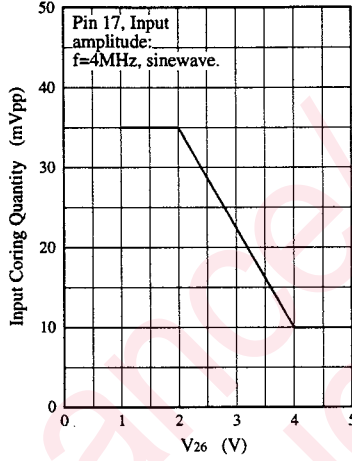


■ Characteristics Curve Diagram (Continue)

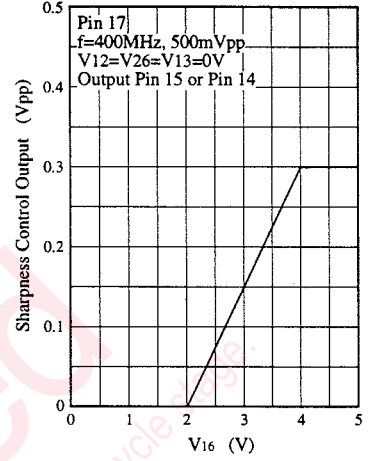
Separation Level Characteristics



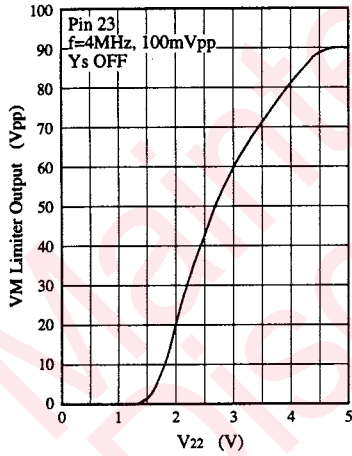
Coring Part Coring Characteristics



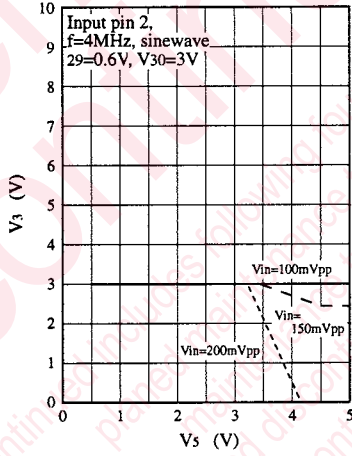
Sharpness Control Characteristics



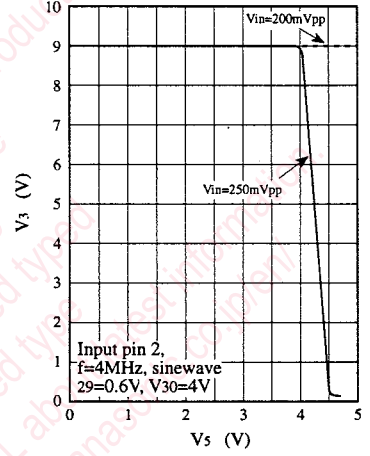
VM Limiter Control Characteristics



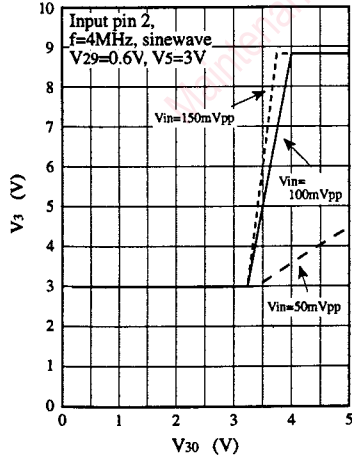
DSC Major Signal Gain Control Characteristics (1)



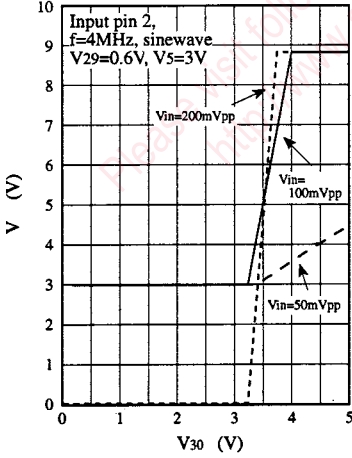
DSC Major Signal Gain Control Characteristics (2)



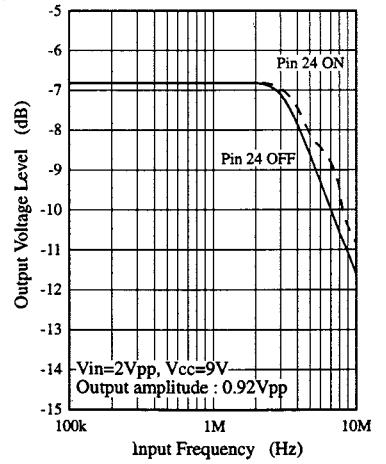
DSC Minor Signal Gain Control Characteristics (1)



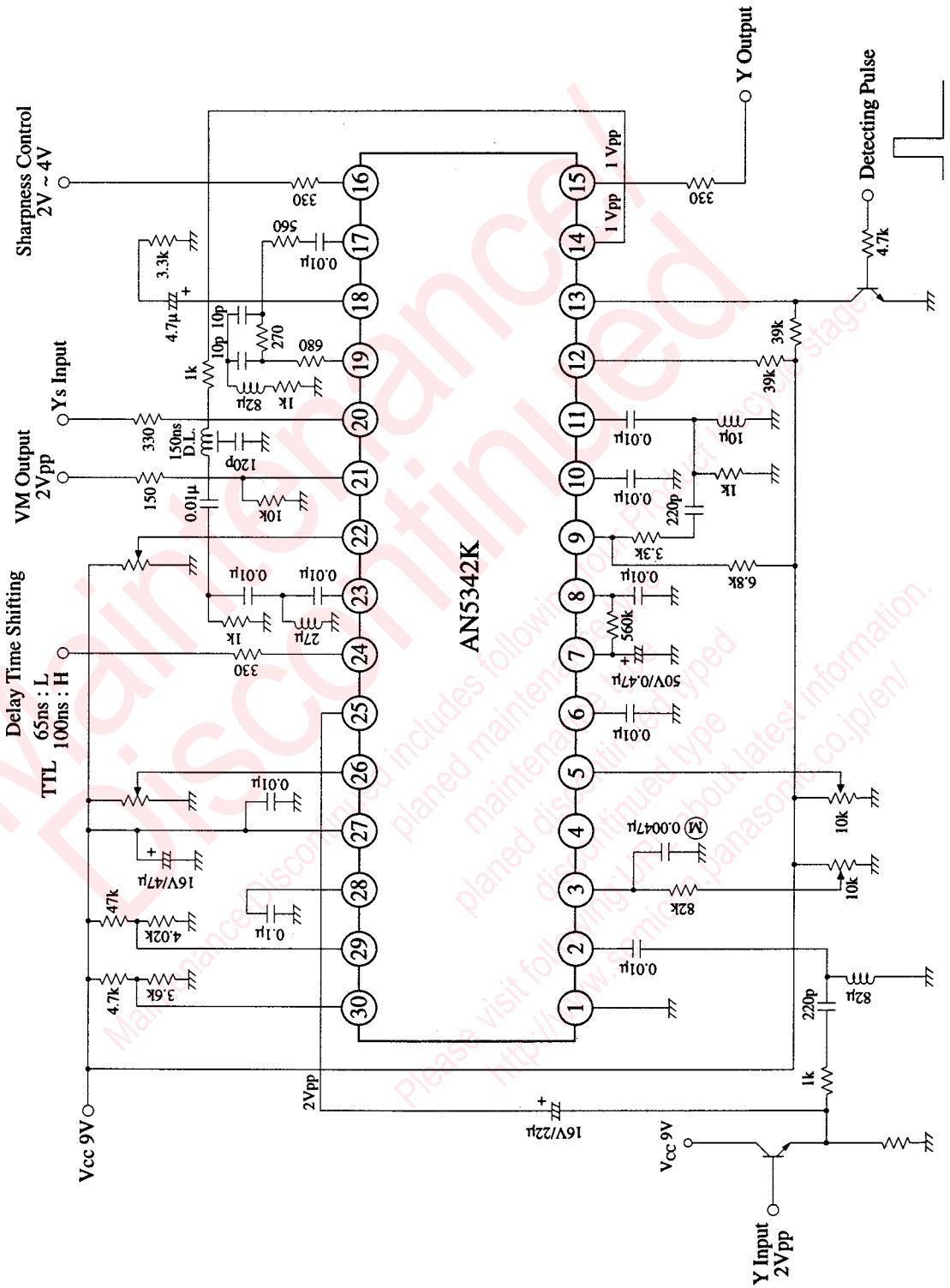
DSC Minor Signal Gain Control Characteristics (2)




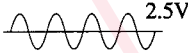
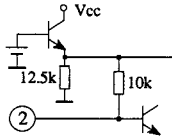
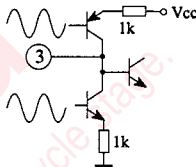
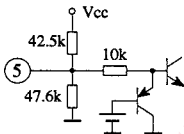
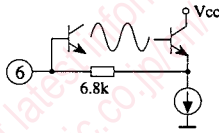
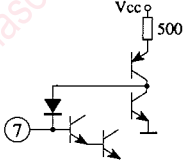
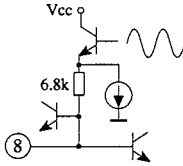
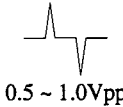
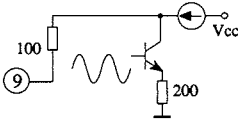
f Characteristics



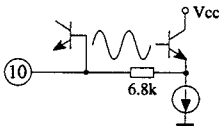
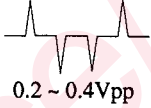
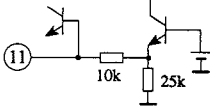
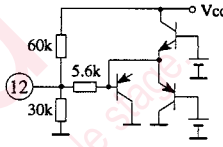
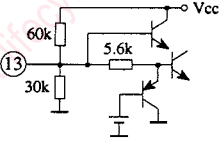
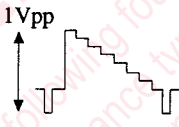
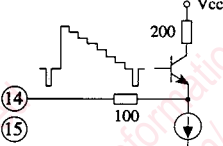
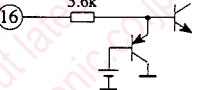
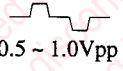
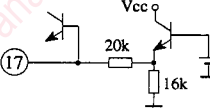

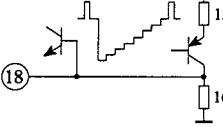
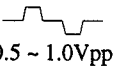
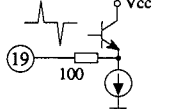
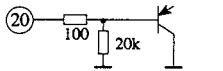
■ Application Circuit



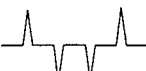
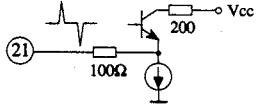
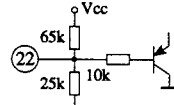

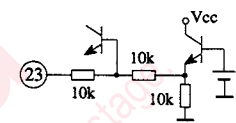
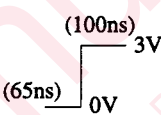
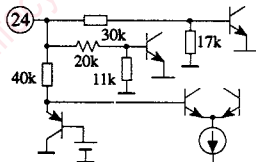

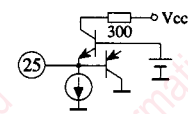
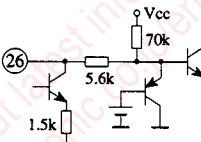
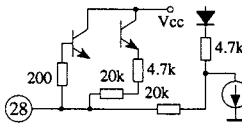
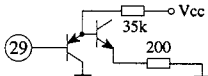
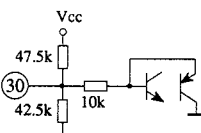
■ Pin Descriptions

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
1	GND	GND Pin		
2	DSC IN	Input Pin to DSC (Dynamic Sharpness Control) circuit. The high frequency signal is passed through high-pass filter is input.		
3	DSC OUT	Detection Output Pin of DSC Circuit. The detection current is output according to the amplitude of input signal. It is smoothed to the DC with an external C. R. The gain of detail signal is dynamically controlled by this detection voltage	DC detection output (0 ~ 9V)	
4	N.C.	No connection		
5	DSC L-Gain Control	Gain control pin for large amplitude signal of the DSC circuit. When voltage is raised, gain is increased and operates to step down the detection output voltage of Pin 3	DC variable range (0 ~ 5V)	
6	Bias 1	Bias pin of the 1st differential signal. A capacitor connected makes the signal smooth and generates DC bias	DC (3.2V)	
7	Y-signal Noise Reduction YNR	Noise detection pin of the Y-signal. The noise at V-pulse period is detected and held to a capacitor connected. YNR is turned ON/OFF when combining this pin with pin 8	DC	
8	Bias 2	Bias pin of the 1st-differential signal. A capacitor connected makes the signal smooth and generates DC bias. YNR is turned ON/OFF when combining this pin with Pin 7	DC (2.4V)	
9	Signal Out for 2nd-Diff.	Output pin of the aperture signal. It is used for generating a 2nd-differential signal		

■ Pin Descriptions (Continue)

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
10	Bias 3	Bias pin of the aperture signal. A capacitor connected makes the signal smooth and generates DC bias	DC (3.5V)	
11	2nd-Diff. Signal In	Input pin of the 2nd-differential signal	 0.2 ~ 0.4Vpp	
12	Separation Control	Controlling the level to separate large amplitude (aperture and small amplitude (detail) by the amplitude of the 1st-differential signal	DC variable range (0 ~ 5V)	
13	VM Peaking Control	Sharpness Control Pin of Y output for VM. When voltage is raised, the correction quantity is increased. It is a V-pulse input pin. The noise is detected at low pulse	DC	
14	Y out (VM)	Y-signal output pin. Connect to the Y-input of Video Chroma IC. (Pin 15) Signal output for VM is provided separately (Pin 14)	 1Vpp	
15	Y out			
16	Sharpness Control	Sharpness control pin of Y out (Pin 15). When voltage is raised, the correction quantity is increased	DC variable range (0 ~ 5V)	
17	1st-Diff. Signal In	Input pin of the 1st-differential signal	 0.5 ~ 1.0Vpp	
18	APL Det	Detection pin of the Y signal level		
19	1st-Diff. Signal out	Output pin of the 1st-differential signal. It is provided by the internal delay circuit	 0.5 ~ 1.0Vpp	
20	Test	Test pin for the VM circuit inspection. Earth it ordinally	Earth	

Pin Descriptions (Continue)

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
21	VM out	VM output pin	 0.2 ~ 0.4Vpp	
22	VM-Limiter Control	Limiter control pin of the VM output. When the voltage is raised, the limiter is gradually released.	DC variable range (0 ~ 5V)	
23	VM In	Input pin to the Amp. for VM. High freq. signal which is passed through the HPF is input from Yout (Pin 14) by way of DL. DL is to correct the time which is delayed at Video Chroma IC.	 0.5 ~ 1.0Vpp	
24	Delay time SW	Switch the delay time of the delay circuit in the IC. The pulse width of the 1st-Dif. signal (Pin 19) is changed and at the same time, the delay time of Y-signal is switched.	 (100ns) 3V (65ns) 0V	
25	Y In	Input pin of Y-signal. Input Y-signal after Y/C separation. Sync-top peak is clamped.	 2Vpp	
26	Small-Signal Coring Control	Controlling the coring level of detail signal (small amplitude signal). When the voltage is raised, coring is gradually released. At YNR ON, the voltage drops and coring operates.	DC variable range (0 ~ 5V)	
27	Vcc	Power Supply Pin	DC 9V	
28	Small Signal Coring Bias	Bias pin for coring of the detail signal (small amplitude signal). A capacitor connected makes the signal smoothed and biased.	DC 5.6V	
29	DSC-Bias	Bias pin of the DSC circuit. Bias it between 0.5V and 0.8V.	DC 0.7V	
30	DSC S-Gain Control	Gain control pin for the small amplitude sig. of the DSC cct. When the voltage is raised, gain is increased so that it operates to increase the det. output voltage of Pin 3. Gain distribution is decided by combining this pin with L-Gain of Pin 5.	DC variable range (0 ~ 5V)	

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- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
 - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
- (7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.