2N6788

File Number **1593**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

6.0A, 100V

$r_{DS}(on)$ = 0.30 Ω

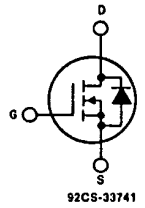
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

N-CHANNEL ENHANCEMENT MODE



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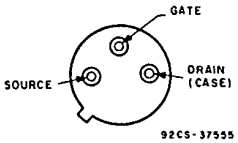
TERMINAL DIAGRAM

TERMINAL DESIGNATION



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JEDEC TO-205AF

Absolute Maximum Ratings

Parameter		2N6788	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5*	A
I_{DM}	Pulsed Drain Current ③	24*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	6.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	24*	A
P_D @ T_C = 25°C	Max. Power Dissipation	20* (See Fig. 14)	W
	Linear Derating Factor	0.16* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 24	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

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Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	µA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	µA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		–	–	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	–	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.6*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 36V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, di_F/dt = 100A/µs
Q_{RR}	Reverse Recovered Charge	1.2	µC	T_J = 150°C, I_F = 6.0A, di_F/dt = 100A/µs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

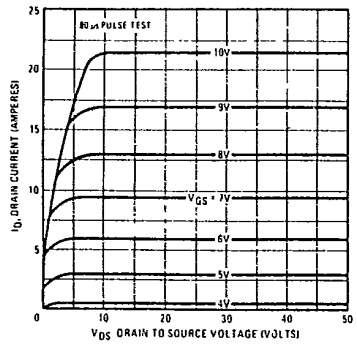

Fig. 1 – Typical Output Characteristics

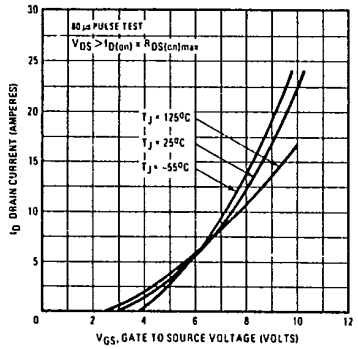

Fig. 2 – Typical Transfer Characteristics

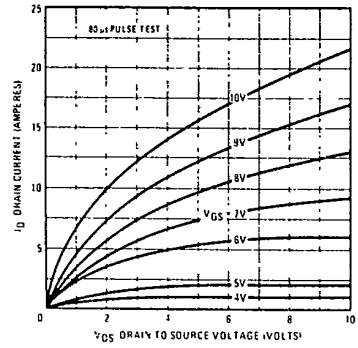

Fig. 3 – Typical Saturation Characteristics

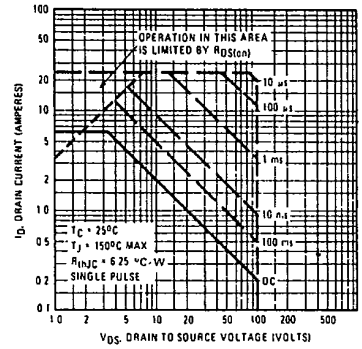

Fig. 4 – Maximum Safe Operating Area

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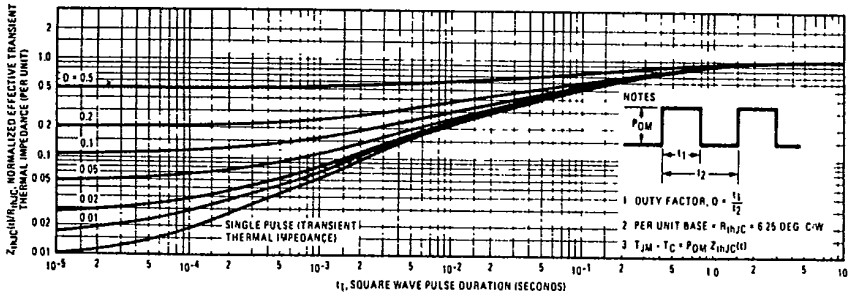

Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

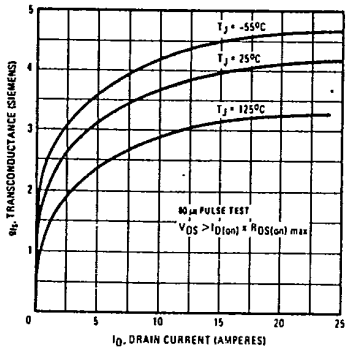

Fig. 6 – Typical Transconductance Vs. Drain Current

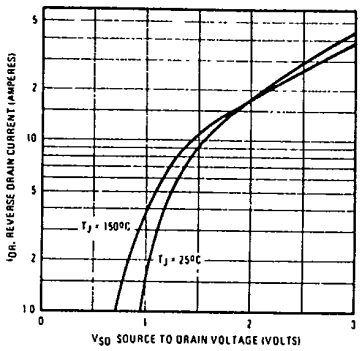

Fig. 7 – Typical Source-Drain Diode Forward Voltage

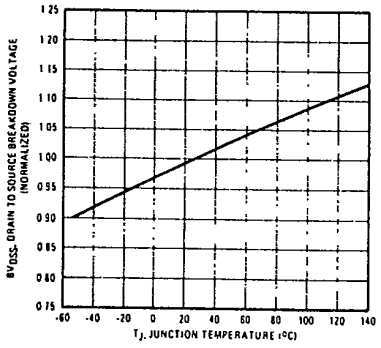

Fig. 8 – Breakdown Voltage Vs. Temperature

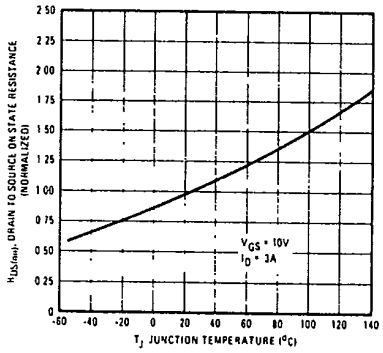

Fig. 9 – Normalized On-Resistance Vs. Temperature

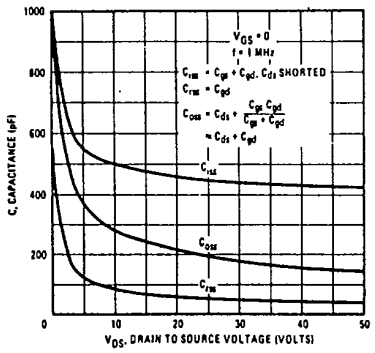

Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

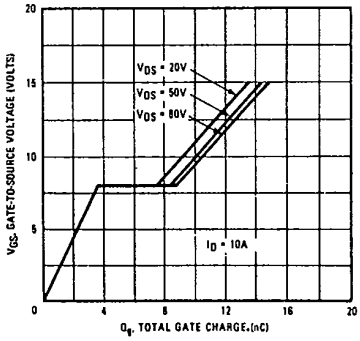

Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

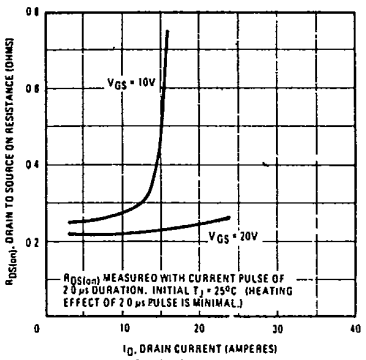

Fig. 12 – Typical On-Resistance Vs. Drain Current

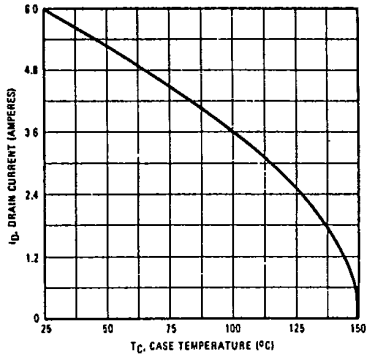

Fig. 13 – Maximum Drain Current Vs. Case Temperature

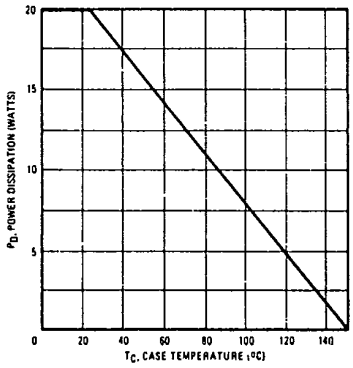

Fig. 14 – Power Vs. Temperature Derating Curve

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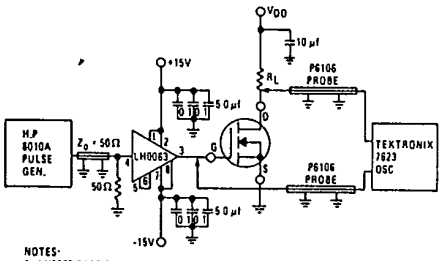
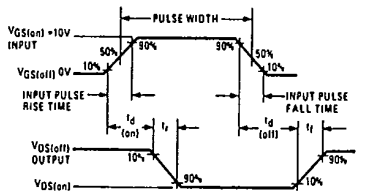
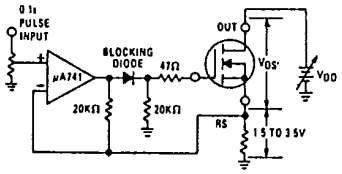


NOTES:
1. LH0063 CASE GROUNDED
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT

Fig. 15 – Switching Time Test Circuit



NOTES
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C
2. SELECT R_S SUCH THAT $I_D = R_S = 2.5 \pm 1.0$ Vdc

Fig. 16 – Safe Operating Area Test Circuit