NEC Electronics Inc.

μPB100474A
1,024 x 4-Bit 100K ECL RAM

T-46-23-08

Description

The μPB100474A is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open emitter outputs and full voltage and temperature compensation. The device is packaged in a 24-pin cerdip or ceramic flatpack.

Features

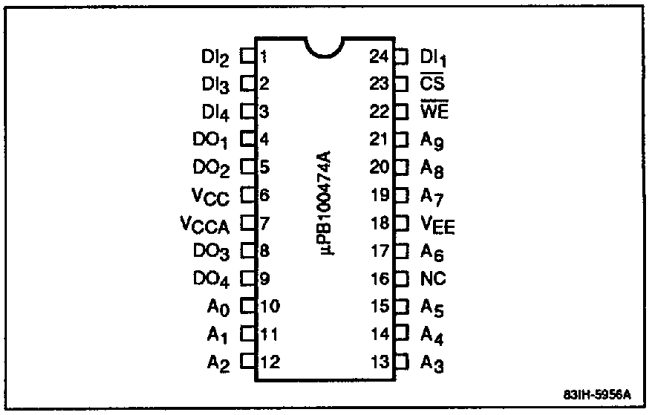
- 1,024 word by 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times
- 24-pin cerdip and flatpack packaging

Ordering Information

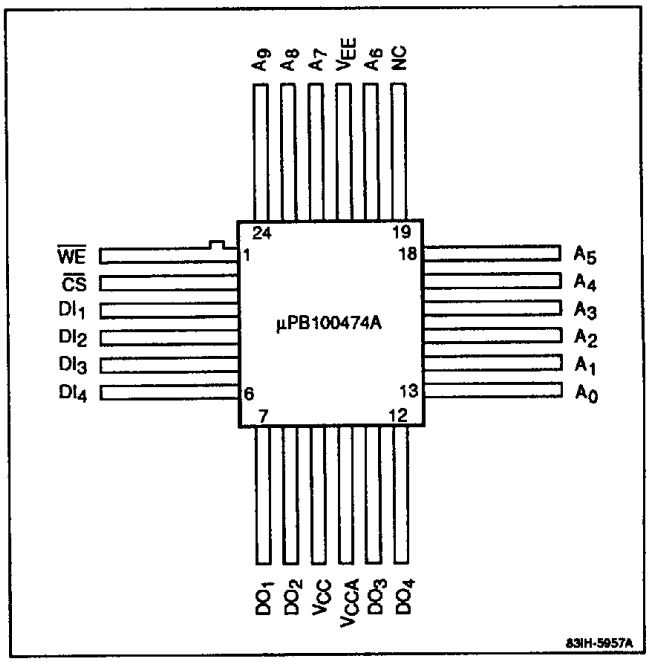
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474AD-5	5 ns	–250 mA	24-pin cerdip
AD-6	6 ns		
μPB100474ABH-5	5 ns	–250 mA	24-pin ceramic flatpack
ABH-6	6 ns		

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



26d

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Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		4		pF
Output capacitance	C_O		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

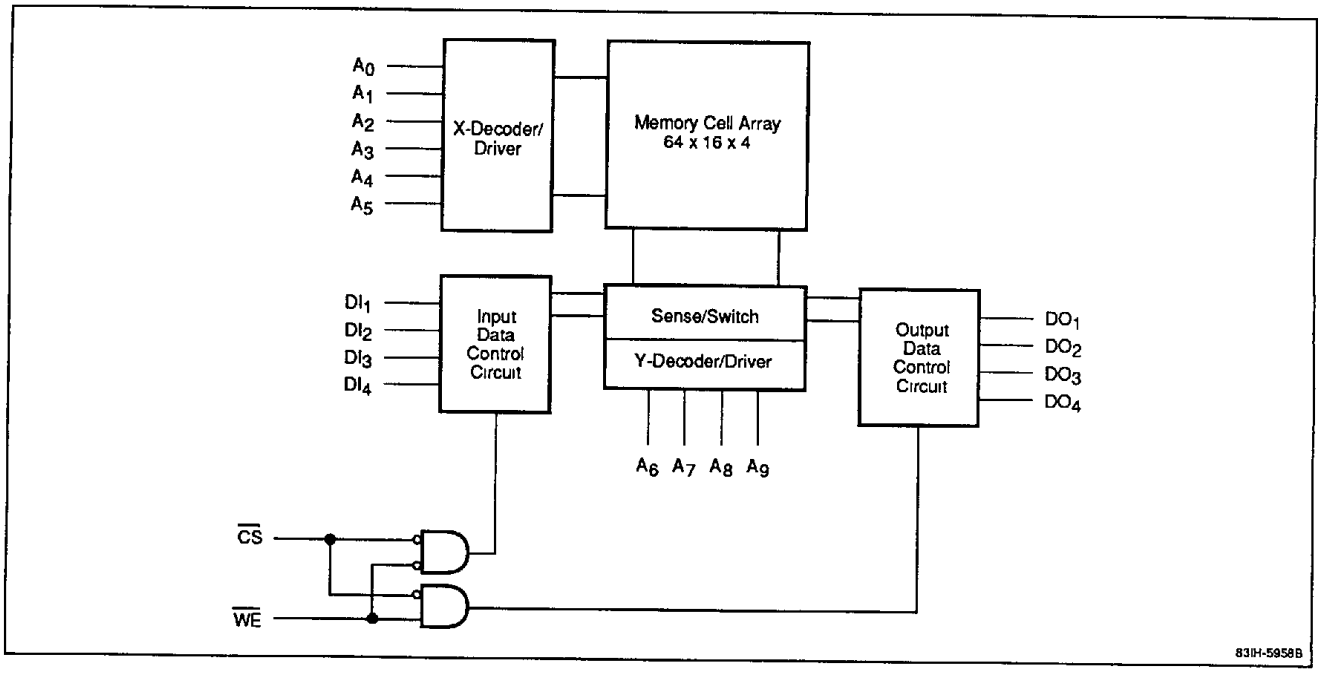
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{IN}	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−250			mA	All inputs and outputs open

26d

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100474A-5			μPB100474A-6				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			6	ns	
Chip select access time	t_{ACS}			3			4	ns	
Chip select recovery time	t_{RCS}			3			4	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	1			1			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	1			1			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	1			1			ns	
Write disable time	t_{WS}			3			4	ns	
Write recovery time	t_{WR}			6			7	ns	
Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

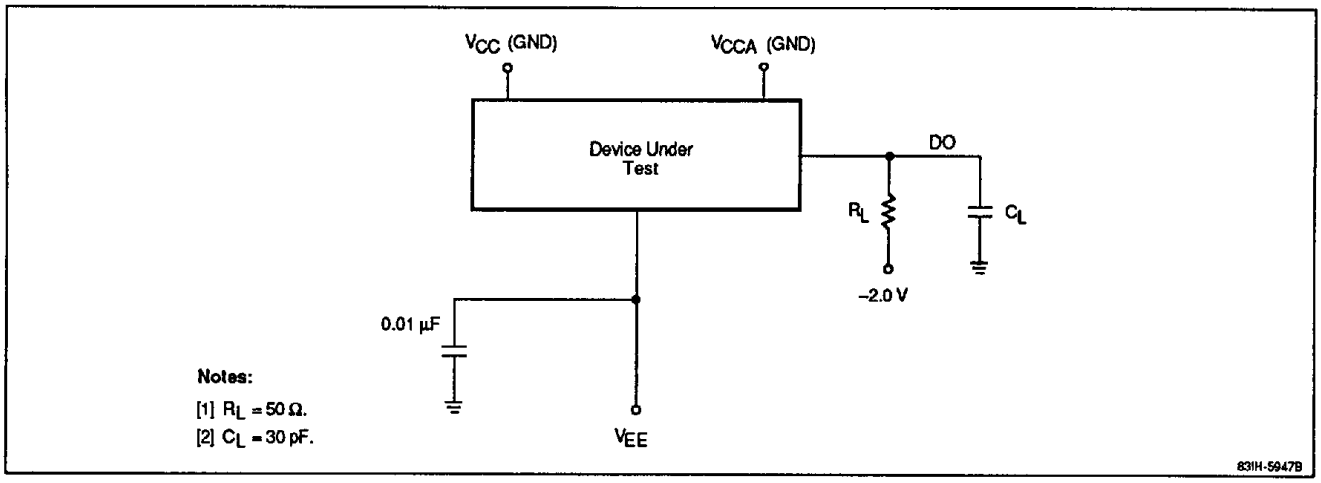
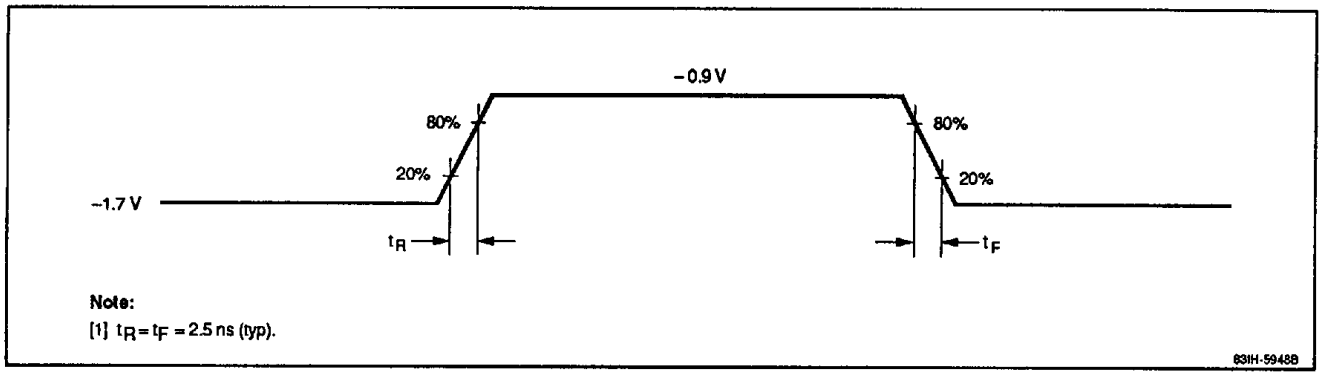
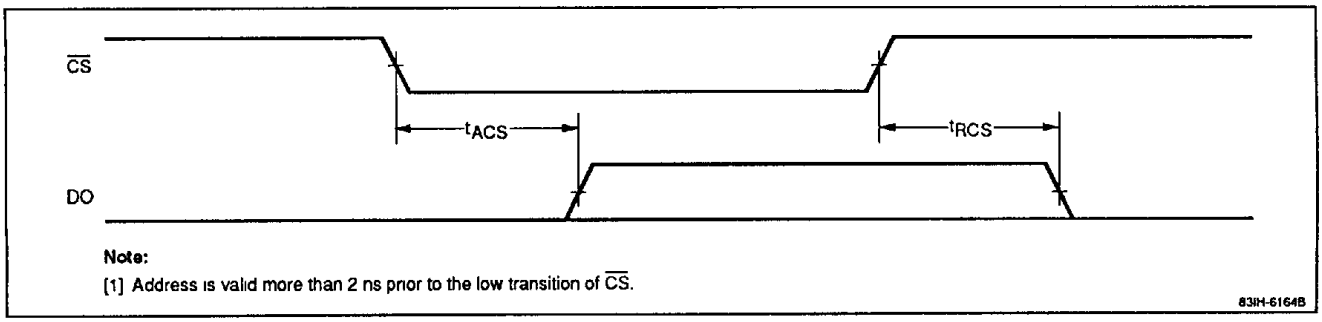


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

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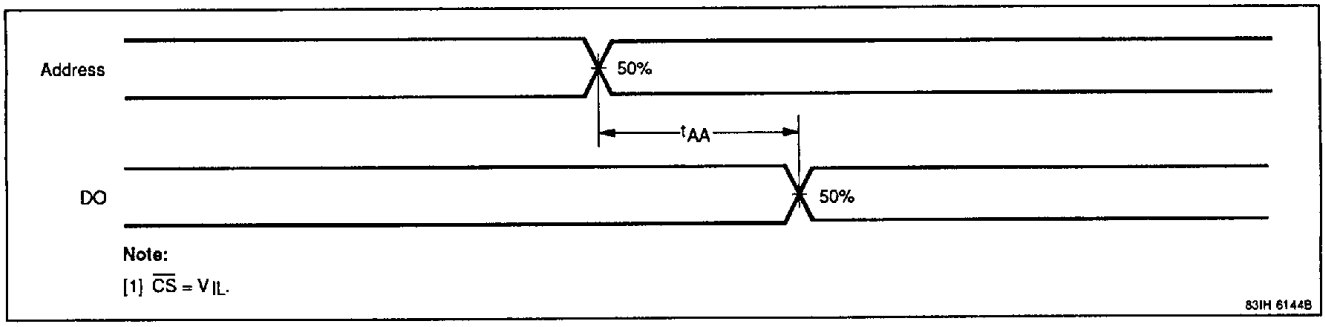
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

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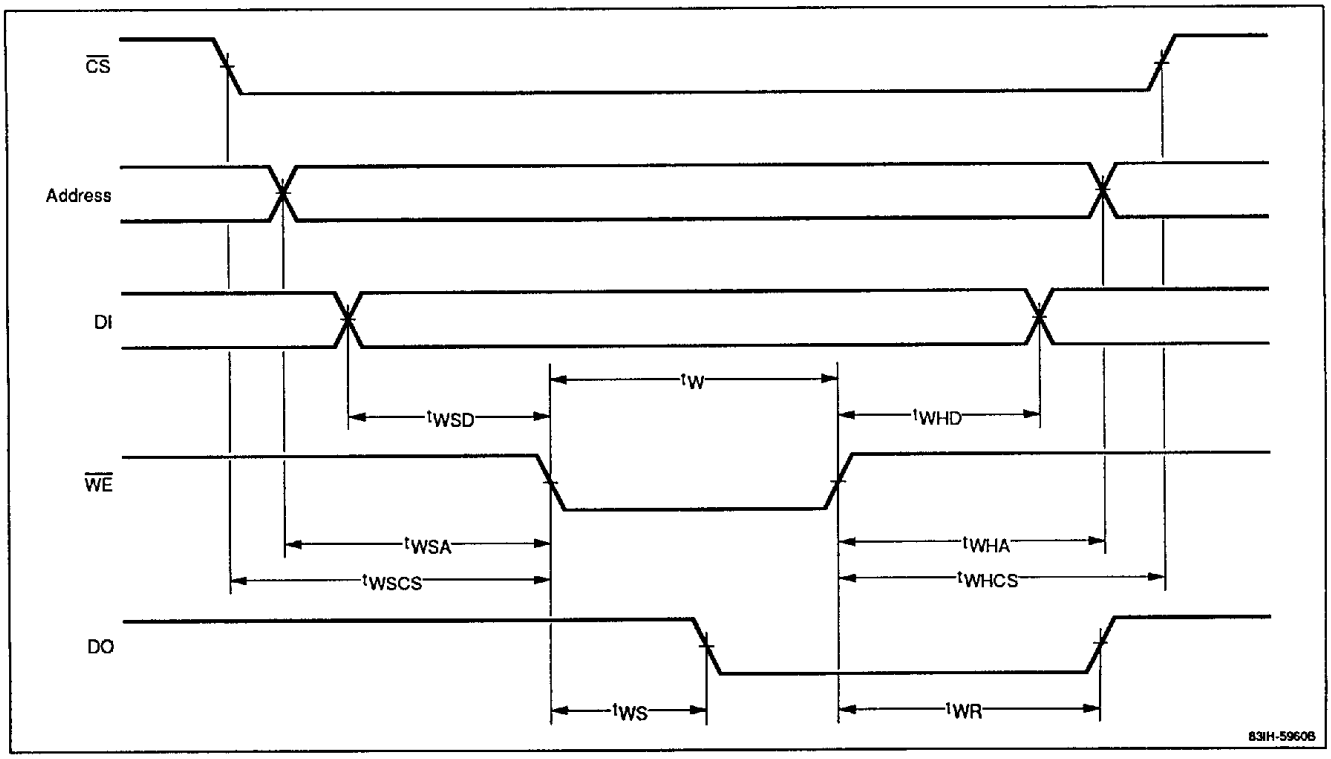
Write Cycle



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