SPT5100

8-BIT, 20 MWPS DUAL CHANNEL VIDEO DAC

FEATURES

- 8-Bit Dual Channel Video Digital-to-Analog Converter
- 20 MWPS Operation
- Low Power: 70 mW
- Internal Voltage Reference
- 5 V Monolithic CMOS
- 32-Lead QFP Package (7 mm by 7 mm, 0.8 mm Pitch)

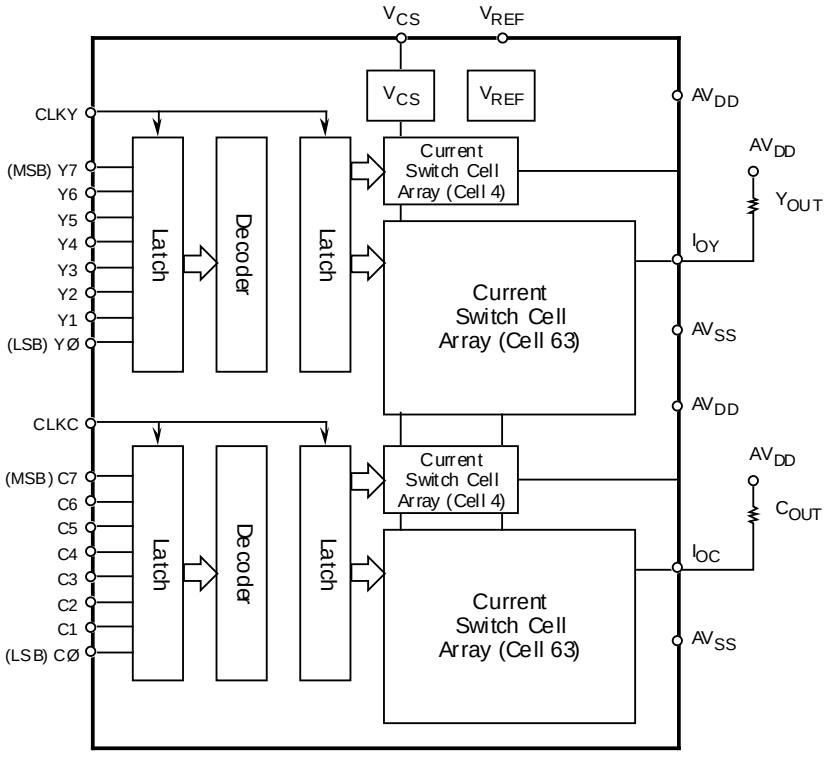
APPLICATIONS

- High-speed Digital-to-Analog Conversion
- Y/ C, S-Video Processing
- Desktop Video Processing
- Digital TV
- Satellite TV Decoders
- Digital VCRs

GENERAL DESCRIPTION

The SPT5100 is an 8-bit, 20 MWPS, dual channel video digital-to-analog converter specifically designed for video processing applications including digital TV decoders and digital VCRs. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of ±0.5 LSB over the full temperature range. The device is available in a 32-lead QFP package in the commercial temperature range.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
AV_{DD} (measured to AV_{SS}) ..... -0.3 to 7.0 V

Input Voltage
Clock and Data ..... AV_{SS} to AV_{DD}

Output Current
I_{OUT} ..... 0 to 8 mA

Temperature
Operating, ambient ..... 0 to +70 °C
Storage ..... -55 to + 125 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

f_{CLK} = 20 MWPS, AV_{DD} = 5.0 V, Output Pull-Up Load = 240 Ω, T_A = 25 °C, AV_{SS} = 0.0 V

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				8.0		Bits
Differential Linearity	$T_A = T_{MIN}$ to T_{MAX}	I		±0.25	±0.5	LSB
Integral Linearity		I		±0.5	±1.0	LSB
Analog Outputs						
Output Voltage Range	V_{CS} = +1.25 V	I	4.0		5.0	V
Conversion Rate		I	20			MWPS
Output Offset Voltage		I		14	25	mV
Signal-to-Noise Ratio		I	41	45		dB
Differential Phase		V		1.2		Degrees
Differential Gain		V		2		%
Glitch Energy		V		80		pV-s
Settling Time		I	31	26		ns
Propagation Delay (t_{pd})		V		10	12	ns
Crosstalk		I	-47			dB
FS Control Voltage (V_{CS})		IV	1.0		1.4	V
Digital Inputs and Timing						
Input Current, Logic High	V_{IH} = 5 V	I			5	µA
Logic Low	V_{IL} = 0 V	I	-5			µA
Set-Up Time, Data and Controls (t_S)		I	5			ns
Hold Time, Data and Controls (t_h)		I	10			ns
Clock Pulse Width (Low)		I	25			ns
Clock Pulse Width (High)		I	25			ns
Power Supply Requirements						
Supply Voltage		I	4.75		5.25	V
Supply Current		I			14	mA
Power Dissipation		I			70	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

INTERFACE CONSIDERATIONS

Figure 1 shows a typical interface circuit of the SPT5100 in normal circuit operation.

SUPPLY AND GROUND CONSIDERATIONS

SPT suggests that all power supply pins (AV_{DD}) be tied together and decoupled using a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

INTERNAL REFERENCE VOLTAGE (V_{REF})

Voltage reference is internally generated. Connect a 0.1 µF bypass capacitor as close to the pin as possible.

FULL-SCALE ADJUST CONTROL (V_{CS})

Connect a 0.1 µF bypass capacitor with the shortest possible lead length between V_{CS} and AV_{SS}. A resistor connected between this pin and AV_{DD} controls the magnitude of the full-scale video signal.

The output voltage range of the SPT5100 can be kept constant and stable by keeping the value of V_{CS} to ground constant. The full-scale voltage changes according to V_{CS}. (See figure 2.)

CURRENT OUTPUTS

The Y channel and C channel current outputs should have a load resistor connected to AV_{DD}. The resistors are typically 240 Ω and should be kept in the 150 Ω to 250 Ω range.

LATCH-UP CONSIDERATIONS

In order to prevent a possible latch-up condition, SPT suggests that a 100 Ω resistor be placed in series with each clock input pin.

Table I - Binary Codes
1 LSB = 3.91 mV, V_{CS} = 1.25 V

Step	Digital Input A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	Analog Out (V)
0	0	0	0	0	0	0	0	0	4.0000
1	0	0	0	0	0	0	0	1	4.0039
2	0	0	0	0	0	0	1	0	4.0078
3	0	0	0	0	0	0	1	1	4.0117
.				.					.
.				.					.
.				.					.
254	1	1	1	1	1	1	1	0	4.9922
255	1	1	1	1	1	1	1	1	4.9961

Figure 1 - Typical Interface Circuit

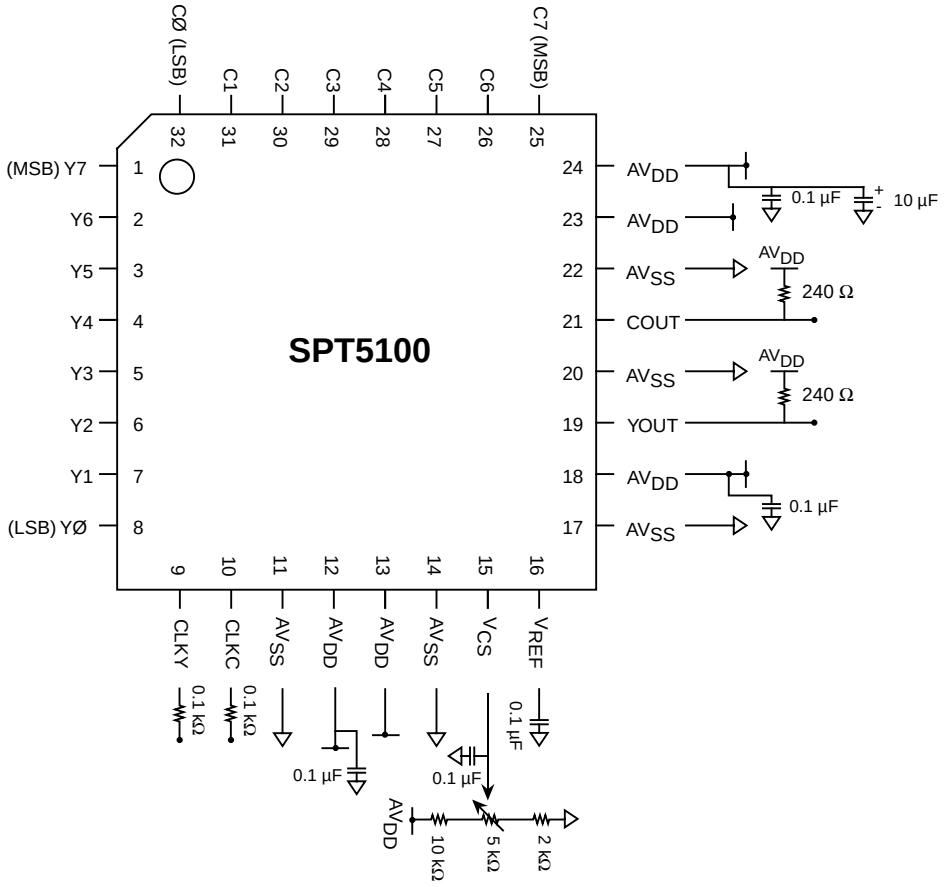


Figure 2 - Typical Performance Characteristics

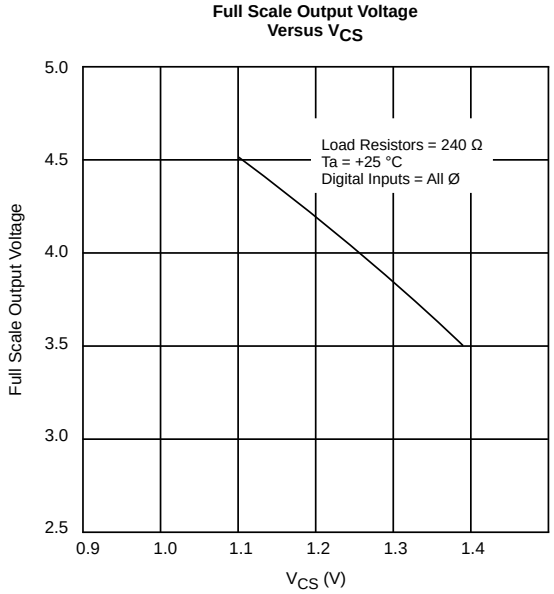
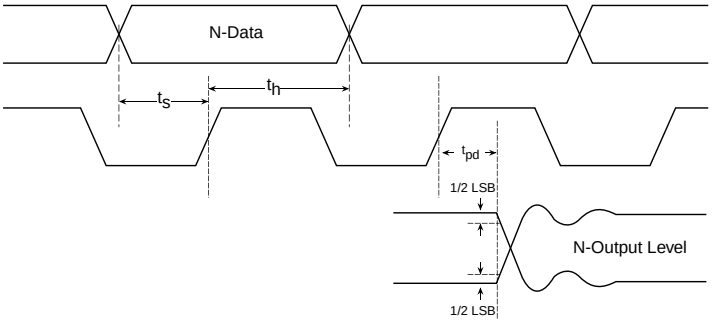
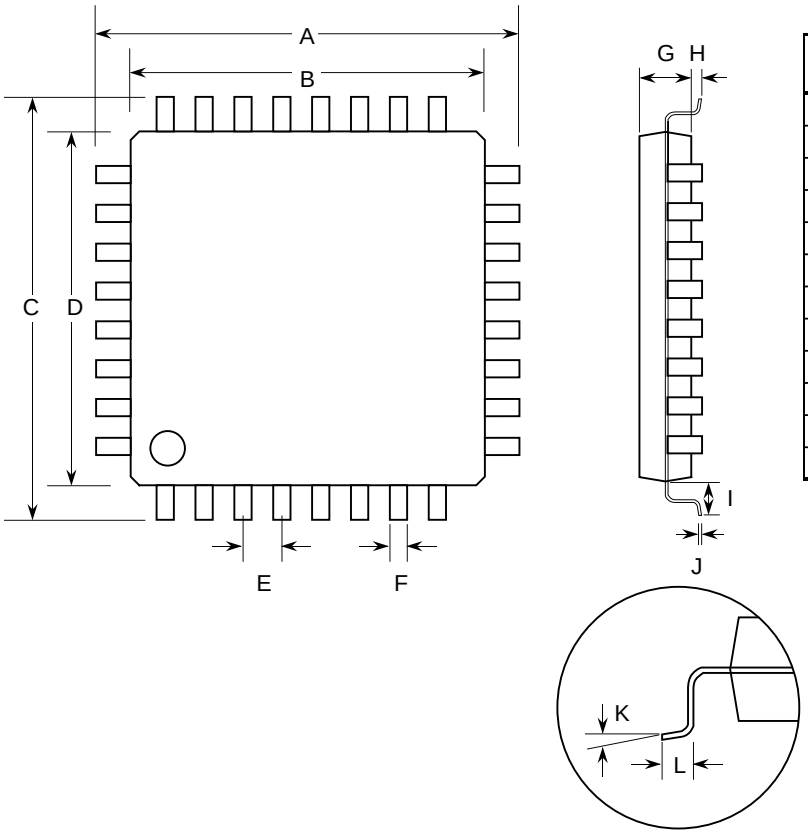


Figure 3 - Timing Diagram



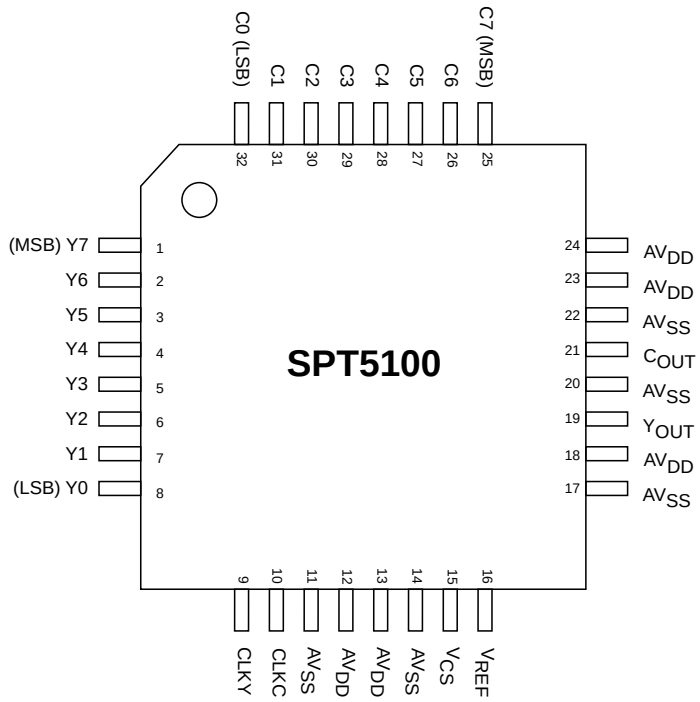
PACKAGE OUTLINE

32-Lead QFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.339	0.363	8.70	9.30
B	0.261	0.285	6.70	7.30
C	0.339	0.363	8.70	9.30
D	0.261	0.285	6.70	7.30
E	0.023	0.039	0.60	1.00
F	0.012	0.020	0.30	0.50
G	0.056	0.057	1.44	1.46
H	0.002	0.006	0.05	0.15
I	0.039 typ		1.00 typ	
J	0.004	0.008	0.09	0.20
K	0°	7°	0°	7°
L	0.016 typ		0.4 typ	

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
C_{OUT}	C Channel Analog Current Output
Y_{OUT}	Y Channel Analog Current Output
C7 - C0	C Channel Data Inputs
Y7 - Y0	Y Channel Data Inputs
CLKY	Y Channel Clock Input
CLKC	C Channel Clock Input
V_{REF}	Voltage Reference (A 0.1 µF ceramic capacitor should be used)
V_{CS}	Full-Scale Adjust Control Voltage 1 to 1.4 V
AV_{SS}	Ground
AV_{DD}	Power Supply Voltage

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5100SCT	0 to +70 °C	32L QFP

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.