





2N7002XFB

#### N-CHANNEL ENHANCEMENT MODE FIELD MOSFET

### **Product Summary**

$V_{(BR)DSS}$	R <sub>DS(ON)</sub>	I <sub>D</sub> T <sub>A</sub> = 25°C
001/	$3.0\Omega @ V_{GS} = 10V$	400mA
60V	4.0Ω @ V <sub>GS</sub> = 5V	330mA

### **Description and Applications**

These N-Channel enhancement mode field effect transistors are produced using DIODES proprietary, high density, uses advanced trench technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small

Load switching

## **Features and Benefits**

- N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package
- ESD Protected Gate, 1.2kV HBM
- Lead, Halogen and Antimony Free, RoHS Compliant
- "Green" Device (Notes 1 and 2)
- Qualified to AEC-Q101 Standards for High Reliability

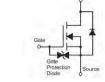
#### **Mechanical Data**

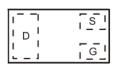
- Case: DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (approximate)

#### DFN1006-3









Top View

Equivalent Circuit

Top View

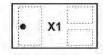
### **Ordering Information** (Note 3)

ı	Part Number	Case	Packaging
	2N7002XFB-7	DFN1006-3	3000/Tape & Reel

Notes:

- 1. No purposefully added lead. Halogen and Antimony Free.
- 2. Product manufactured with Data Code V9 (week 33, 2008) and newer are built with Green Molding Compound. Product manufactured prior to Date Code V9 are built with Non-Green Molding Compound and may contain Halogens or Sb203 Fire Retardants.
- 3. For packaging details, go to our website at http://www.diodes.com

# **Marking Information**



Top View Dot Denotes Drain Side X1 = Product Type Marking Code

Date Code Key

Date Code Itey												
Year	200	9	2010		2011	20	12	2013		2014	2	2015
Code	W		Х		Υ	7	7	Α		В		С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D





# **Maximum Ratings**

Characteris	tic	Symbol	Value	Units	
Drain-Source Voltage		V <sub>DSS</sub>	60	V	
Gate-Source Voltage		$V_{GSS}$	±20	V	
Continuous Drain Current (Note 4) V <sub>GS</sub> = 10V	Steady State	$T_A = 25$ °C $T_A = 70$ °C	I <sub>D</sub>	260 210	mA
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	Steady State	$T_A = 25$ °C $T_A = 70$ °C	I <sub>D</sub>	400 310	mA

### **Thermal Characteristics**

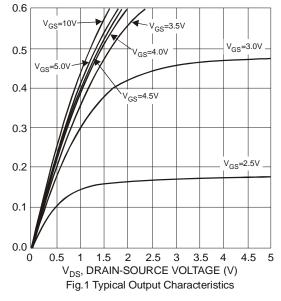
Characteristic	Symbol	Value	Units
Power Dissipation, @T <sub>A</sub> = 25°C (Note 4)	$P_{D}$	430	mW
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = 25°C (Note 4)	$R_{ heta JA}$	290	°C/W
Power Dissipation, @T <sub>A</sub> = 25°C (Note 5)	$P_{D}$	840	mW
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = 25°C (Note 5)	$R_{ heta}$ JSA	147	°C/W
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C

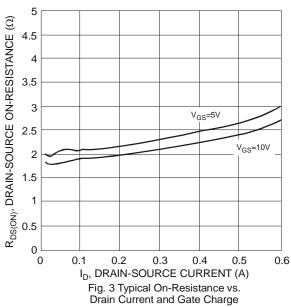
# Electrical Characteristics @TA = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)		•				•
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current T <sub>J</sub> = 25°C	I <sub>DSS</sub>	-	-	0.1	μA	$V_{DS} = 60V, V_{GS} = 0V$
Gate-Body Leakage	I <sub>GSS</sub>	-	-	±10	μA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 6)		_	_			
Gate Threshold Voltage	V <sub>GS(th)</sub>	1.2	-	2.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Static Drain-Source On-Resistance	R <sub>DS (ON)</sub>	-	2.1 2.3	3.0 4.0	Ω	$V_{GS} = 10V, I_{D} = 0.115A$ $V_{GS} = 5V, I_{D} = 0.1115A$
Forward Transfer Admittance	Y <sub>fs</sub>	80	320	-	mS	$V_{DS} = 10V, I_D = 0.115A$
Diode Forward Voltage	$V_{SD}$	-	0.7	1.0	V	$V_{GS} = 0V, I_{S} = 0.115A$
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C <sub>iss</sub>	-	25	-	pF	
Output Capacitance	Coss	-	4,7	1	pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$
Reverse Transfer Capacitance	C <sub>rss</sub>	-	2.5	-	pF	
Turn-On Delay Time	t <sub>D(on)</sub>	-	3.27	-	ns	
Turn-On Rise Time	t <sub>r</sub>	-	3.15	•	ns	$V_{DD} = 30V, V_{GEN} = 10V,$
Turn-Off Delay Time	t <sub>D(off)</sub>	-	12.025	1	ns	$R_{GEN} = 25\Omega, I_D = 0.115A$
Turn-Off Fall Time	t <sub>f</sub>	-	6.29	-	ns	

- 4. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
  5. Device mounted on 2" x 2" FR-4 PCB with high coverage 2 oz. Copper, single sided.
  6. Short duration pulse test used to minimize self-heating effect.
  7. Guaranteed by design. Not subject to production testing.







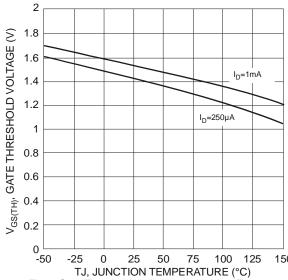
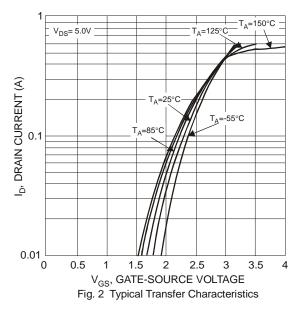
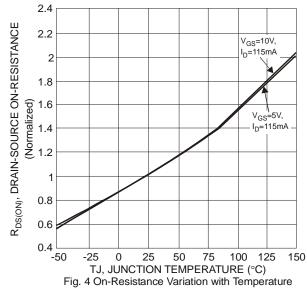
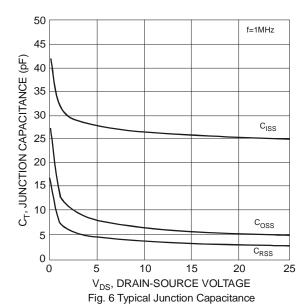


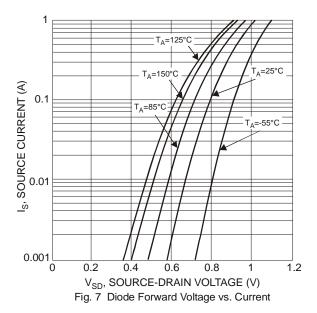
Fig. 5 Gate Threshold Variation vs. Ambient Temperature



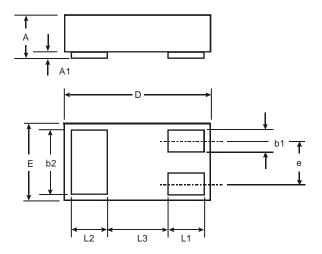






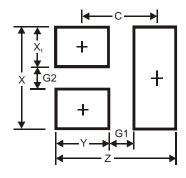


# **Package Outline Dimensions**



DFN1006							
Dim	Min	Max	Тур				
Α	0.47	0.53	0.50				
A1	0	0.05	0.03				
b1	0.10	0.20	0.15				
b2	0.45	0.55	0.50				
D	0.95	1.075	1.00				
Е	0.55	0.675	0.60				
е			0.35				
L1	0.20	0.30	0.25				
L2	0.20	0.30	0.25				
L3			0.40				
All Dimensions in mm							

# **Suggested Pad Layout**



Dimensions	Value (in mm)			
Z	1.1			
G1	0.3			
G2	0.2			
Х	0.7			
X1	0.25			
Y	0.4			
С	0.7			



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