Ordering number : ENA1335B

LC87F2708A

CMOS LSI

8-bit Microcontroller

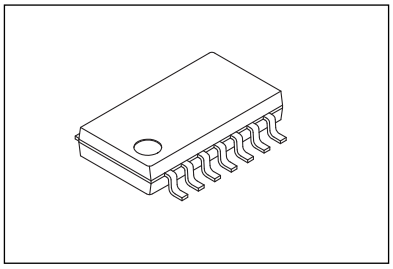
8K-byte Flash ROM / 512-byte RAM / 14-pin

ON Semiconductor®

http://onsemi.com

Overview

The LC87F2708A is an 8-bit microcotroller that, centered around a CPU running at a minimum bus cycle time of 100ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (onboard programmable), 512-byte RAM, an on-chip debugger, a sophisticated 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers or PWMs), a synchronous SIO interface, a high-speed 12-bit PWM, two high-speed pulse width/period counters, a 7-channel AD converter with 12-/8-bit resolution selector, an analog comparator, a watchdog timer, an internal reset circuit, a system clock frequency divider, and a 16-source 10-vector interrupt feature.



MFP14S(225mil)

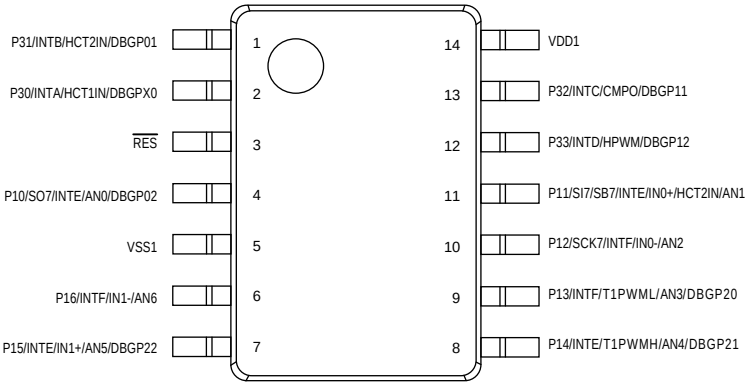
Features

■ Flash ROM
- 8192 × 8 bits
- Capable of on-board-programming with wide range of voltage source (3.0 to 5.5V).
- Block-erasable in 128-byte units

■ RAM
- 512 × 9 bits

■ Minimum Bus Cycle Time Note1
- 100ns (10MHz) V_{DD}=2.7 to 5.5V Note2

■ Minimum Instruction Cycle Time
- 300ns (10MHz) V_{DD}=2.7 to 5.5V Note2



Note1: The bus cycle time here refers to the ROM read speed.
Note2: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is 2.87V±0.12V.

■ Package Form
- MFP14S (Pb-Free / Halogen Free type)

* This product is licensed from Silicon Storage Technology, Inc.

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

Semiconductor Components Industries, LLC, 2014

■ Ports

- I/O ports
  Ports whose I/O direction can be designated in 1 bit units: 11 (P10 to P16, P30 to P33)
- Reset pins: 1 (RES#)
- Power pins: 2 (VSS1, VDD1)

■ Timers

- Timer 0: 16-bit timer/counter with a capture register
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3: 16-bit counter (with a 16-bit capture register)

- Timer 1: 16-bit timer/counter that can provide with PWM/toggle output
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter with an 8-bit prescaler (with toggle output)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle output)
  (Toggle output also possible from lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle output)
  (Lower-order 8 bits may be used as PWM.)

■ Serial Interface

- SIO7: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)

■ High-speed 12-bit PWM

- System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
- Duty/period programmable
- Continuous PWM output/specific count PWM output (automatic stop) selectable

■ High-speed Pulse Width/Period Counter

- HCT1: High-speed pulse width/period counter 1
  1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  2) H-level width/L-level width/period measurement modes selectable
  3) Input triggering noise filter

- HCT2: High-speed pulse width/period counter 2
  1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  2) Can measure both L-level width and period simultaneously.
  3) Input triggering noise filter
  4) Input trigger selectable
  (from 3 signals, i.e., P11/HCT2IN, P31/HCT2IN, and analog comparator output)

■ AD converter: 12 bits × 7 channels

- 12-/8-bit AD converter resolution selectable

■ Analog Comparator
- Sends output to the P32/CMPO port (polarity selectable).
- Edge detection function (shared with INTC and also allows the selection of the noise filter function)

■ Watchdog Timer
- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/ HOLD mode.

■ Interrupt Source Flags
- 16 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INTA
2	0000BH	X or L	INTB
3	00013H	H or L	INTC/T0L/INTE
4	0001BH	H or L	INTD/INTF
5	00023H	H or L	T0H/SIO7
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	HCT1
8	0003BH	H or L	HCT2
9	00043H	H or L	ADC/HPWM automatic stop/HPWM cycle
10	0004BH	H or L	None

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine Stack Levels: 256 levels maximum (The stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillation Circuits
- Medium speed RC oscillation circuit (internal): For system clock (1MHz)
- Low speed RC oscillation circuit (internal): For watchdog timer (30kHz)
- High speed RC oscillation circuit (internal): For system clock (20MHz or 40MHz)

1) 2 source oscillation frequencies (20MHz or 40MHz) selectable for the high-speed RC oscillation circuit by optional configuration.

■ System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (when high speed RC oscillation is selected for system clock.).

■ Programming Board

Package	Programming Board
MFP14S	W87F27M-DBG

■ Flash ROM Programming Board

Maker		Model	Version	Device
Flash Support Group, Inc. (FSG) + ON Semiconductor (Note 4)	In-circuit Programmer	AF9101/AF9103 (Main body) (FSG models)	(Note 5)	LC87F2708A
		SIB87 (Inter Face Driver) (ON Semiconductor model)		
ON Semiconductor	Single/Gang Programmer	SKK-DBG Type B (SanyoFWS)	Application Version 1.04 or later Chip Data Version 2.10 or later	LC87F2708A
	In-circuit/ Gang Programmer			

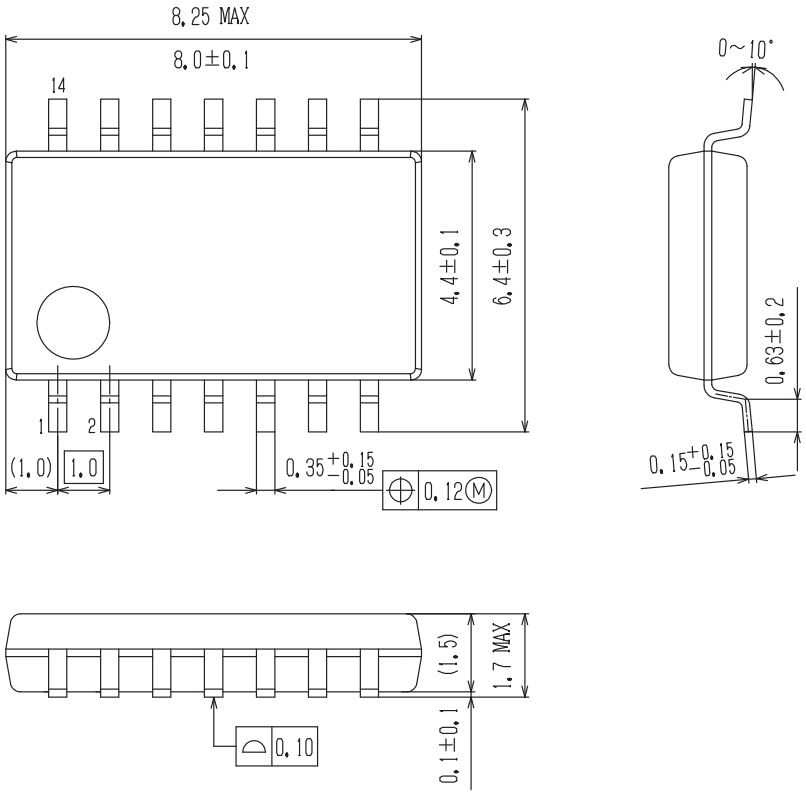
For information about AF-series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

Note4: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from ON Semiconductor (SIB87) together can give a PC-less, standalone on-board-programming capabilities.
Note5: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or ON Semiconductor for the information.

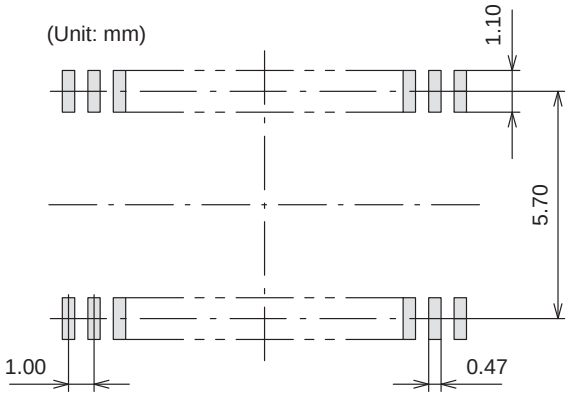
Package Dimensions

unit : mm

SOIC14 W / MFP14S (225 mil)
CASE 751CB
ISSUE A



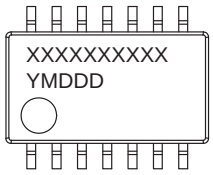
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

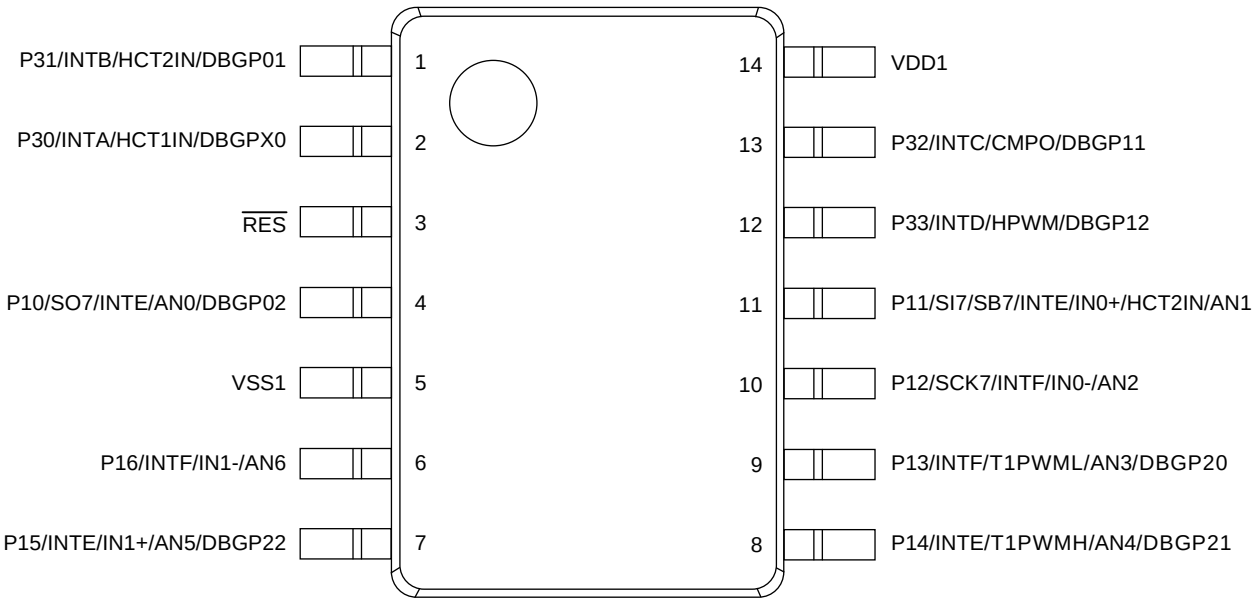
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

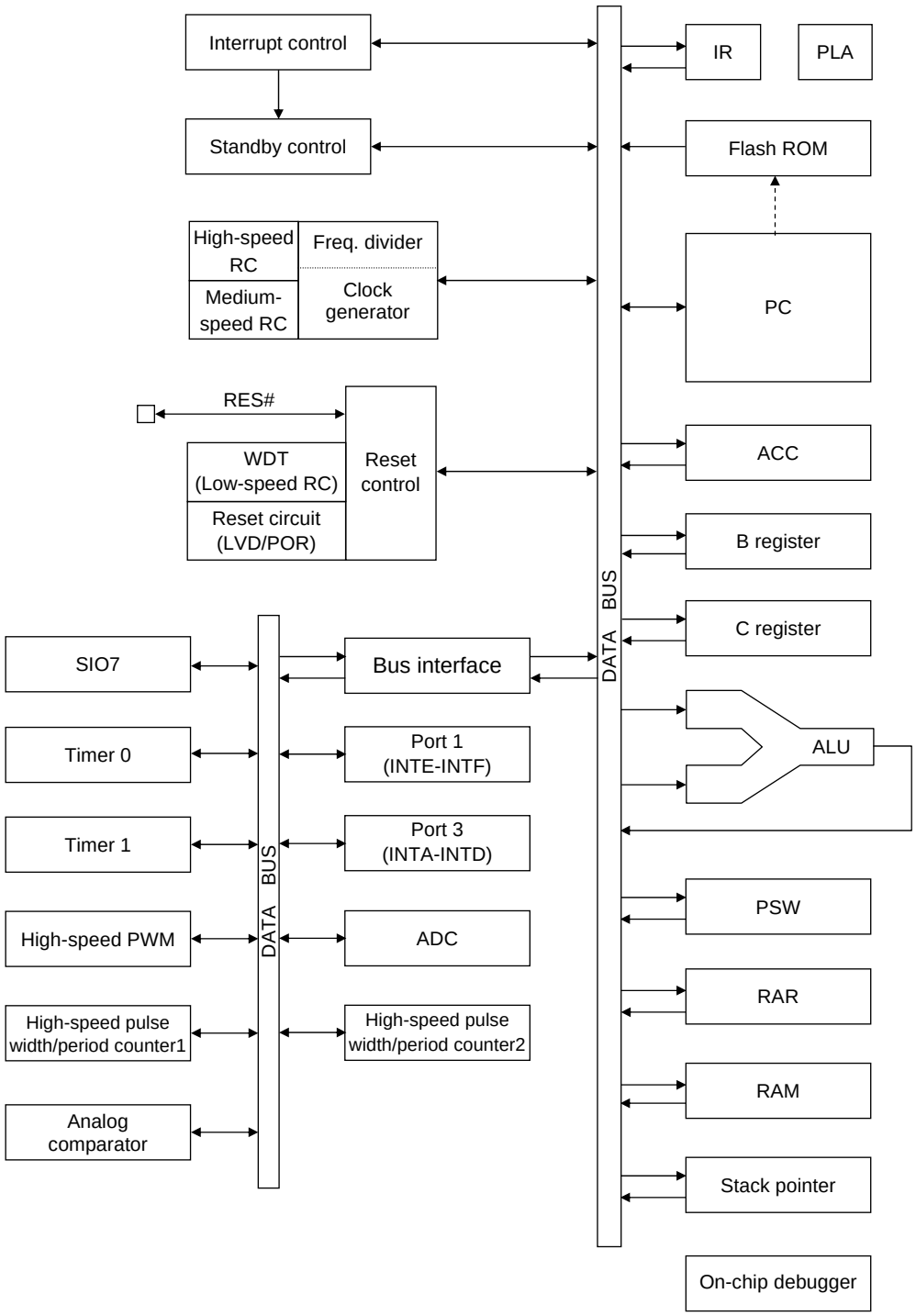
Pin Assignment



MFP14S (Pb-Free / Halogen Free type)

MFP14S	NAME
1	P31/INTB/HCT2IN/DBGP01
2	P30/INTA/HCT1IN/DBGPX0
3	$\overline{\text{RES}}$
4	P10/SO7/INTE/AN0/DBGP02
5	VSS1
6	P16/INTF/IN1-/AN6
7	P15/INTE/IN1+/AN5/DBGP22
8	P14/INTE/T1PWMH/AN4/DBGP21
9	P13/INTF/T1PWML/AN3/DBGP20
10	P12/SCK7/INTF/IN0-/AN2
11	P11/SI7/SB7/INTE/IN0+/HCT2IN/AN1
12	P33/INTD/HPWM/DBGP12
13	P32/INTC/CMPO/DBGP11
14	VDD1

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>–</td><td>– power supply pin</td><td>No</td></tr>
<tr><td>VDD1</td><td>–</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>PORT1
P10 to P16</td><td>I/O</td><td>- 7-bit I/O port
- I/O specifiable in 1-bit units
- Pull-up resistors can be turned on and off in 1-bit units
- Multiplexed pins
P10: SIO7 data output
P11: SIO7 data input/bus I/O
/high-speed pulse width/period counter 2 input
P12: SIO7 clock I/O
P13: Timer 1 PWML output
P14: Timer 1 PWMH output
P10, P11, P14, P15:
INTE input/HOLD release input/timer 1 event input
/timer 0L capture input/timer 0H capture input
P12, P13, P16:
INTF input/HOLD release input/timer 1 event input
/timer 0L capture input/timer 0H capture input
AD converter input port: AN0 to AN6(P10 to P16)
Analog comparator input port 0: IN0+, IN0-(P11, P12)
Analog comparator input port 1: IN1+, IN1-(P15, P16)
On-chip debugger pin 1: DBGP02 (P10)
On-chip debugger pin 3: DBGP20 to DBGP22 (P13 to P15)
- Interrupt acknowledge type
<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr><tr><td>INTE</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr><tr><td>INTF</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr></table></td><td>Yes</td></tr>
<tr><td>PORT3
P30 to P33</td><td>I/O</td><td>- 4-bit I/O port
- I/O specifiable in 1-bit units
- Pull-up resistors can be turned on and off in 1-bit units
- Multiplexed pins
P30: INTA input/HOLD release input/timer 0L capture input
/high-speed pulse width/period counter 1 input
P31: INTB input/HOLD release input/timer 0H capture input
/high-speed pulse width/period counter 2 input
P32: INTC input/HOLD release input/timer 0 event input
/timer 0L capture input/analog comparator output
P33: INTD input/HOLD release input/timer 0 event input
/timer 0H capture input/high-speed PWM output
On-chip debugger pin 1: DBGPX0 to DBGP01(P30 to P31)
On-chip debugger pin 2: DBGPX0 to DBGP12(P30, P32 to P33)
- Interrupt acknowledge type
<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr><tr><td>INTA</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr><tr><td>INTB</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr><tr><td>INTC</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr><tr><td>INTD</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr></table></td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input/internal reset output</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P10 to P16	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P30 to P33	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable

On-chip Debugger Pin Processing

For the processing of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation" and "LC872000 Series On-chip Debugger Pin Processing."

Recommended Unused Pin Connections

Pin Name	Recommended Unused Pin Connections	
	Board	Software
P10 to P16	OPEN	Set output low
P30 to P33	OPEN	Set output low

User Options

Option Name	Option Type	Flash Version	Option Switched in Unit of	Description
Port output type	P10 to P16	○	1bit	CMOS
				N-channel open drain
	P30 to P33	○	1bit	CMOS
				N-channel open drain
Program start address	–	○	–	00000H
				01E00H
Brown-out detector reset function	Brown-out detector function	○	–	Enable: Used
				Disable: Not used
	Brown-out trip level	○	–	3 levels
Power-on-reset function	Power-on-reset level	○	–	3 levels
High-speed RC oscillator circuit	Oscillation frequency	○	–	20 MHz
				40 MHz

1. Absolute Maximum Ratings at Ta=25°C, $V_{SS}1$=0V

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			
						min.	typ.	max.	unit
Maximum supply voltage		V_{DD}MAX	VDD1			–0.3	to	+6.5	V
Input voltage		VI	RES#			–0.3	to	V_{DD}+0.3	
Input/output voltage		VIO	・Port 1 ・Port 3			–0.3	to	V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Port 1	・CMOS output selected ・Per applicable pin		–7.5			mA
		IOPH(2)	Port 3	・CMOS output selected ・Per applicable pin		–10			
	Mean output current (Note 1-1)	IOMH(1)	Port 1	・CMOS output selected ・Per applicable pin		–5			
		IOMH(2)	Port 3	・CMOS output selected ・Per applicable pin		–7.5			
	Total output current	ΣIOAH(1)	・Ports 10, 15, 16 ・Ports 30, 31	Total of currents at all applicable pins		–20			
		ΣIOAH(2)	・Ports 11 to 14 ・Ports 32, 33	Total of currents at all applicable pins		–20			
		ΣIOAH(3)	・Port 1 ・Port 3	Total of currents at all applicable pins		–35			
Low level output current	Peak output current	IOPL(1)	Port 1	Per applicable pin				15	
		IOPL(2)	Port 3	Per applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	Port 1	Per applicable pin				10	
		IOML(2)	Port 3	Per applicable pin				7.5	
	Total output current	ΣIOAL(1)	・Port 10 ・Ports 30, 31	Total of currents at all applicable pins				25	
		ΣIOAL(2)	・Ports 11 to 16 ・Ports 32, 33	Total of currents at all applicable pins				35	
		ΣIOAL(3)	・Port 1 ・Port 3	Total of currents at all applicable pins				55	
Power dissipation		Pdmax(1)	MFP14S	・Ta=–40 to +85°C ・Independent package				113	mW
		Pdmax(2)		・Ta=–40 to +85°C ・Mounted on thermal test board ・(Note 1-2)				260	
Operating ambient temperature		Topr				–40	to	+85	°C
Storage ambient temperature		Tstg				–55	to	+125	

Note 1-1: Mean output current refers to the average of output currents measured for a period of 100ms.
Note 1-2: Thermal test board used conforms to SEMI (size : 76.1 × 114.3 × 1.6 tmm, glass epoxy board).

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Allowable Operating Conditions at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Operating supply voltage (Note 2-1)	V_{DD}	VDD1	0.272μs ≤ tCYC ≤ 100μs		2.7		5.5	V
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode		2.0		5.5	
High level input voltage	VIH(1)	・Port 1 ・Port 3	Output disabled	2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	VIH(2)	RES#		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	VIL(1)	・Port 1 ・Port 3	Output disabled	4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	VIL(2)	RES#		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 5.5	0.272		100	μs
Oscillation frequency range	FmHRC(1)		・High-speed RC oscillation ・40MHz selected as option ・Ta=–20 to +85°C	4.5 to 5.5	38	40	42	MHz
	FmHRC(2)		・High-speed RC oscillation ・40MHz selected as option ・Ta=–40 to +85°C	4.5 to 5.5	37.6	40	42.4	
	FmHRC(3)			3.5 to 5.5	36.8	40	43.2	
	FmHRC(4)			2.7 to 5.5	32	40	43.2	
	FmHRC(5)		・High-speed RC oscillation ・20MHz selected as option ・Ta=–20 to +85°C	3.0 to 5.5	19	20	21	
	FmHRC(6)		・High-speed RC oscillation ・20MHz selected as option ・Ta=–40 to +85°C	2.7 to 5.5	18.7	20	21.3	
	FmRC		Medium-speed RC oscillation	2.7 to 5.5	0.5	1.0	2.0	
	FmSLRC		Low-speed RC oscillation	2.7 to 5.5	15	30	60	kHz
Oscillation stabilization time	tmsHRC		・When high-speed RC oscillation state is switched from stopped to enabled. ・See Fig. 2.	2.7 to 5.5			100	μs

Note 2-1: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is 2.87V±0.12V.

Note 2-2: Relationship between tCYC and oscillation frequency is as follows:

- When system clock source is set to medium-speed RC oscillation
  3/FmRC at a division ratio of 1/1, 6/FmRC at a division ratio of 1/2, 12/FmRC a division ratio of 1/4, and so forth
- When system clock source is set to high-speed RC oscillation (40MHz selected by optional configuration)
  12/FmHRC at a division ratio of 1/1, 24/FmHRC at a division ratio of 1/2, 48/FmHRC a division ratio of 1/4, and so forth
- When system clock source is set to high-speed RC oscillation (20MHz selected by optional configuration)
  6/FmHRC at a division ratio of 1/1, 12/FmHRC at a division ratio of 1/2, 24/FmHRC a division ratio of 1/4, and so forth

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Electrical Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
High level input current	IIH(1)	・Port 1 ・Port 3	・Output disabled ・Pull-up resistor off ・$V_{IN}=V_{DD}$ (including output Tr. off leakage current)	2.7 to 5.5			1	μA
	IIH(2)	RES#	$V_{IN}=V_{DD}$	2.7 to 5.5			1	
Low level input current	IIL	・Port 1 ・Port 3	・Output disabled ・Pull-up resistor off ・$V_{IN}=V_{SS}$ (including output Tr. off leakage current)	2.7 to 5.5	–1			
High level output voltage	VOH(1)	CMOS output type port 1	IOH=–1mA	4.5 to 5.5	V_{DD}–1			V
	VOH(2)		IOH=–0.35mA	2.7 to 5.5	V_{DD}–0.4			
	VOH(3)	CMOS output type port 3	IOH=–5mA	4.5 to 5.5	V_{DD}–1.5			
	VOH(4)		IOH=–0.7mA	2.7 to 5.5	V_{DD}–0.4			
Low level output voltage	VOL(1)	Port 1	IOL=10mA	4.5 to 5.5			1.5	
	VOL(2)		IOL=1.4mA	2.7 to 5.5			0.4	
	VOL(3)	Port 3	IOL=5mA	4.5 to 5.5			1.5	
	VOL(4)		IOL=0.7mA	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	・Port 1 ・Port 3	VOH=0.9V_{DD}	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 4.5	18	50	150	
	Rpu(3)	RES#		2.7 to 5.5	216	360	504	
Hysteresis voltage	VHYS	・Port 1 ・Port 3 ・RES#		2.7 to 5.5		0.1V_{DD}		V
Pin capacitance	CP	All pins	・$V_{IN}=V_{SS}$ for pins other than that under test ・f=1MHz ・Ta=25°C	2.7 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Serial I/O Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

4-1. SIO7 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min.	typ.	max.	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK7(P12)	・See Fig. 4. (Note 4-1-2)	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK7(P12)	・CMOS output selected ・See Fig. 4.	2.7 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SB7(P11), SI7(P11)	・Must be specified with respect to rising edge of SIOCLK. ・See Fig. 4.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdDO(1)	SO7(P10), SB7(P11)	・Must be specified with respect to rising edge of SIOCLK. ・Must be specified as the time to the beginning of output state change in open drain output mode. ・See Fig. 4.	2.7 to 5.5			1tCYC +0.05	
	Output clock		tdDO(2)						(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in transmission/reception mode, the time from SI7RUN being set when serial clock is "H" to the first falling edge of the serial clock must be longer than 1tCYC.

5. Pulse Input Conditions at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INTA(P30), INTB(P31), INTD(P33), INTE (P10, P11, P14, P15), INTF (P12, P13, P16)	・Interrupt source flag can be set. ・Event inputs for timers 0 and 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INTC(P32) when noise filter time constant is "none"	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	2.7 to 5.5	1			
	tPIH(3) tPIL(3)	INTC(P32) when noise filter time constant is "1/16"	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INTC(P32) when noise filter time constant is "1/32"	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	2.7 to 5.5	128			
	tPIH(5) tPIL(5)	INTC(P32) when noise filter time constant is "1/64"	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIH(6) tPIL(6)	HCT1IN(P30)	Pulses can be recognized as signals by the high-speed pulse width/period counter 1.	2.7 to 5.5	3			H1CK (Note 5-1)
	tPIH(7) tPIL(7)	HCT2IN(P11, P31)	Pulses can be recognized as signals by the high-speed pulse width/period counter 2.	2.7 to 5.5	6			H2CK (Note 5-2)
	tPIL(8)	RES#	Resetting is enabled.	2.7 to 5.5	200			µs

Note 5-1: H1CK denotes the period of the base clock (1 to 8 × high-speed RC oscillation clock or system clock) for the high-speed pulse width/period counter 1.

Note 5-2: H2CK denotes the period of the base clock (2 to 16 × high-speed RC oscillation clock or system clock) for the high-speed pulse width/period counter 2.

6. Comparator Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	Unit
Common mode input voltage range	VCMIN	IN0+(P11), IN0–(P12), IN1+(P15), IN1–(P16)		2.7 to 5.5	V_{SS}		V_{DD} –1.5	V
Offset voltage	VOFF		Within common mode input voltage range	2.7 to 5.5		±10	±30	mV
Response time	tRT		・Within common mode input voltage range ・Input amplitude=100mV ・Overdrive=50mV	2.7 to 5.5		200	600	ns
Operation stabilization time (Note 6-1)	tCMW			2.7 to 5.5			1.0	µs

Note 6-1: The interval after CMPON is set till the operation gets stabilized.

7. AD Converter Characteristics at $V_{SS}1$=0V

< 12-bit AD conversion mode at Ta=–40 to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Resolution	N	AN0(P10) to AN6(P16)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note7-1)	3.0 to 5.5			±16	LSB
Conversion time	tCAD		・See "Conversion time calculation method." ・(Note7-2)	4.0 to 5.5	38		104.3	μs
				3.0 to 5.5	75.8		104.3	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	–1			

< 8-bit AD conversion mode at Ta=–40 to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Resolution	N	AN0(P10) to AN6(P16)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note7-1)	3.0 to 5.5			±1.5	LSB
Conversion time	tCAD		・See "Conversion time calculation method." ・(Note7-2)	4.0 to 5.5	23.4		64.3	μs
				3.0 to 5.5	46.7		64.3	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	–1			

< Conversion time calculation method >

12-bit AD conversion mode: tCAD (conversion time) = ((52/(division ratio)) + 2) × (1/3) × tCYC
8-bit AD conversion mode: tCAD (conversion time) = ((32/(division ratio)) + 2) × (1/3) × tCYC

< Recommended Operating Conditions >

High-speed RC Oscillation (FmHRC)	Supply Voltage Range (V_{DD})	System Clock Division Ratio (SYSDIV)	Cycle Time (tCYC)	AD Division Ratio (ADDIV)	Conversion Time (tCAD)	
					12-bit AD	8-bit AD
40MHz/20MHz	4.0V to 5.5V	1/1	300ns	1/8	41.8μs	25.8μs
	3.0V to 5.5V	1/1	300ns	1/16	83.4μs	51.4μs

Note 7-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.

Note 7-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital conversion value against the analog input value is loaded in the result register.

* The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

8. Power-on Reset (POR) Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions	Option Selecting Voltage	Specification min.	typ.	max.	unit
POR release voltage	PORRL		・Option selected ・See Fig. 6. (Note 8-1)	2.87V	2.75	2.87	2.99	V
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Unknown voltage area	POUKS		・See Fig. 6. (Note 8-2)			0.7	0.95	
Power startup time	PORIS		Power startup time from V_{DD}=0V to 2.8V				100	ms

Note 8-1: The POR release voltage can be selected from three levels when the low-voltage detection feature is deselected.
Note 8-2: There is an unpredictable period before the power-on reset transistor starts to turn on.

9. Low-voltage Detection (LVD) Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions	Option Selecting Voltage	Specification min.	typ.	max.	unit
LVD reset voltage (Note 9-2)	LVDET		・Option selected ・See Fig. 7. (Note 9-1) (Note 9-3)	2.81V	2.71	2.81	2.91	V
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD voltage hysteresis	LVHYS			2.81V		60		mV
				3.79V		65		
				4.28V		65		
Unknown voltage area	LVUKS		・See Fig. 7. (Note 9-4)			0.7	0.95	V
Minimum low voltage detection width (response sensitivity)	tLVDW		・LVDET-0.5V ・See Fig. 8.		0.2			ms

Note 9-1: The LVD reset voltage can be selected from three levels when the low-voltage detection feature is selected.
Note 9-2: The hysteresis voltage is not included in the LVD reset voltage value.
Note 9-3: There are cases when the LVD reset voltage value is exceeded when a greater change in the output level or large current is applied to the port.
Note 9-4: There is an unpredictable period before the low-voltage detection resetting transistor starts to run.

10. Consumption Current Characteristics at Ta=–40 to +85°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Normal mode consumption current (Note 10-1)	IDDOP(1)	VDD1	・FmHRC=40MHz oscillation mode ・System clock set to high-speed RC, 10MHz (1/4 of 40MHz)	4.5 to 5.5		7.8	14	mA
	IDDOP(2)		・Medium-speed RC oscillation stopped ・System clock frequency division ratio set to 1/1	2.7 to 3.6		4.9	9.4	
	IDDOP(3)		・FmHRC=20MHz oscillation mode ・System clock set to high-speed RC, 10MHz (1/2 of 20MHz)	4.5 to 5.5		7.1	12.8	
	IDDOP(4)		・Medium-speed RC oscillation stopped ・System clock frequency division ratio set to 1/1	2.7 to 3.6		4.5	8.6	
	IDDOP(5)		・High-speed RC oscillation stopped ・System clock set to medium-speed RC oscillation mode	4.5 to 5.5		0.60	1.9	
	IDDOP(6)		・System clock frequency division ratio set to 1/2	2.7 to 3.6		0.38	1.3	
HALT mode consumption current (Note 10-1)	IDDHALT(1)		HALT mode ・FmHRC=40MHz oscillation mode ・System clock set to high-speed RC, 10MHz(1/4 of 40MHz)	4.5 to 5.5		3.2	5.0	
	IDDHALT(2)		・Medium-speed RC oscillation stopped ・System clock frequency division ratio set to 1/1	2.7 to 3.6		2.0	3.1	
	IDDHALT(3)		HALT mode ・FmHRC=20MHz oscillation mode ・System clock set to high-speed RC, 10MHz (1/2 of 20MHz)	4.5 to 5.5		2.5	3.9	
	IDDHALT(4)		・Medium-speed RC oscillation stopped ・System clock frequency division ratio set to 1/1	2.7 to 3.6		1.6	2.5	
	IDDHALT(5)		HALT mode ・High-speed RC oscillation stopped ・System clock set to medium-speed RC oscillation mode	4.5 to 5.5		0.32	1.0	
	IDDHALT(6)		・System clock frequency division ratio set to 1/2	2.7 to 3.6		0.16	0.55	
HOLD mode consumption current (Note 10-1)	IDDHOLD(1)		HOLD mode ・Ta=–10 to +50°C	4.5 to 5.5		0.04	3.0	μA
	IDDHOLD(2)			2.7 to 3.6		0.02	1.8	
	IDDHOLD(3)		HOLD mode ・Ta=–40 to +85°C	4.5 to 5.5		0.04	34	
	IDDHOLD(4)			2.7 to 3.6		0.02	22	
	IDDHOLD(5)		HOLD mode ・LVD option selected ・Ta=–10 to +50°C	4.5 to 5.5		3.1	6.8	
	IDDHOLD(6)			2.7 to 3.6		2.4	4.2	
	IDDHOLD(7)		HOLD mode ・LVD option selected ・Ta=–40 to +85°C	4.5 to 5.5		3.1	39	
	IDDHOLD(8)			2.7 to 3.6		2.4	25	
	IDDHOLD(9)		HOLD mode ・Watchdog timer active ・Ta=–10 to +50°C	4.5 to 5.5		3.4	10	
	IDDHOLD(10)			2.7 to 3.6		1.7	6.0	
	IDDHOLD(11)		HOLD mode ・Watchdog timer active ・Ta=–40 to +85°C	4.5 to 5.5		3.4	42	
	IDDHOLD(12)			2.7 to 3.6		1.7	27	
	IDDHOLD(13)		HOLD mode ・Comparator active (IN+=V_{DD}, IN–=V_{SS})	4.5 to 5.5		110	160	
	IDDHOLD(14)			2.7 to 3.6		65	100	

Note 10-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

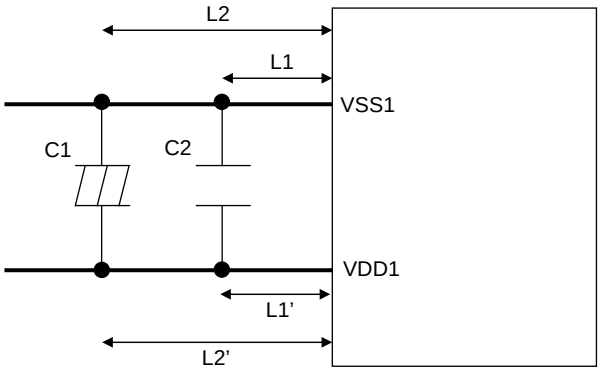
11. F-ROM Programming Characteristics at Ta=+10 to +55°C, $V_{SS}1$=0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification		
				VDD[V]	min.	typ.	max.	unit
Onboard programming current	IDDFW	VDD1	・Microcontroller consumption current is excluded.	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		・Erase operation	3.0 to 5.5		20	30	ms
	tFW(2)		・Programming operation			40	60	μs

12. Power Pin Treatment Recommendations (VDD1, VSS1)

Connect bypass capacitors that meet the following conditions between the VDD1 and VSS1 pins:

・Connect among the VDD1 and VSS1 pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
・Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
The capacitance of C2 should be approximately 0.1μF.



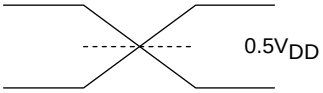


Figure 1 AC Timing Measurement Point

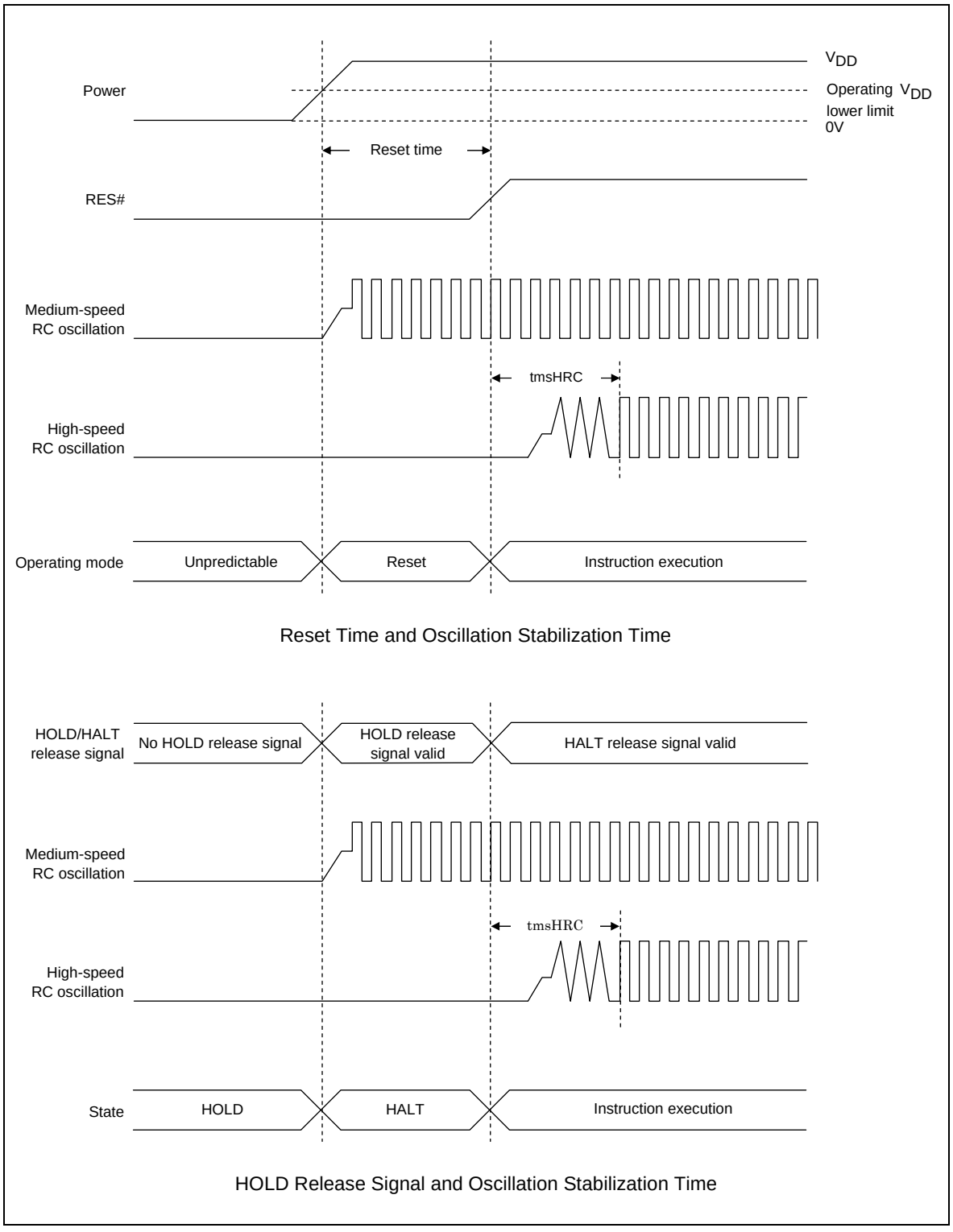
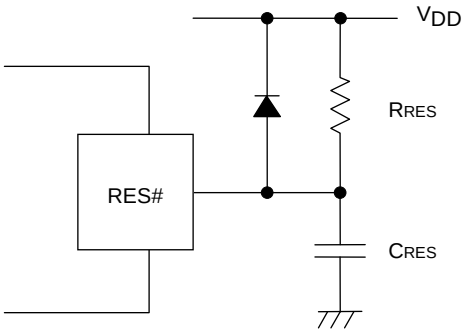


Figure 2 Oscillation Stabilization Times



Note:
The external peripheral circuit differs depending on the way in which the power-on reset and low-voltage detection reset functions are used. Refer to the Chapter, entitled "Reset Function," of the user's manual.

Figure 3 Sample Reset Circuit

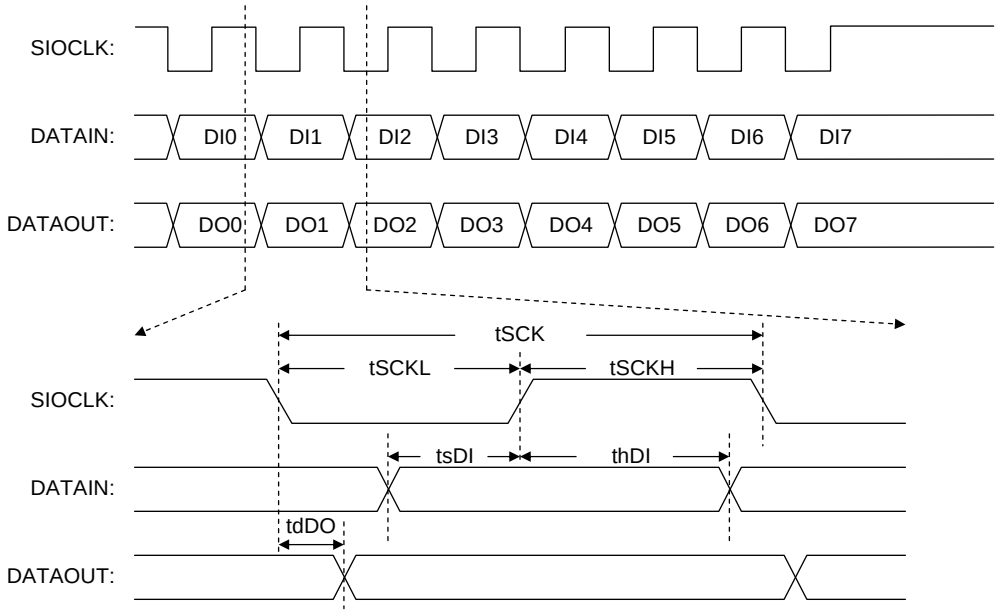


Figure 4 Serial I/O Waveforms

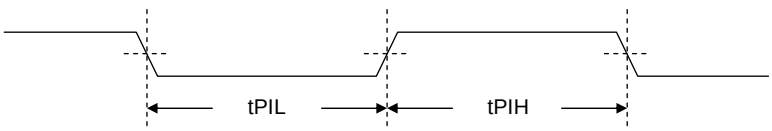


Figure 5 Pulse Input Timing Signal Waveform

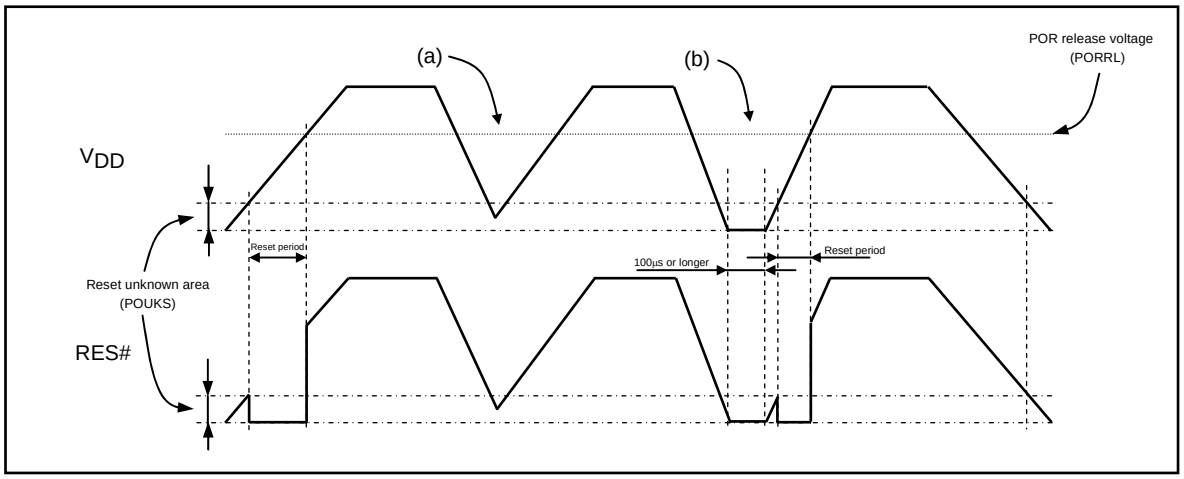


Figure 6 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with RRES Pull-up Resistor Only)

- The POR circuit generates a reset signal only when the power voltage is raised from the VSS level.
- No stable reset signal is generated if power is turned on again when the power voltage does not go down to the VSS level as shown in (a). If this case is anticipated, use the LVD function as explained below or configure an external reset circuit.
- A reset is effected only when power is turned on again after the power voltage goes down to and remains at the VSS level for 100μs or longer as shown in (b).

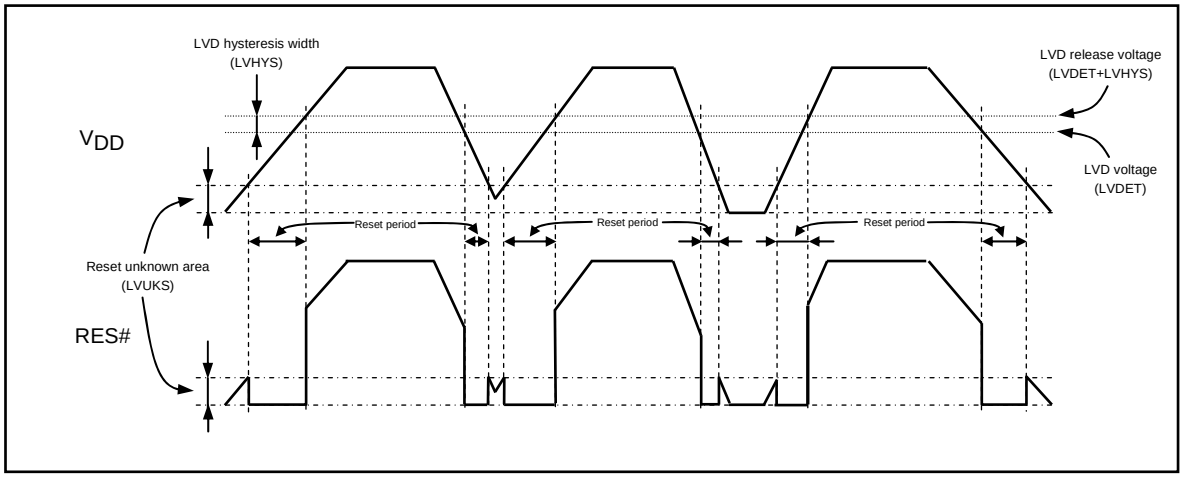


Figure 7 Example of POR + LVD Mode Waveforms (at Reset Pin with RRES Pull-up Resistor Only)

- A reset is effected both when power is turned on and when it goes down.
- The hysteresis width (LVHYS) is introduced in the LVD circuit to prevent the iterations of the IC entering and exiting the reset state near the detection threshold level.

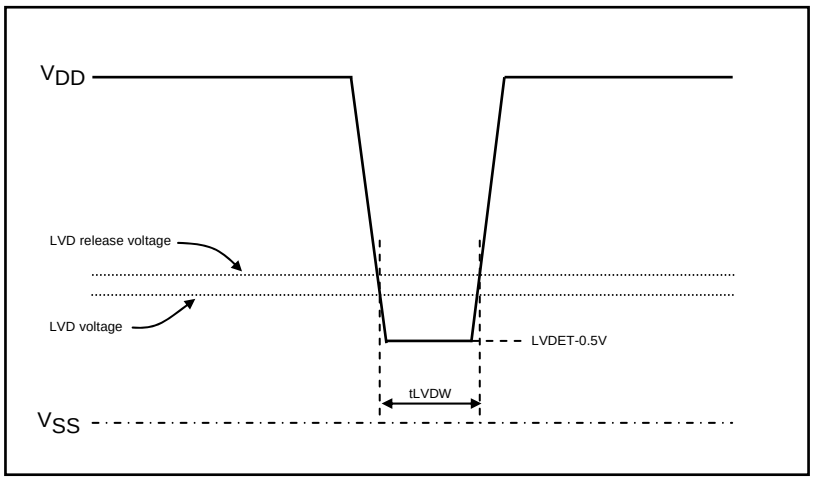


Figure 8 Minimum Low Voltage Detection Width
(Example of Short Interruption of Power/ Power Fluctuation Waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F2708AUMD-AH	MFP14S(225mil) (Pb-Free / Halogen Free)	1000 / Tape & Reel

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