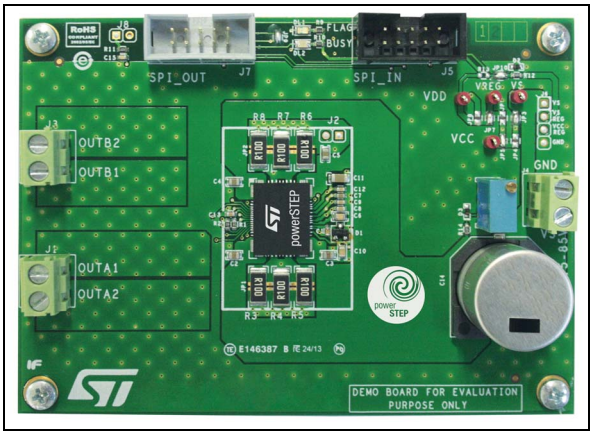
EVLPOWERSTEP01

System-in-package integrating microstepping controller and 10 A power MOSFETs demonstration board

Data brief



Features

- Voltage range from 10.5 V to 85 V
- 10 $A_{r.m.s.}$ maximum output current
- Up to 1/128 microstep
- Programmable speed profile and advanced commands
- Adjustable output slew rate
- SPI with daisy chain feature
- FLAG and BUSY LED indicators
- Flexible supply voltage management
- Suitable to be used in combination with STEVAL-PCC009V2

Applications

- High power bipolar stepper motors:
  - Stage lighting
  - Surveillance systems
  - Textile and sewing machines
  - Pick and place machines

Description

The EVLPOWERSTEP01 demonstration board is a microstepping motor driver delivering up to 10 $A_{r.m.s.}$. In combination with the STEVAL-PCC009V2 communication board and the evaluation software, the board allows the user to investigate all the features of the powerSTEP01. In particular, the board can be used to check the performance and to regulate the parameters in order to fit the application requirements.

The EVLPOWERSTEP01 supports the daisy chain configuration making it suitable for the evaluation of the powerSTEP01 in multi motor applications.

Board description

Table 1. Electrical specifications

Parameter	Value
Supply voltage (VS)	10.5 V to 85 V
Maximum output current (each phase)	10 $A_{r.m.s.}$
Gate drivers supply voltage (VCC)	7.5 V to 15 V
Logic supply voltage	3.3 V
Logic interface supply voltage	3.3 V or 5 V
Low logic level input	0 V
High logic level input	VDD(1)
Operating ambient temperature	0 °C to +85 °C

1. All logic inputs are 5 V tolerant.

Figure 1. Jumpers and connectors location

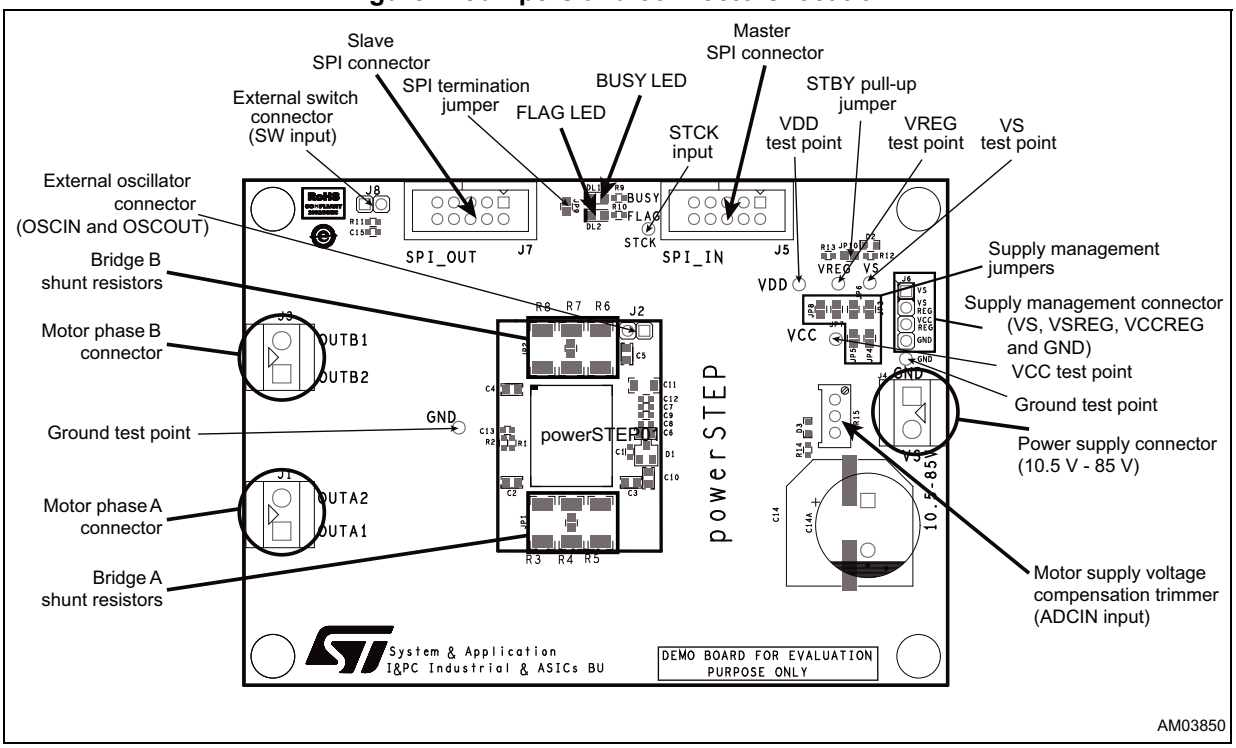


Table 2. Jumpers and connectors description

Name	Type	Function
J4	Power supply	Main supply voltage
J1	Power output	Power bridge A outputs
J3	Power output	Power bridge B outputs
J6	Power supply	Integrated voltage regulator inputs
J5	SPI	Master SPI connector
J7	SPI	Slave SPI connector
JP3	Jumper	VS to VSREG jumper
JP4	Jumper	VSREG to VCC jumper
JP5	Jumper	VCC to VCCREG jumper
JP6	Jumper	VCCREG to VREG jumper
JP7	Jumper	VREG to VDD jumper
JP8	Jumper	VDD to 3.3 V from SPI connector jumper
JP9	Jumper	Daisy chain termination jumper
JP10	Jumper	STBY to VS pull-up jumper

Table 3. Master SPI connector pinout (J5)

Pin number	Type	Function
1	Open drain output	powerSTEP01 BUSY output
2	Open drain output	powerSTEP01 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI “Master In Slave Out” signal (connected to powerSTEP01 SDO output through daisy chain termination jumper JP9)
6	Digital input	SPI “Serial Clock” signal (connected to powerSTEP01 CK input)
7	Digital input	SPI “Master Out Slave In” signal (connected to powerSTEP01 SDI input)
8	Digital input	SPI “Slave Select” signal (connected to powerSTEP01 CS input)
9	Digital input	powerSTEP01 step-clock input
10	Digital input	powerSTEP01 standby/reset input

Table 4. Slave SPI connector pinout (J7)

Pin number	Type	Function
1	Open drain output	powerSTEP01 BUSY output
2	Open drain output	powerSTEP01 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI “Master In Slave Out” signal (connected to pin 5 of J5)
6	Digital input	SPI “Serial Clock” signal (connected to powerSTEP01 CK input)
7	Digital input	SPI “Master Out Slave In” signal (connected to powerSTEP01 SDO output)
8	Digital input	SPI “Slave Select” signal (connected to powerSTEP01 CS input)
9	Digital input	powerSTEP01 step-clock input
10	Digital input	powerSTEP01 standby/reset input

Figure 2. Schematic page 1 of 2

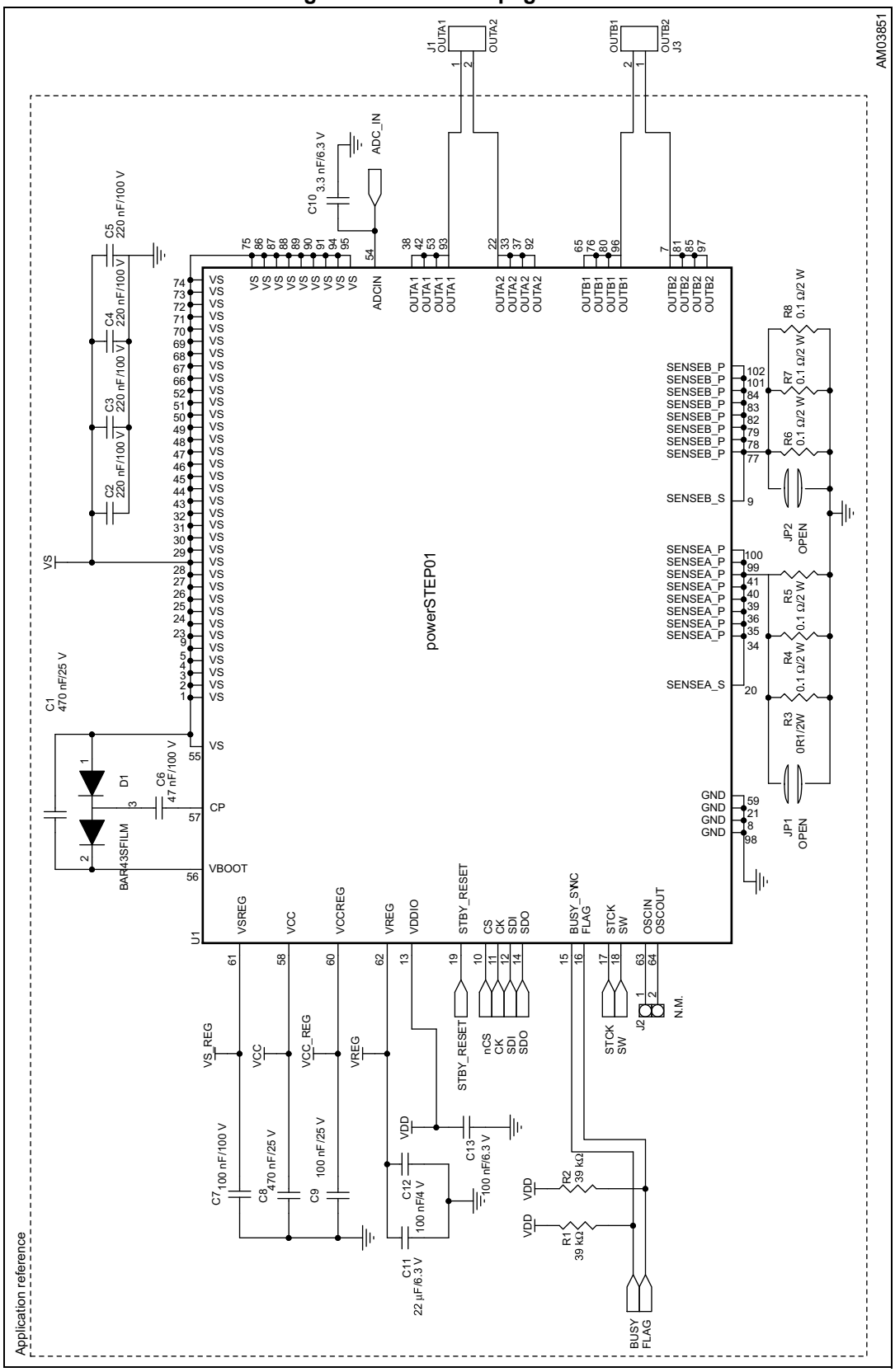
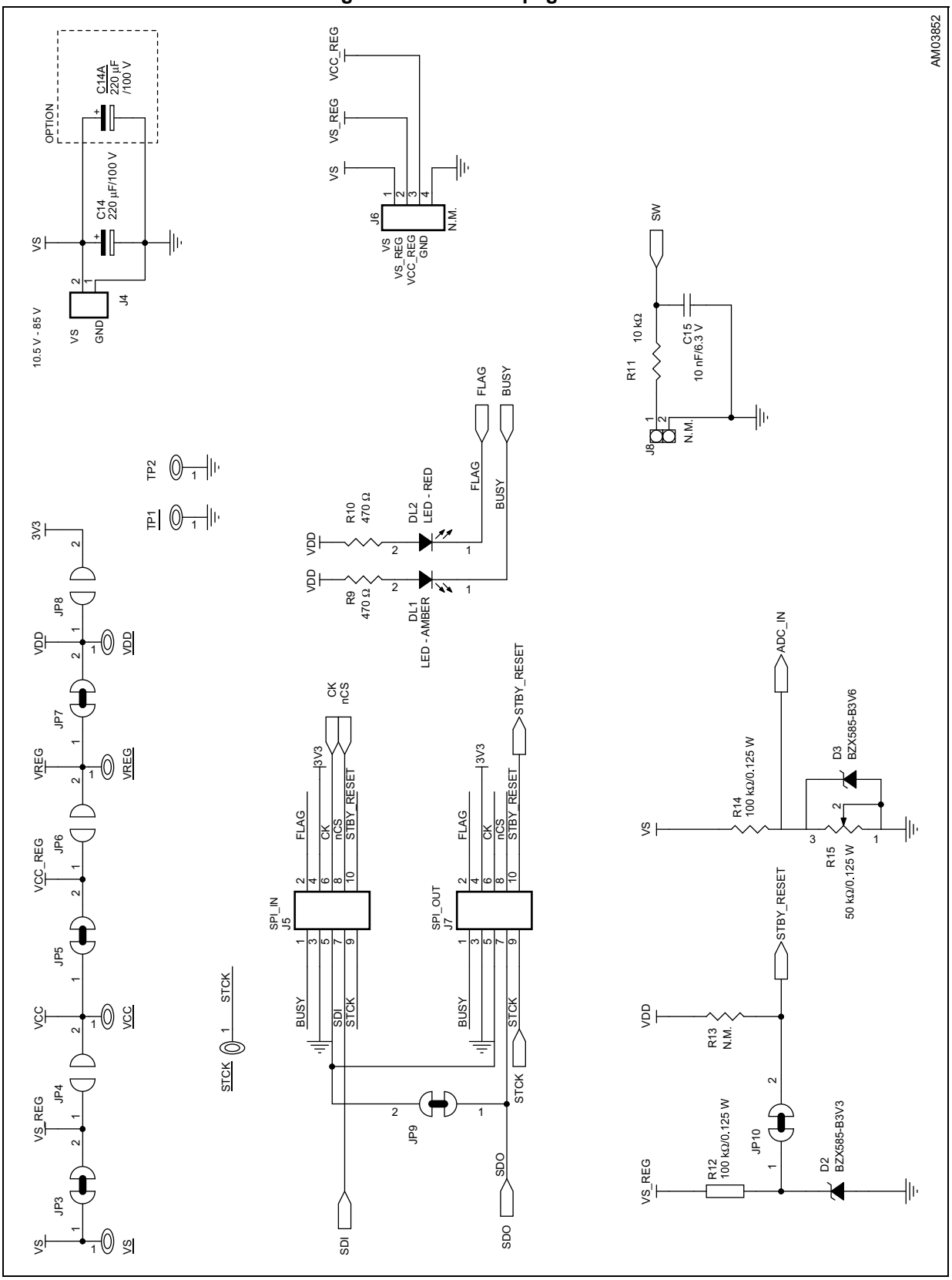


Figure 3. Schematic page 2 of 2



Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Oct-2014	1	Initial release.