



# N-Channel Depletion-Mode Vertical DMOS FETs

## Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

## Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Linear amplifiers
- ▶ Constant current sources
- ▶ Power supply circuits
- ▶ Telecom

## Ordering Information

Part Number	Package Option	Packing
DN2535N3-G	TO-92	1000/Bag
DN2535N3-G P002	TO-92	2000/Reel
DN2535N3-G P003		
DN2535N3-G P005		
DN2535N3-G P013		
DN2535N3-G P014		
DN2535N5-G	TO-220	50/Tube

-G denotes a lead (Pb)-free / RoHS compliant package.  
 Contact factory for Wafer / Die availability.  
 Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

## Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSX}$
Drain-to-gate voltage	$BV_{DGX}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Typical Thermal Resistance

Package	$\theta_{ja}$
TO-92	132°C/W
TO-220	29°C/W

## General Description

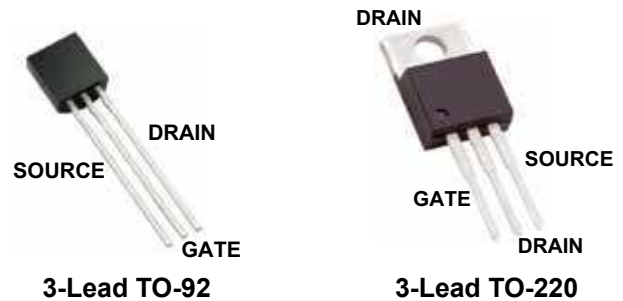
The Supertex DN2535 is a low threshold depletion mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Product Summary

$BV_{DSX}/BV_{DGX}$	$R_{DS(ON)}$ (max)	$I_{DSS}$ (min)
350V	25Ω	150mA

## Pin Configuration



## Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

### 3-Lead TO-92



L = Lot Number  
 YY = Year Sealed  
 WW = Week Sealed  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

### 3-Lead TO-220

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup>	$I_D$ (pulsed)	Power Dissipation @ $T_c = 25^\circ\text{C}$	$I_{DR}$ <sup>†</sup>	$I_{DRM}$
TO-92	120mA	500mA	1.0W	120mA	500mA
TO-220	500mA	500mA	15W	500mA	500mA

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_J$ .

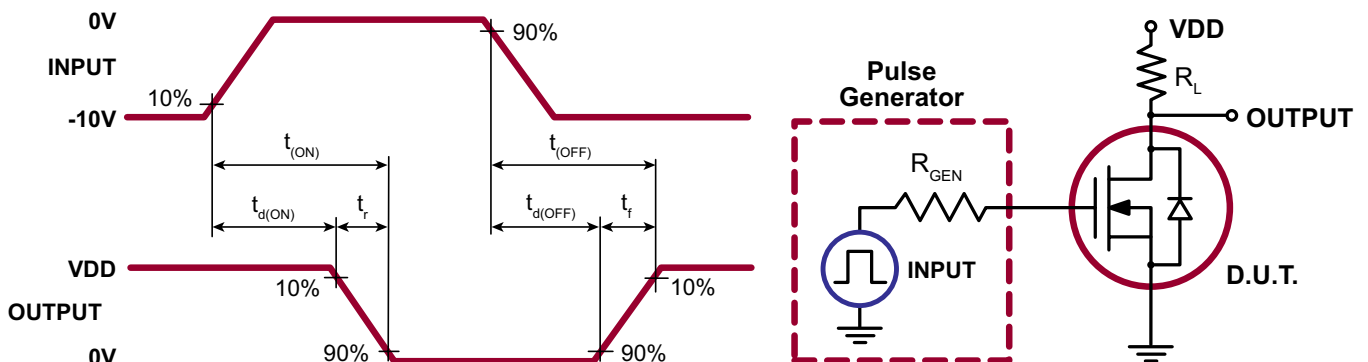
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSX}$	Drain-to-source breakdown voltage	350	-	-	V	$V_{GS} = -5.0\text{V}, I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	$V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$
$I_{GSS}$	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	10	$\mu\text{A}$	$V_{DS} = \text{Max rating}, V_{GS} = -10\text{V}$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = -10\text{V}, T_A = 125^\circ\text{C}$
$I_{DSS}$	Saturated drain-to-source current	150	-	-	mA	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	17	25	$\Omega$	$V_{GS} = 0\text{V}, I_D = 120\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}, I_D = 120\text{mA}$
$G_{FS}$	Forward transconductance	-	325	-	mmho	$V_{DS} = 10\text{V}, I_D = 100\text{mA}$
$C_{ISS}$	Input capacitance	-	200	300	pF	$V_{GS} = -10\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$
$C_{OSS}$	Common source output capacitance	-	12	30		
$C_{RSS}$	Reverse transfer capacitance	-	1.0	5.0		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = 25\text{V}, I_D = 150\text{mA}, R_{GEN} = 25\Omega,$
$t_r$	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	15		
$t_f$	Fall time	-	-	20		
$V_{SD}$	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = -10\text{V}, I_{SD} = 120\text{mA}$
$t_{rr}$	Reverse recovery time	-	800	-	ns	$V_{GS} = -10\text{V}, I_{SD} = 1.0\text{A}$

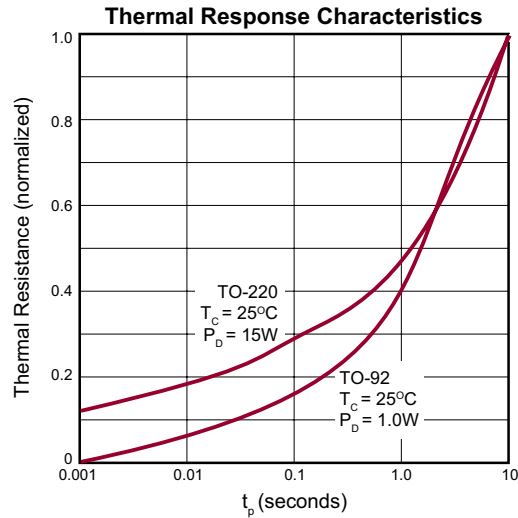
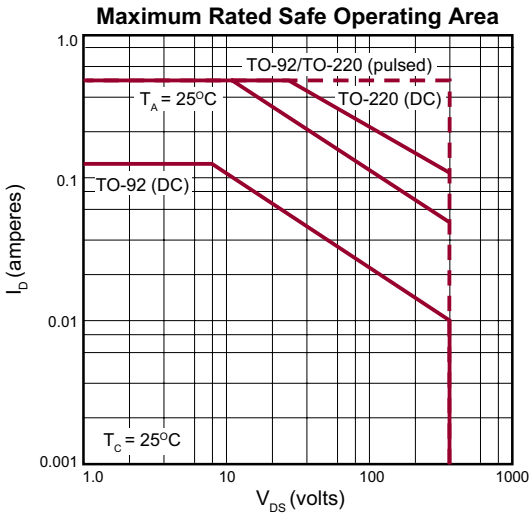
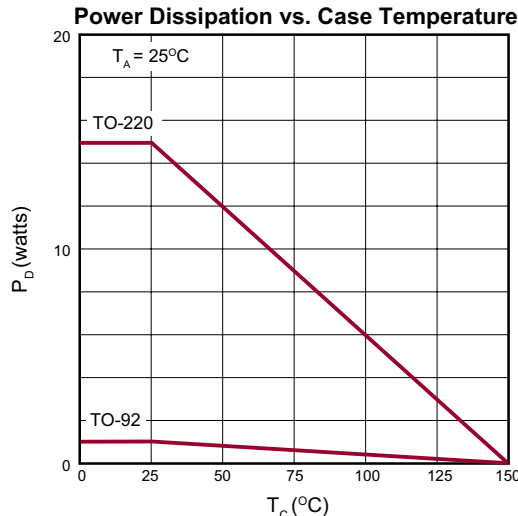
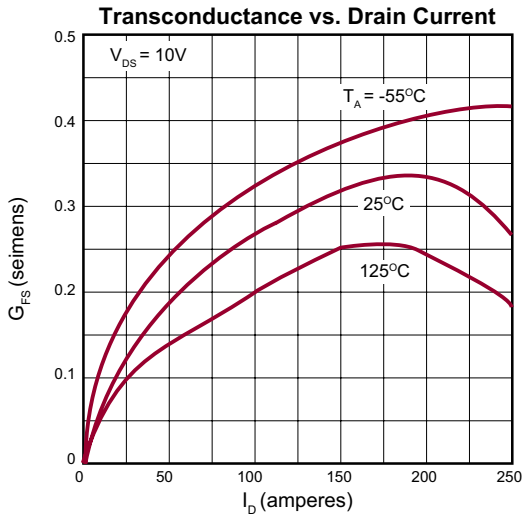
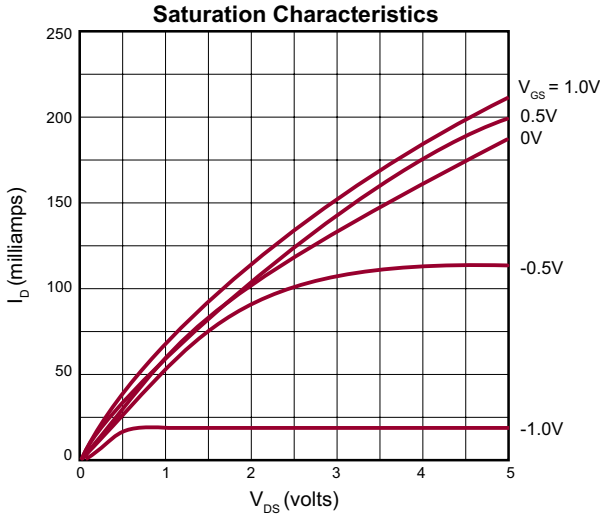
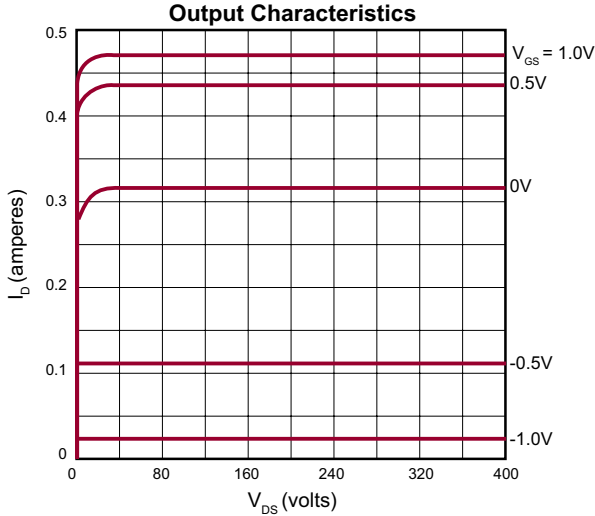
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

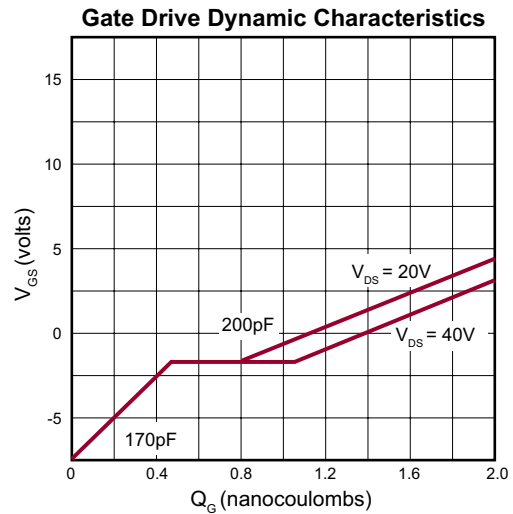
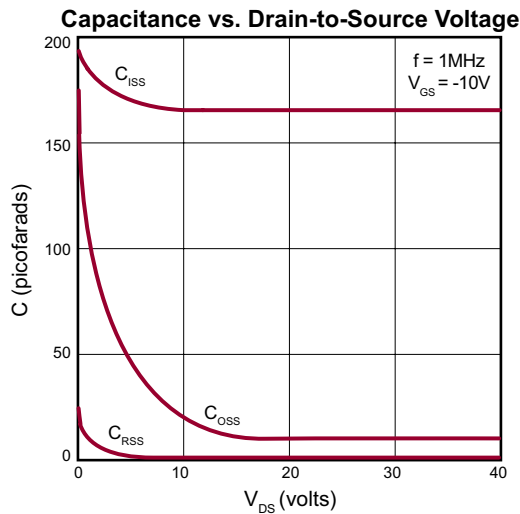
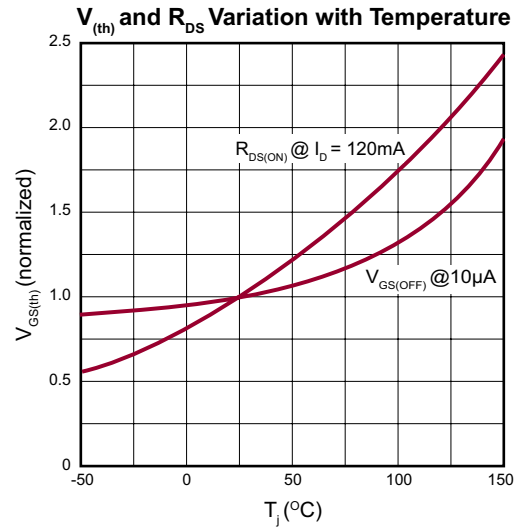
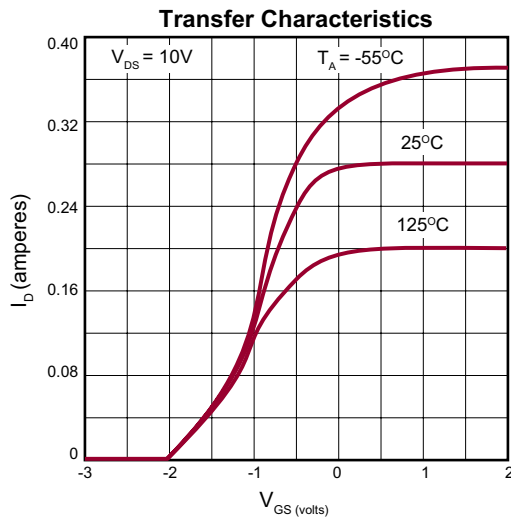
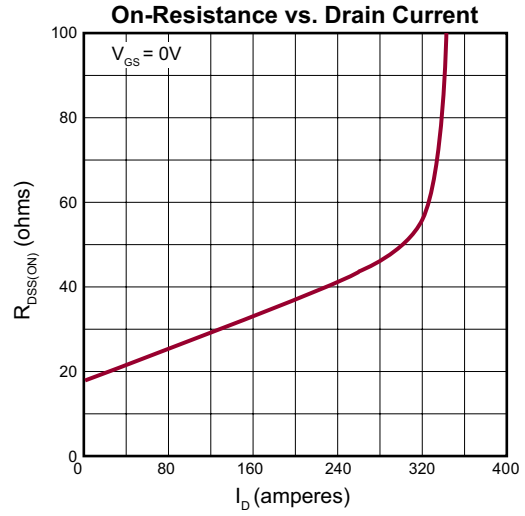
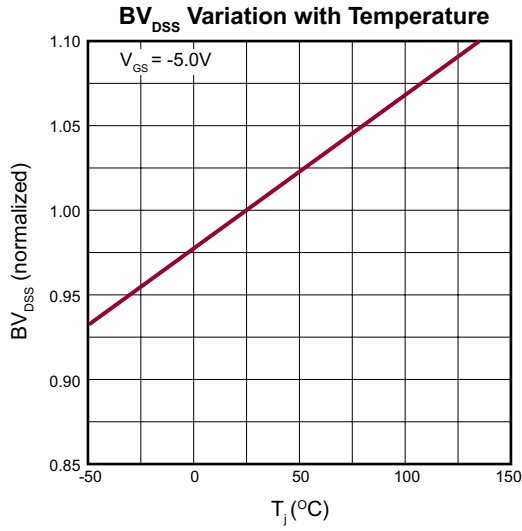
### Switching Waveforms and Test Circuit



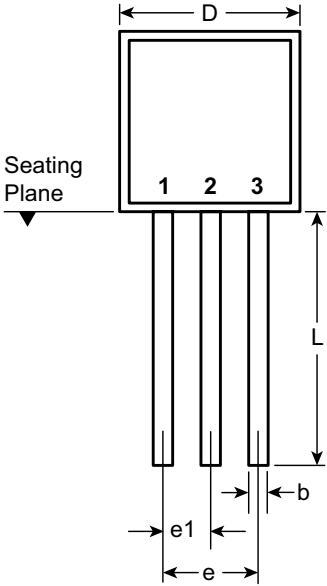
# Typical Performance Curves



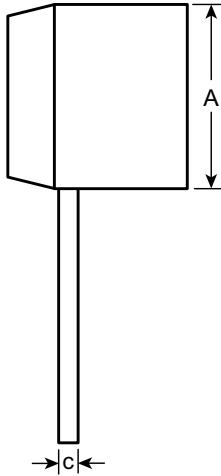
Typical Performance Curves (cont.)



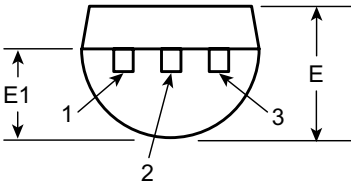
### 3-Lead TO-92 Package Outline (N3)



**Front View**



**Side View**

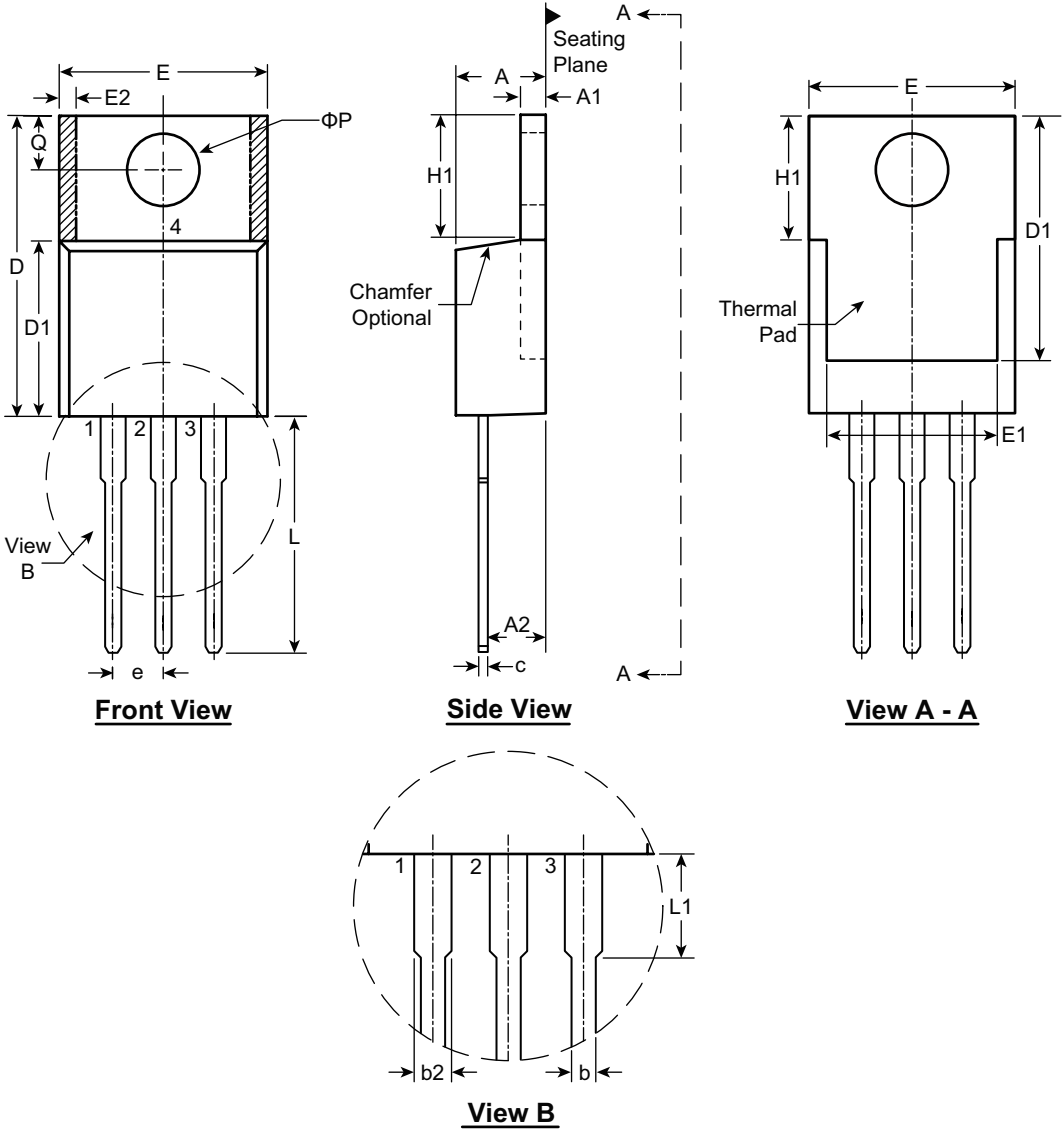


**Bottom View**

Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.  
 \* This dimension is not specified in the JEDEC drawing.  
 † This dimension differs from the JEDEC drawing.  
**Drawings not to scale.**  
 Supertex Doc.#: DSPD-3TO92N3, Version E041009.

# 3-Lead TO-220 Package Outline (N5)



Symbol	A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	$\Phi P$		
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.012 <sup>†</sup>	.560	.326 <sup>†</sup>	.474 <sup>†</sup>	.380	.270	0.20*	.100 BSC	.230	.500	.200*	.100	.139	
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-	-
	MAX	.190	.055	.120 <sup>†</sup>	.040	.070	.024	.650	.361 <sup>†</sup>	.507	.420	.350	.030		-	.270	.580	.250	.135	.161

JEDEC Registration TO-220, Variation AB, Issue K, April 2002.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO220N5, Version C041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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