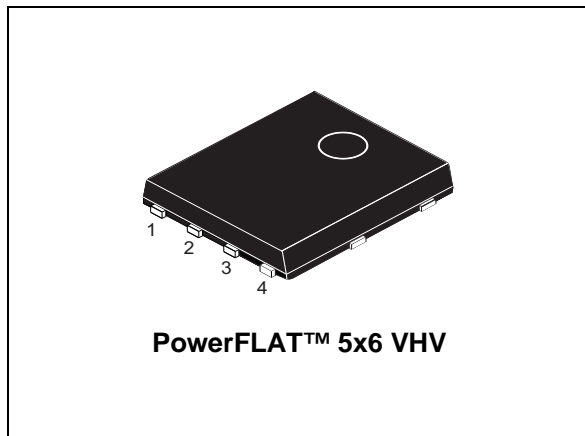
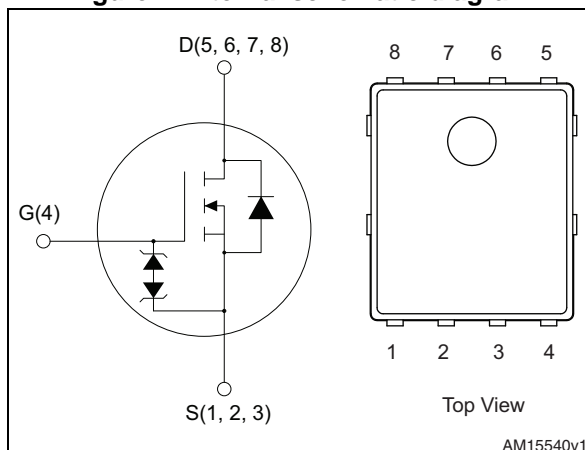


N-channel 800 V, 0.80 Ω typ., 4.5 A Zener-protected SuperMESH™ 5 Power MOSFET in a PowerFLAT™ 5x6 VHV package

Datasheet – production data


Figure 1. Internal schematic diagram


Features

| Order code | V_{DS} | $R_{DS(on)max.}$ | I_D |
|------------|----------|------------------|-------|
| STL8N80K5 | 800 V | 0.95 Ω | 4.5 A |

- Outstanding $R_{DS(on)}$ * area
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener protected

Applications

- Switching applications

Description

This N-channel Zener-protected Power MOSFET is designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|--------------------|---------------|
| STL8N80K5 | 8N80K5 | PowerFLAT™ 5x6 VHV | Tape and reel |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------------|------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ °C}$ | 4.5 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ °C}$ | 3 | A |
| $I_{DM}^{(1),(2)}$ | Drain current (pulsed) | 18 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ °C}$ | 42 | W |
| $I_{AR}^{(3)}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 2 | A |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 114 | mJ |
| $dv/dt^{(5)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(6)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T_{stg} | Storage temperature | - 55 to 150 | °C |
| T_j | Max. operating junction temperature | | °C |

1. The value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_{jmax}
4. Starting $T_j=25\text{ °C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$
5. $I_{SD} \leq 4.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$
6. $V_{DS} \leq 640\text{ V}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|--------------------------------------|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 3 | °C/W |
| $R_{thj-amb}^{(1)}$ | Thermal resistance junction-amb max | 59 | °C/W |

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS} = 0$) | $I_D = 1\text{ mA}$ | 800 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 800\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 800\text{ V}, T_C = 125\text{ °C}$ | | | 50 | μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 3\text{ A}$ | | 0.80 | 0.95 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 450 | - | pF |
| C_{oss} | Output capacitance | | - | 50 | - | pF |
| C_{riss} | Reverse transfer capacitance | | - | 1 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related | $V_{DS} = 0\text{ to }640\text{ V}, V_{GS} = 0$ | - | 57 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related | | - | 24 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}, I_D = 0$ | - | 6 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 640\text{ V}, I_D = 6\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 16) | - | 16.5 | - | nC |
| Q_{gs} | Gate-source charge | | - | 3.2 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 11 | - | nC |

1. $C_{oss\text{ eq}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|--------------|---------------------|---|------|------|-----|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15), (see Figure 20) | - | 12 | - | ns |
| t_r | Rise time | | - | 14 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 32 | - | ns |
| t_f | Fall time | | - | 20 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 4.5 | A |
| I_{SDM} | Source-drain current (pulsed) | | - | | 18 | A |
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD} = 6\text{ A}$, $V_{GS} = 0$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17) | - | 300 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 3 | | μC |
| I_{RRM} | Reverse recovery current | | - | 20 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17) | - | 415 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 3.8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 18 | | A |

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---------------|-------------------------------|--|-----|------|-----|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$, $I_D = 0$ | 30 | - | - | V |

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

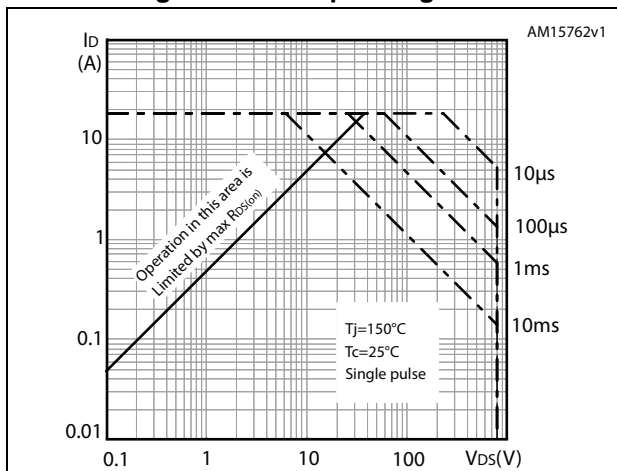


Figure 3. Thermal impedance

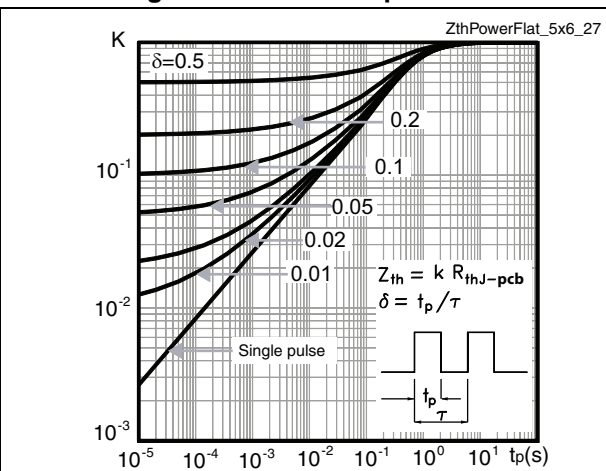


Figure 4. Output characteristics

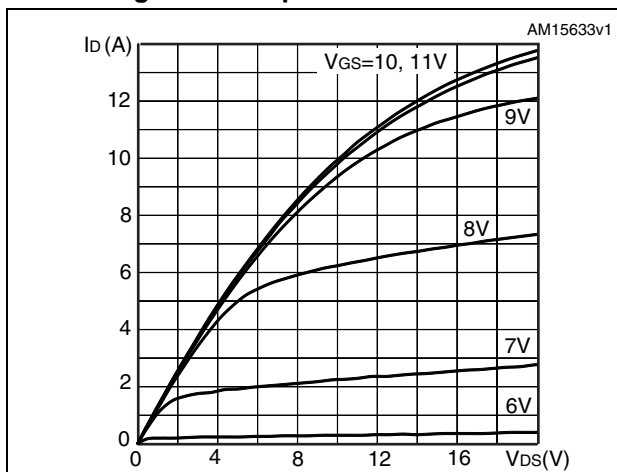


Figure 5. Transfer characteristics

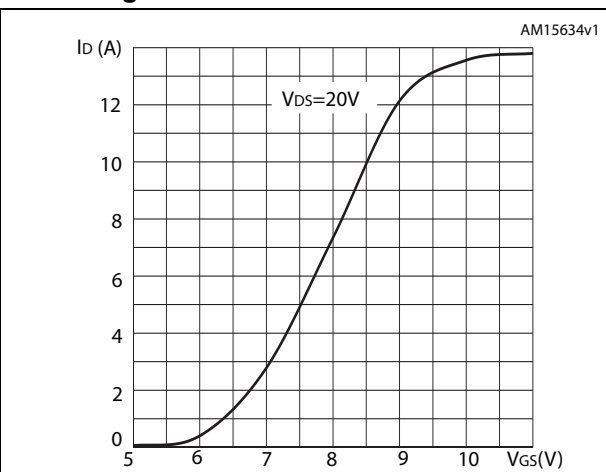


Figure 6. Gate charge vs gate-source voltage

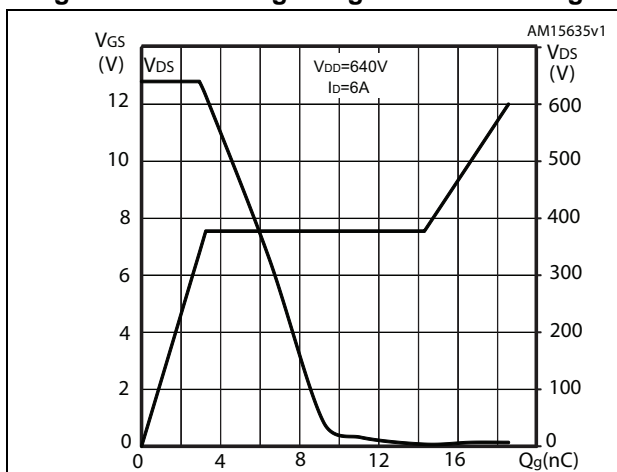


Figure 7. Static drain-source on-resistance

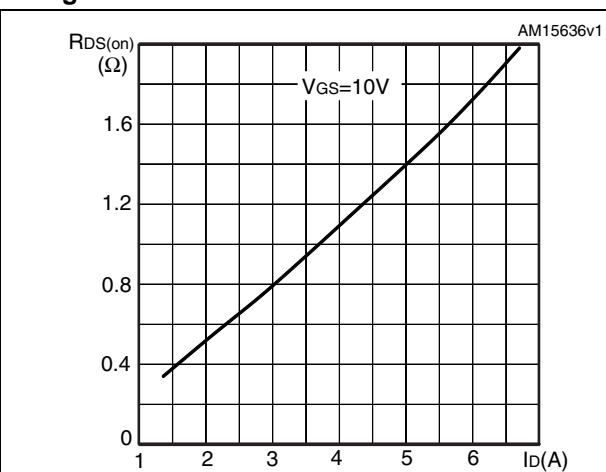


Figure 8. Capacitance variations

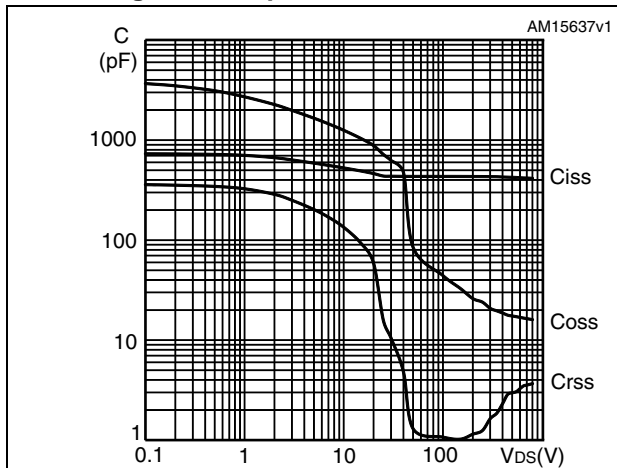


Figure 9. Output capacitance stored energy

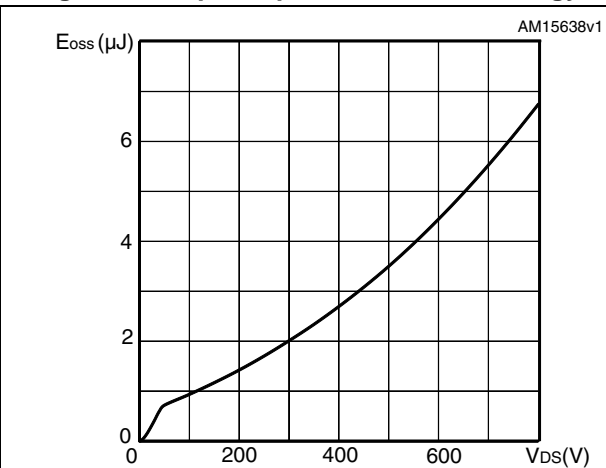


Figure 10. Normalized gate threshold voltage vs. temperature

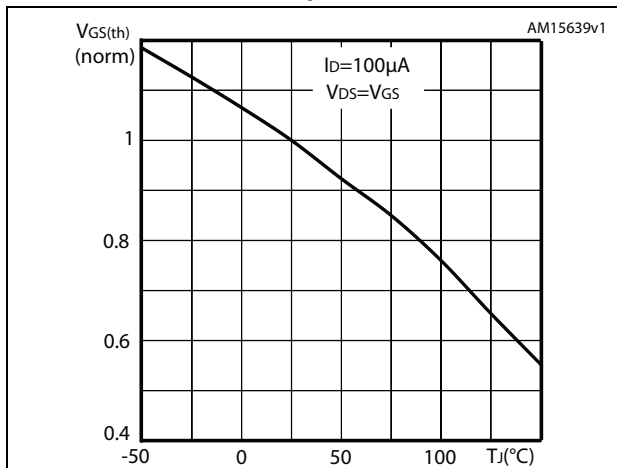


Figure 11. Normalized on-resistance vs. temperature

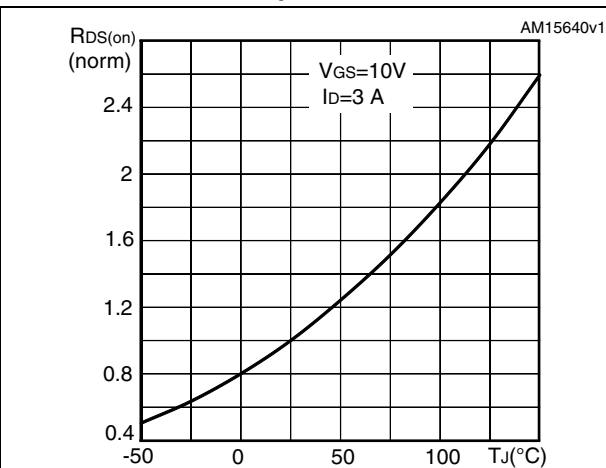


Figure 12. Drain-source diode forward characteristics

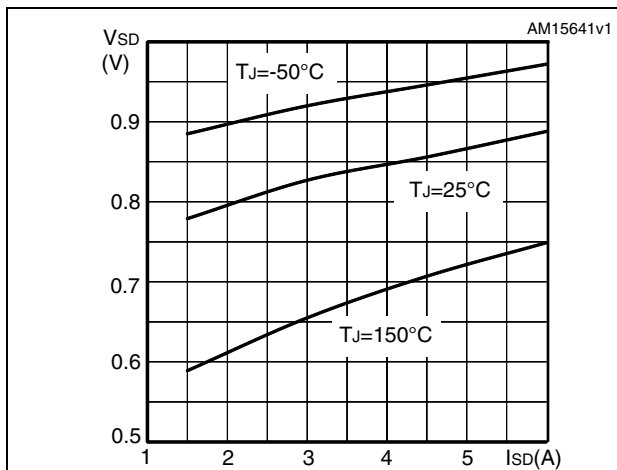


Figure 13. Normalized V_{DS} vs. temperature

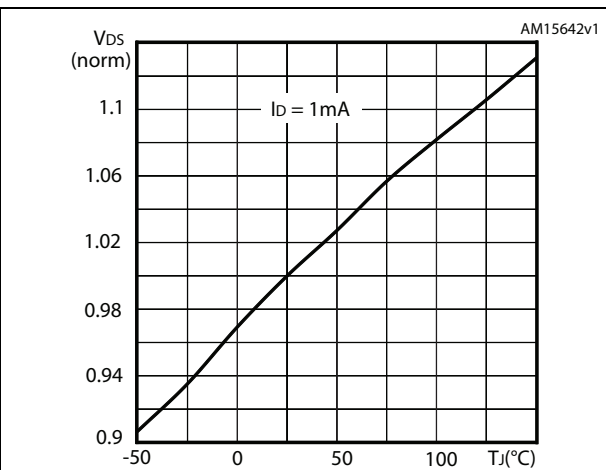
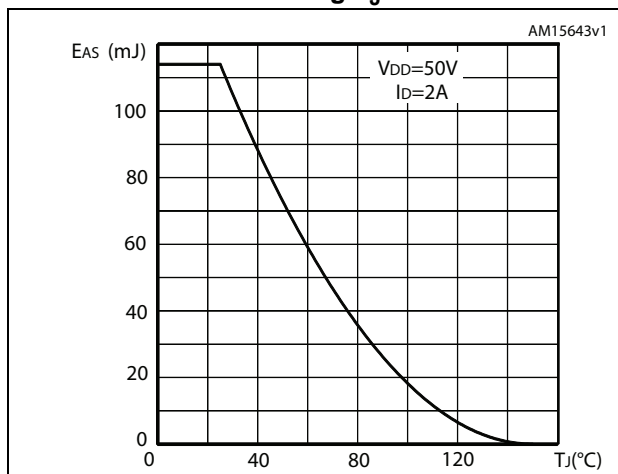


Figure 14. Maximum avalanche energy vs. starting T_J



3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times



Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

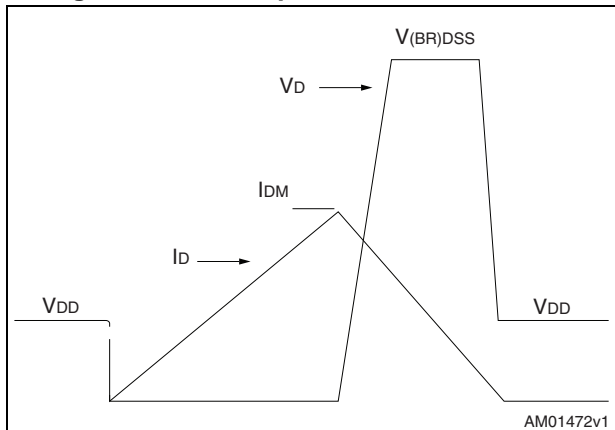
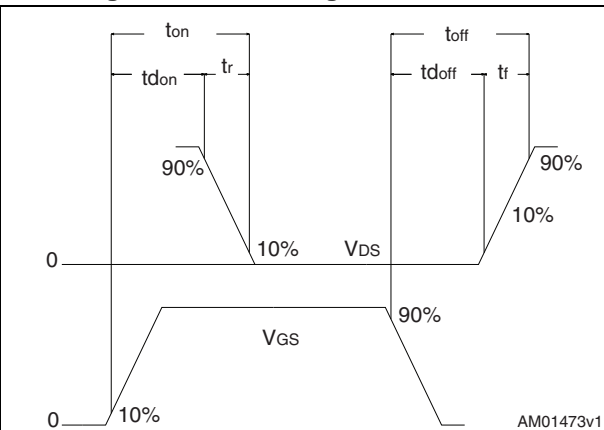


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. PowerFLAT™ 5x6 VHV mechanical data

| DIM | mm. | | |
|-----|------|------|------|
| | min. | typ. | max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.30 | 4.40 | 4.50 |
| E2 | 2.40 | 2.50 | 2.60 |
| e | | 1.27 | |
| L | 0.50 | 0.55 | 0.60 |
| K | 2.60 | 2.70 | 2.80 |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.10 | |
| eee | | 0.10 | |

Figure 21. PowerFLAT™ 5x6 VHV

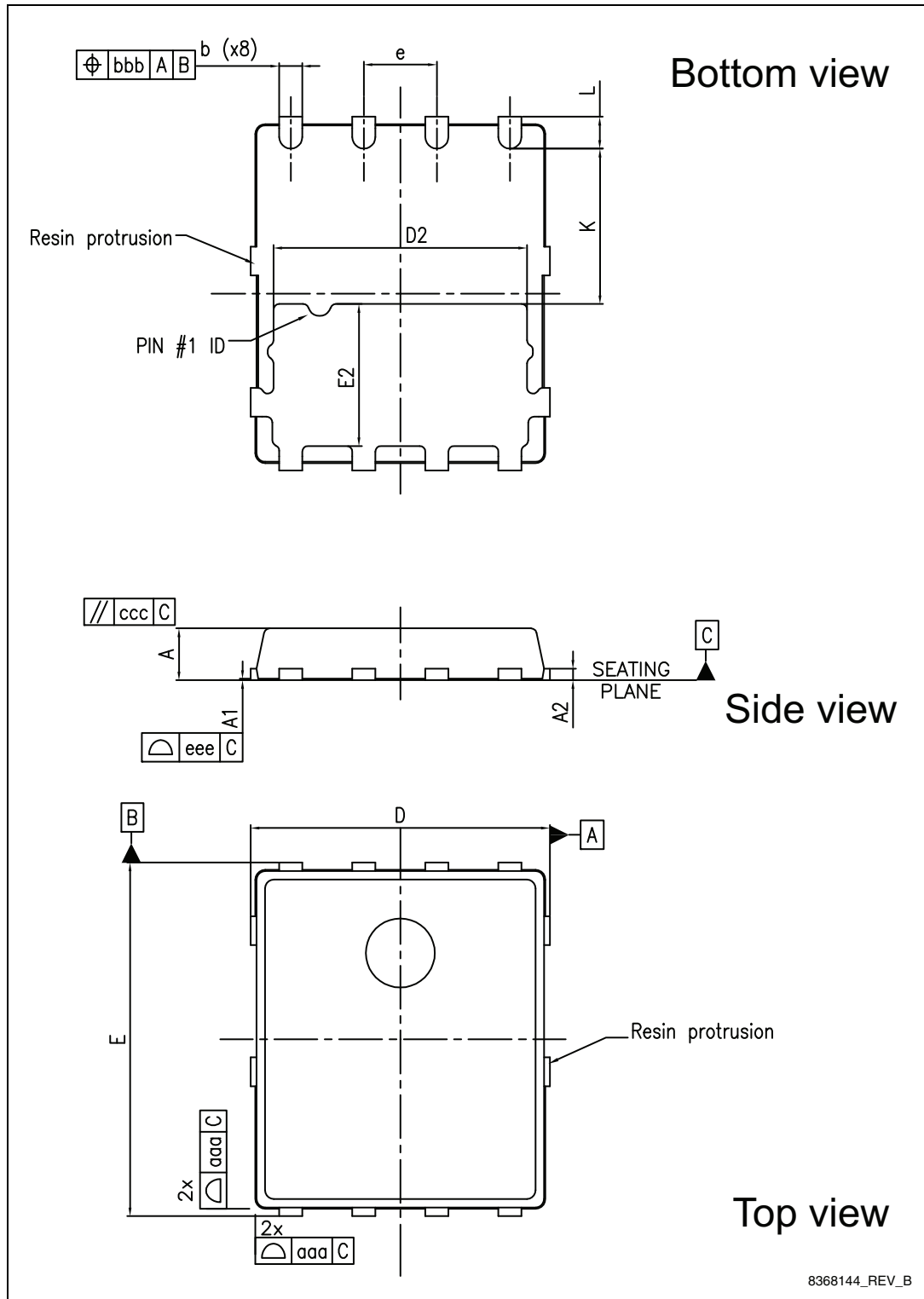
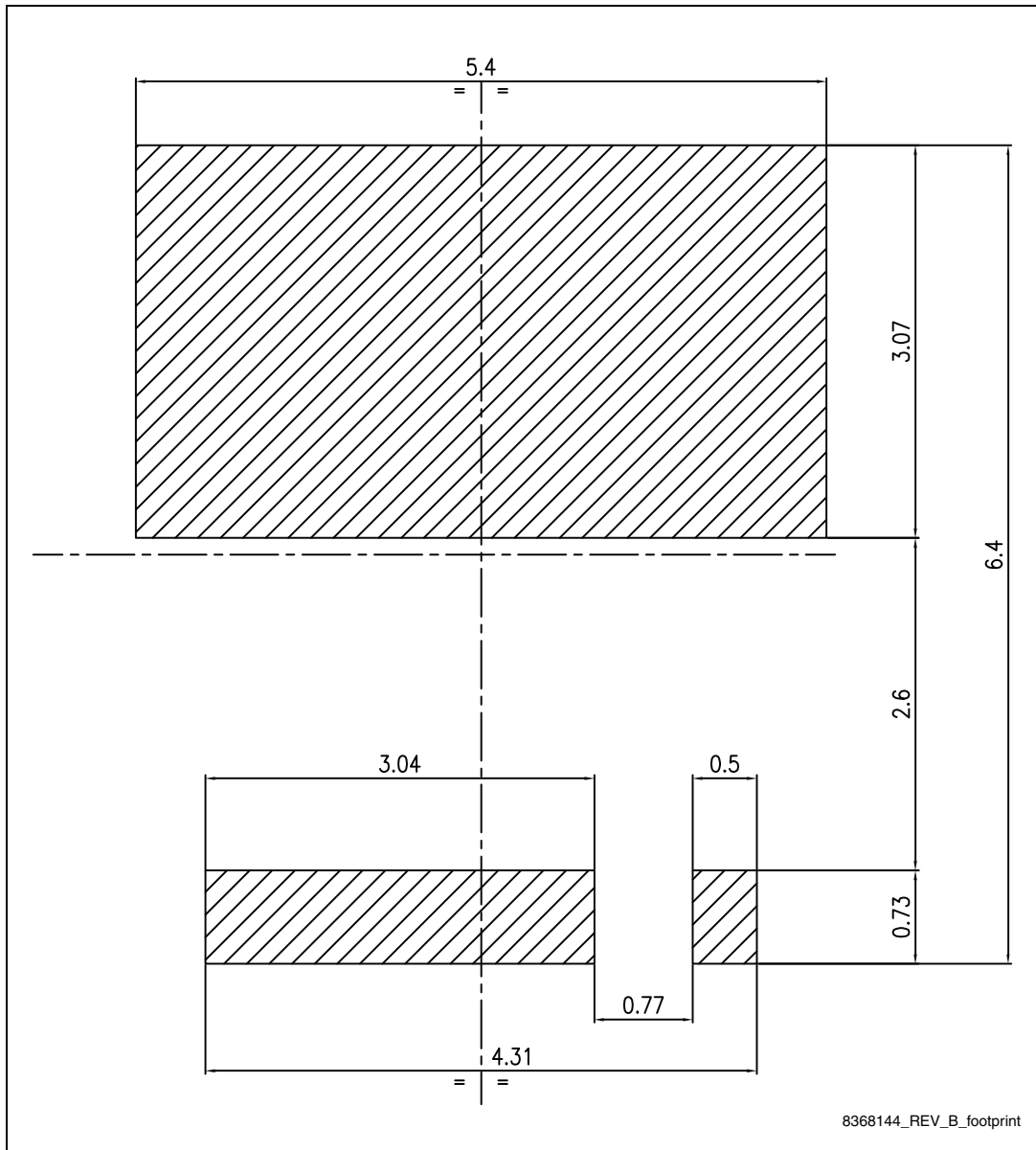


Figure 22. PowerFLAT™ 5x6 VHV (dimensions are in mm)



5 Packaging mechanical data

Figure 23. PowerFLAT™ 5x6 tape

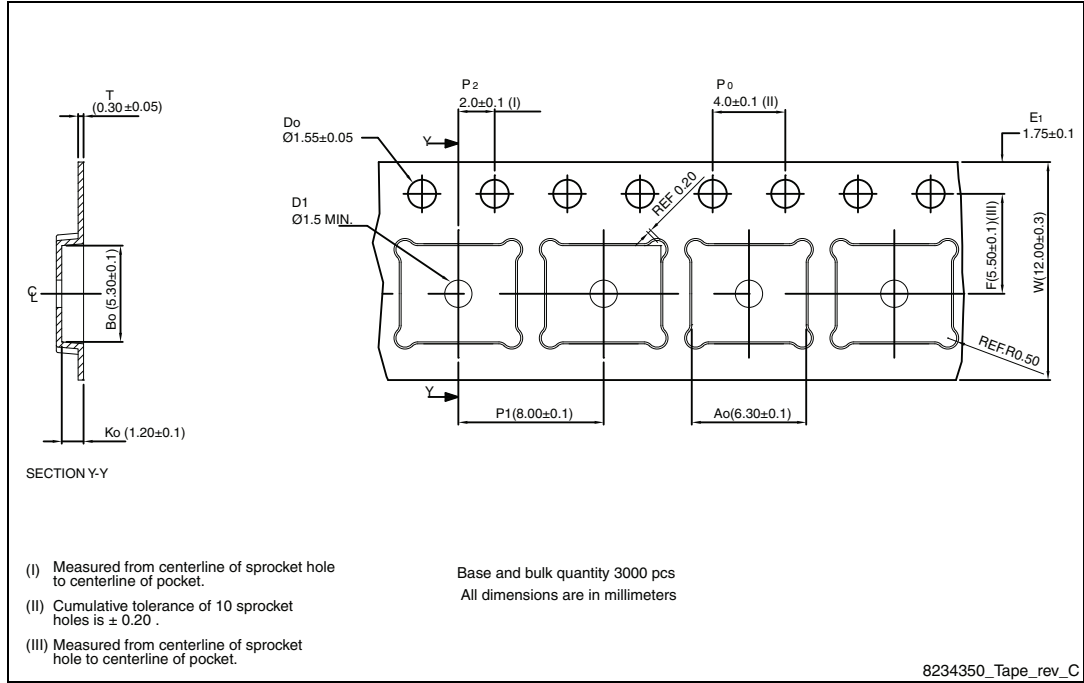


Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape.

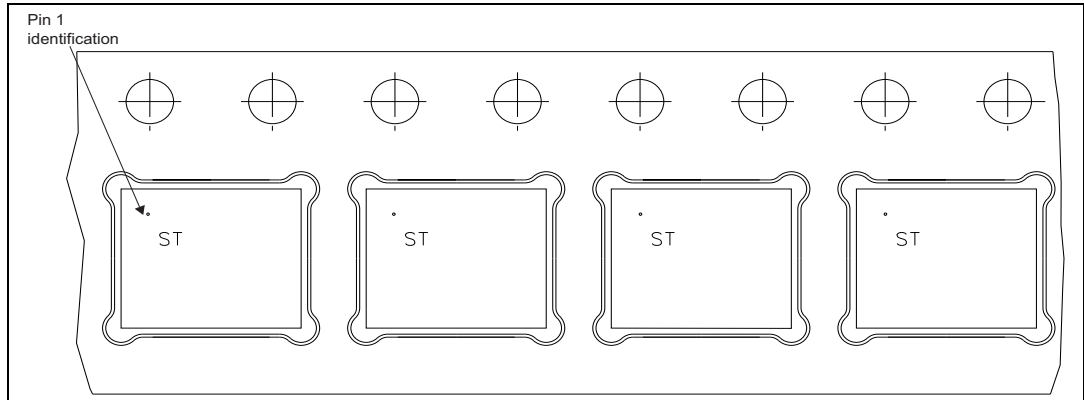
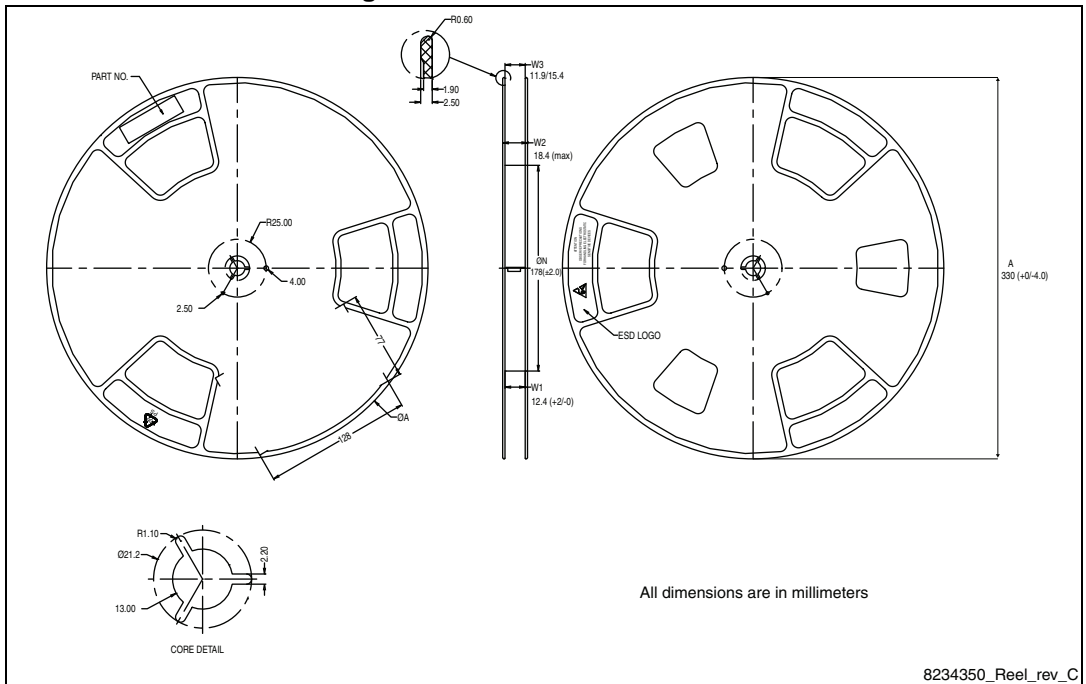


Figure 25. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 18-Dec-2012 | 1 | First release. |
| 22-Apr-2013 | 2 | <ul style="list-style-type: none"> – Deleted: V_{DS}, drain current (continuous) at $T_{amb} = 25\text{ °C}$ and $T_{amb} = 100\text{ °C}$, total dissipation at $T_{amb} = 25\text{ °C}$ in Table 2 – Modified: P_{TOT}, I_{AR} and E_{AS} values in Table 2 – Added: MOSFET dv/dt ruggedness parameter and note 6 in Table 2 – Modified: values in Table 3, $R_{DS(on)}$ typ in Table 4, the entire typical values in Table 5, 6 and 7 – Inserted: Section 2.1: Electrical characteristics (curves) |
| 19-Nov-2013 | 3 | <ul style="list-style-type: none"> – Modified: Figure 3, 15, 16, 17 and 18 – Minor text changes |

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