i705x

General description

The i7050/i7051 limiting amplifiers, with complementary PECL data outputs, are designed for fiber-optic based communication with data rate up to 200 Mbps.

Each device includes a programmable signal-level detector, allowing the user to set
the threshold level at which PECL data outputs are enabled. The hysteresis is fixed internally in 2dB optical to prevent chattering when the signal level is close to the threshold level. The i7050's signal detect outputs are compatible with PECL-logic levels. The i7051 has CMOS signal detect outputs.

STB and JAM can be used to implement a squelch function, which gives fixed logic
levels at data outputs when the input signal is below the programmed threshold level.

Features

- ☐ Programmable chatter-free signal level detector.
- ☐ 1.6 mV input sensitivity (differential).
- ☐ 3.3V to 5V supply voltage.
- ☐ PECL data outputs.
- ☐ PECL signal detect logic interface (i7050).
- ☐ CMOS signal detect logic interface (i7051).
- ☐ Available in SSOP-16 package.