

# BLF2425M8L140; BLF2425M8LS140

Power LDMOS transistor

Rev. 1 — 27 August 2013

Product data sheet

## 1. Product profile

### 1.1 General description

140 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M8L140 and BLF2425M8LS140 are designed for high-power CW applications and are assembled in high performance ceramic packages, available in eared and earless versions

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $I_{Dq} = 1300\text{ mA}$  in a common source class-AB production test circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L(AV)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW	2450	28	140	19	56

### 1.2 Features and benefits

- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

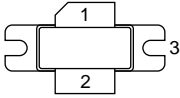
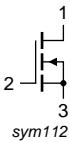
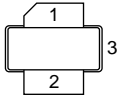
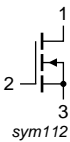
### 1.3 Applications

- Industrial, scientific and medical applications in the frequency range from 2400 MHz to 2500 MHz



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF2425M8L140 (SOT502A)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		
<b>BLF2425M8LS140 (SOT502B)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M8L140	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF2425M8LS140	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	-	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 125\text{ W}$	0.28	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.16\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 216\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	5	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	41	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	500	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 10.8\text{ A}$	-	16	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 7.56\text{ A}$	-	69	-	m $\Omega$

**Table 7. RF characteristics**

Test signal: CW;  $f = 2450\text{ MHz}$ ;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $T_{case} = 25\text{ °C}$  unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 140\text{ W}$	17.5	19	-	dB
$RL_{in}$	input return loss	$P_L = 140\text{ W}$	-	-16	-8	dB
$\eta_D$	drain efficiency	$P_L = 140\text{ W}$	51	56	-	%

## 7. Test information

### 7.1 Ruggedness in class-AB operation

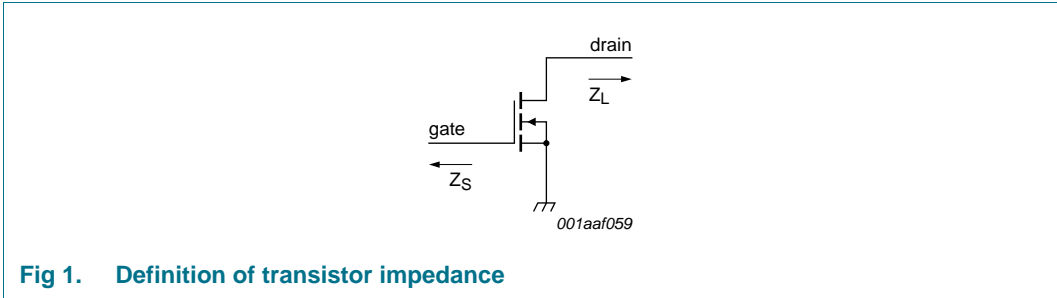
The BLF2425M8L140 and BLF2425M8LS140 are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $P_L = 140\text{ W}$  (CW);  $f = 2450\text{ MHz}$ .

### 7.2 Impedance information

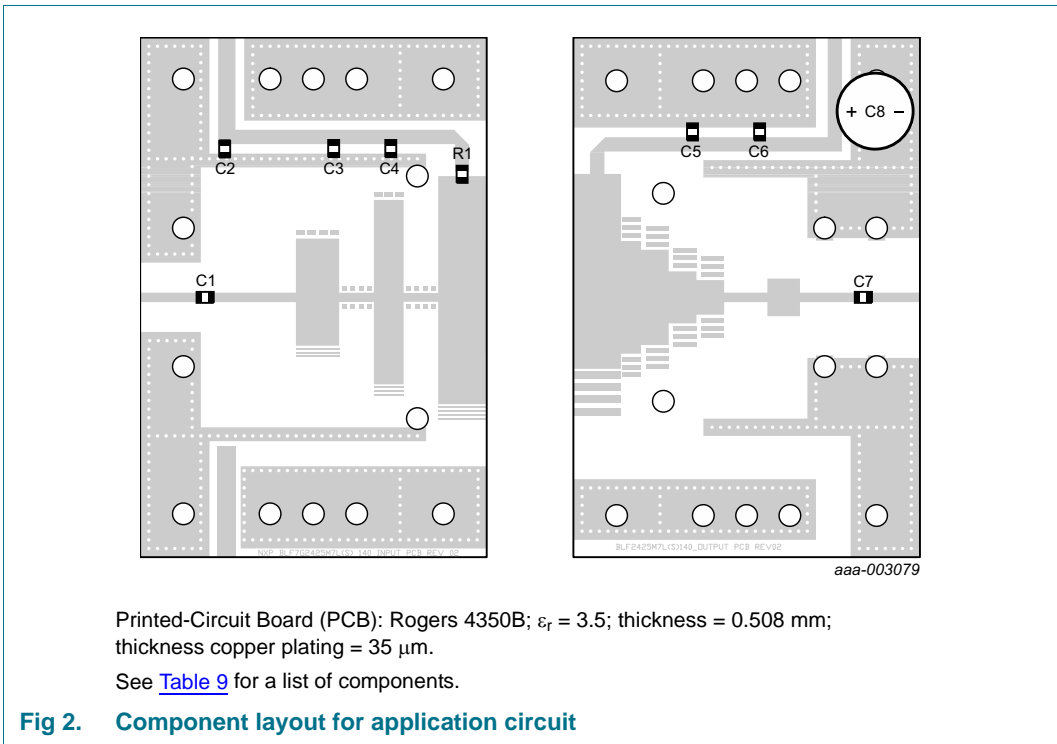
**Table 8. Typical impedance**

Measured load-pull data. Typical values unless otherwise specified.  $I_{Dq} = 1300\text{ mA}$ ;  $V_{DS} = 28\text{ V}$ .  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
2400	$3.7 - 5.4j$	$1.3 - 1.5j$
2450	$6.9 - 5.0j$	$1.5 - 1.6j$
2500	$8.7 - 2.0j$	$1.5 - 1.6j$



**7.3 Circuit information**

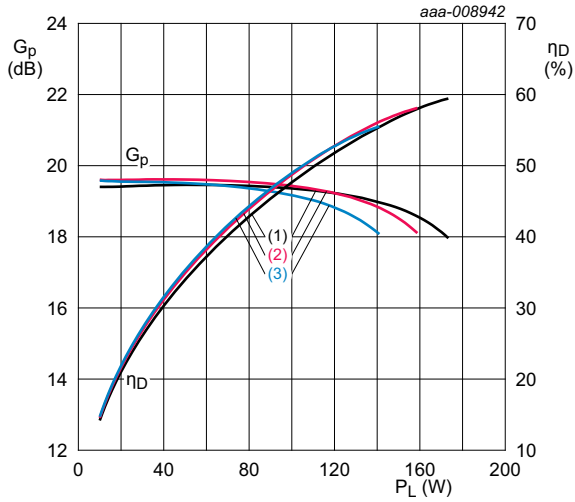


**Table 9. List of components**

For test circuit see [Figure 2](#).

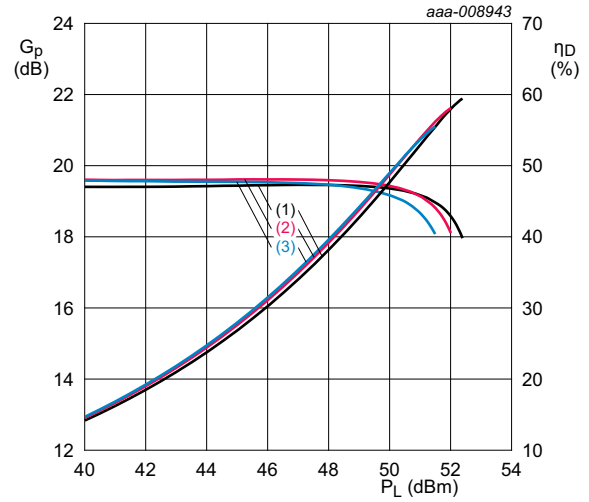
Component	Description	Value	Remarks
C1, C4, C5	multilayer ceramic chip capacitor	15 pF	ATC100B
C2, C6	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	Murata
C3	multilayer ceramic chip capacitor	100 nF	Murata
C7	multilayer ceramic chip capacitor	62 pF	ATC100B
C8	electrolytic capacitor	22 $\mu\text{F}$ , 63 V	
R1	resistor	10 $\Omega$	SMD 0805; Bourns

7.4 Graphical data



$V_{DS} = 28\text{ V}; I_{Dq} = 1300\text{ mA.}$   
 (1)  $f = 2400\text{ MHz}$   
 (2)  $f = 2450\text{ MHz}$   
 (3)  $f = 2500\text{ MHz}$

**Fig 3. Power gain and drain efficiency as function of output power, typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 1300\text{ mA.}$   
 (1)  $f = 2400\text{ MHz}$   
 (2)  $f = 2450\text{ MHz}$   
 (3)  $f = 2500\text{ MHz}$

**Fig 4. Power gain and drain efficiency as function of output power, typical values**

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

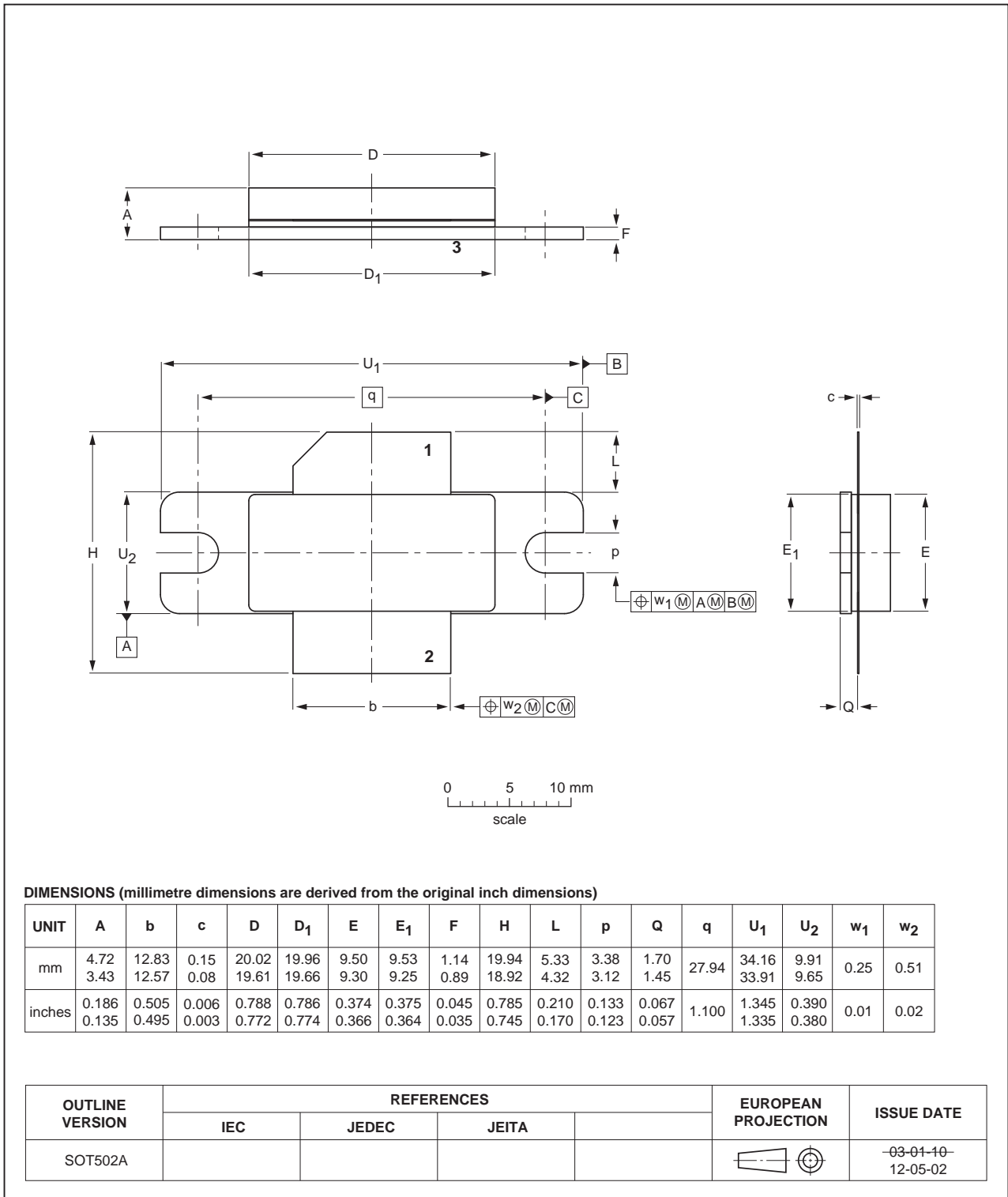


Fig 5. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

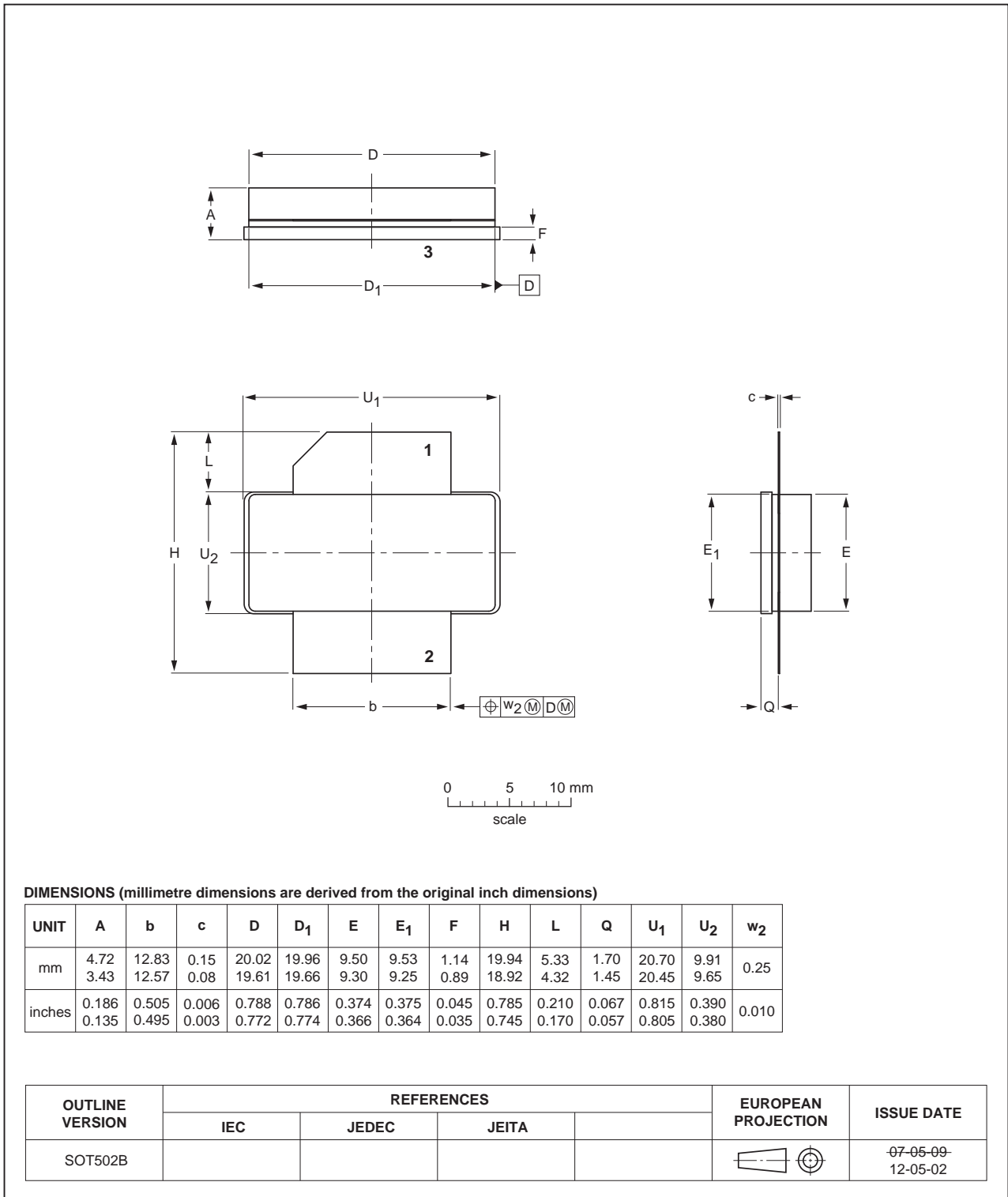


Fig 6. Package outline SOT502B

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M8L140_2425M8LS140 v.1	20130827	Product data sheet	-	-



## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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