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Preliminary Data Sheet

BCM43903

WICED™ IEEE 802.11 b/g/n SoC with an Embedded Applications Processor

GENERAL DESCRIPTION

The Broadcom® Ltd. BCM43903 embedded wireless system-on-a-chip (SoC) is uniquely suited for Internet-of-Things applications. It supports all rates specified in the IEEE 802.11 b/g/n specifications.The device includes an ARM Cortex-based applications processor, a single stream IEEE 802.11n MAC/ baseband/radio, a power amplifier (PA), and a receive low-noise amplifier (LNA). It also supports optional antenna diversity for improved RF performance in difficult environments.

The BCM43903 is an optimized SoC targeting embedded Internet-of-Things applications in the industrial and medical sensor, and home appliance markets. Using advanced design techniques and process technology to reduce active and idle power, the device is designed for embedded applications that require minimal power consumption and a compact size.

The device includes a PMU for simplifying system power topology and allows for direct operation from a battery while maximizing battery life.

FEATURES

Application Processor Features

- ARM Cortex-R4 32-bit RISC processor.
- 1 MB of on-chip SRAM for code and data.
- An on-chip cryptography core
- 640 KB of ROM containing WICED SDK components such as RTOS and TCP/IP stack.
- 17 GPIOs supported.
- Q-SPI serial flash interface to support up to 40 Mbps of peak transfer.
- Support for UART (3), SPI or BSC master, and BSC-only interfaces. (Broadcom Serial Control (BSC) is an I^{2}C-compatible interface.)

FEATURES

Key IEEE 801.11x Features

- IEEE 802.11n compliant.
- Single-stream spatial multiplexing up to 150 Mbps.
- Supports 20 MHz channels with optional SGI.
- Full IEEE 802.11 b/g legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- On-chip power and low-noise amplifiers.
- An internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Integrated ARM Cortex-R4 processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions (to further minimize power consumption while maintaining the ability to upgrade to future features in the field).
- Software architecture supported by standard WICED SDK allows easy migration from existing discrete MCU designs and to future devices.
- Security support:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication.
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility.
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, and CCX 5.0).
  - Wi-Fi Protected Setup and Wi-Fi Easy-Setup
- Worldwide regulatory support: Global products supported with worldwide design approval.

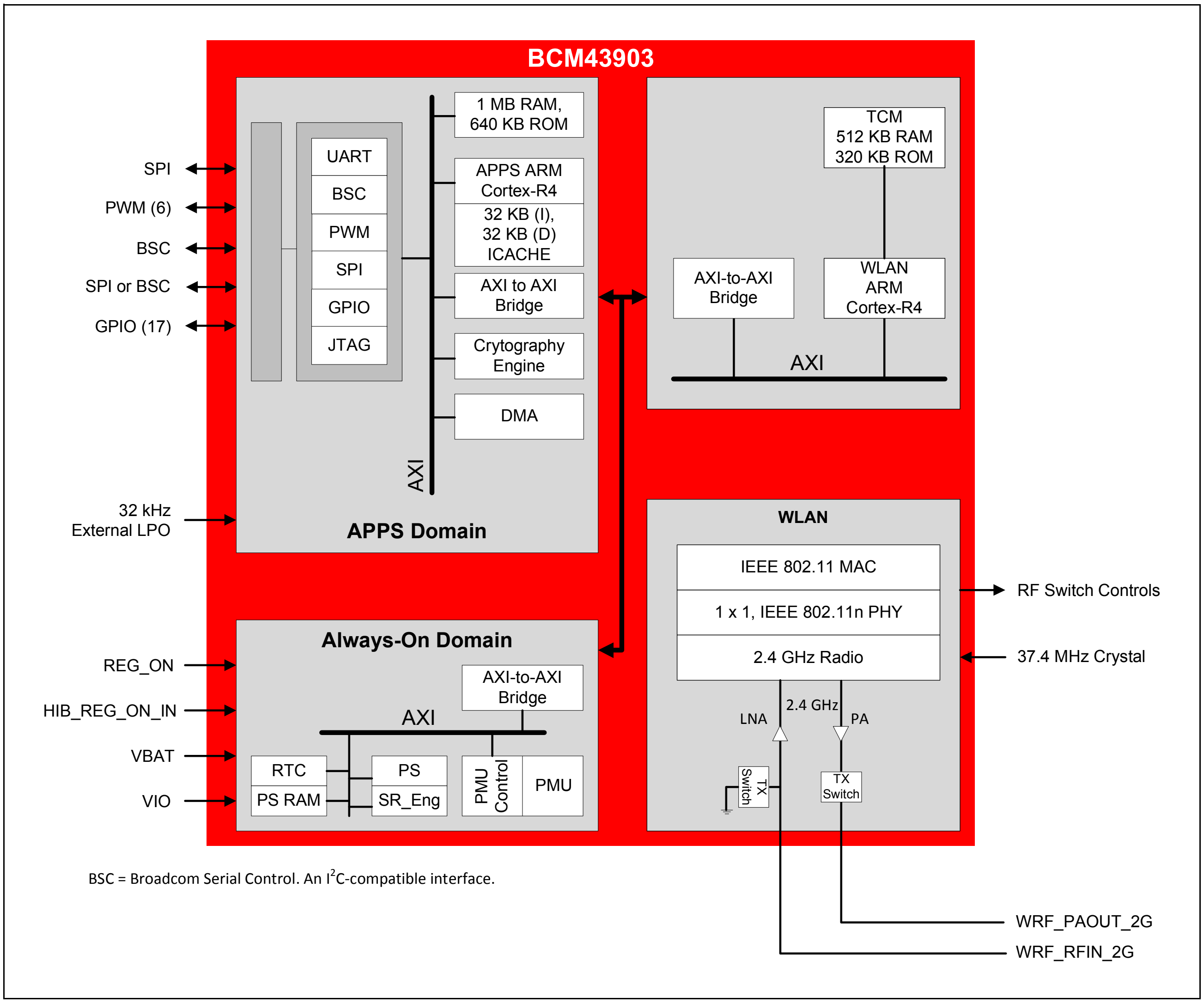
General Features

- Supports battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 6 Kb OTP memory for storing board parameters.
- 151-ball WLBGA (4.91mm x 5.85mm, 0.4mm pitch)

Corporate Headquarters: San Jose, CA

March 12, 2016

Figure 1: Functional Block Diagram



BSC = Broadcom Serial Control. An I^{2}C-compatible interface.

Revision History

Revision	*Date*	*Change Description*
43903-DS102-R	03/12/16	**Updated:** • General edits
43903-DS101-R	11/03/15	**Updated:** • Table 21: “Absolute Maximum Ratings,” on page 109. • Table 24: “Recommended Operating Conditions and DC Characteristics,” on page 111 • Table 30: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 116 • Table 31: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 119.
43903-DS100-R	10/15/2015	Initial release

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® Ltd. BCM43903. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK**, press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

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In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

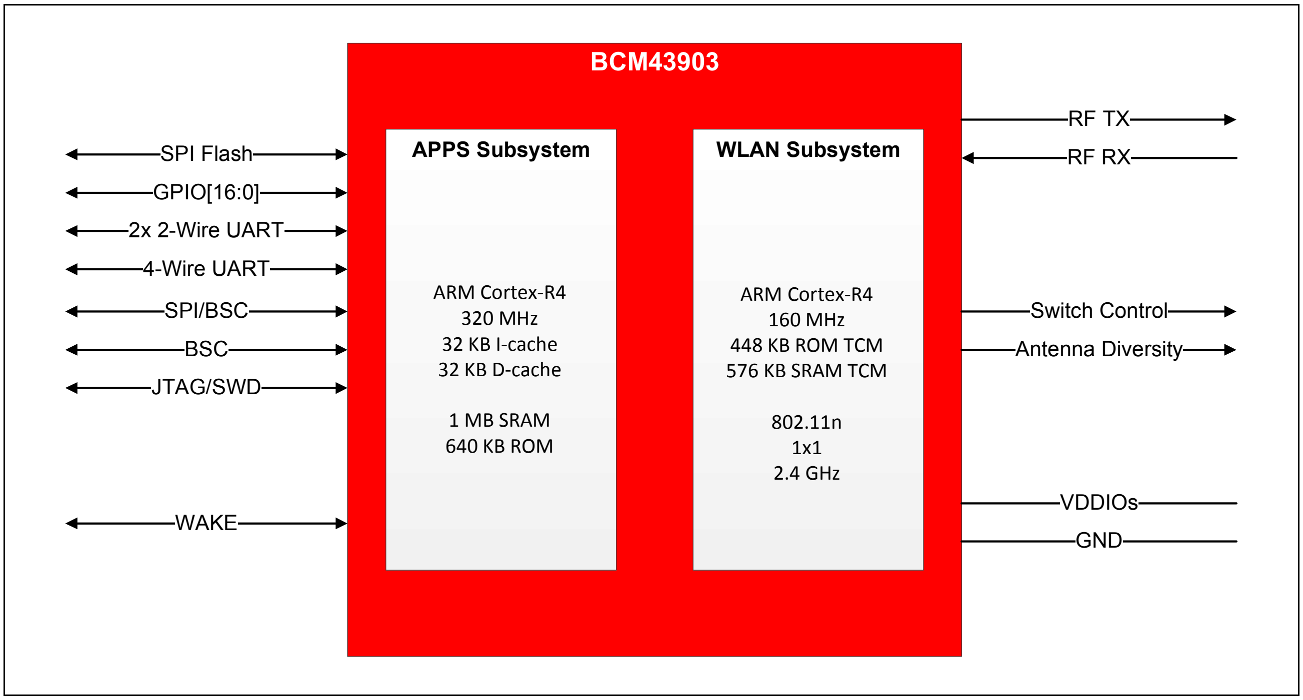
Section 1: Overview

Introduction

The Broadcom Ltd. BCM43903 is a single-chip device that provides the highest level of integration for an embedded system-on-a-chip with integrated IEEE 802.11 b/g/n MAC/baseband/radio and a separate ARM Cortex-R4 applications processor. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for an embedded system with flexibility in size, form, and function. Comprehensive power management circuitry and software ensure that the system can meet the needs of highly embedded systems that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43903 and their associated external interfaces, which are described in greater detail in Section 5: "Applications Subsystem External Interfaces," on page 26.

Figure 2: Block Diagram and I/O



Note: Another SPI interface can be defined by reconfiguring GPIO_8 through GPIO_11 and another BSC interface can be defined by reconfiguring GPIO_12 and GPIO_13 (see Table 10: "Pin Multiplexing," on page 52).

Features

The BCM43903 supports the following features:

- ARM Cortex-R4 clocked at 160 MHz (in 1× mode) or up to 320 MHz (in 2× mode).
- 1 MB of SRAM and 640 KB ROM available for the applications processor.
- One high-speed 4-wire UART interface with operation up to 4 Mbps.
- Two low-speed 2-wire UART interfaces multiplexed on general purpose I/O (GPIO) pins.
- One dedicated BSC[1] interface.

Note: Another BSC interface can be defined by reconfiguring GPIOs. See Table 10: "Pin Multiplexing," on page 52.

- One SPI master/slave interface with operation up to 24 MHz.

Note: In addition to the dedicated BSC interface, the SPI interface can be used as a BSC master interface.

Note: Another SPI interface can be defined by reconfiguring GPIOs. See Table 10: "Pin Multiplexing," on page 52.

- One SPI master interface for serial flash.
- Six dedicated PWM outputs.
- 17 GPIOs.
- IEEE 802.11 b/g/n 1×1 2.4 GHz radio.
- Single- and dual-antenna support.

Standards Compliance

The BCM43903 supports the following standards:

- IEEE 802.11n
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal

---

[1] Broadcom Serial Control (BSC) is an I^2C-compatible interface.

  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC

The BCM43903 supports the following additional standards:

- IEEE 802.11r—Fast Roaming (between APs)
- IEEE 802.11w—Secure Management Frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS enhancements (already supported as per the WMM specification)
  - IEEE 802.11i MAC enhancements
  - IEEE 802.11k radio resource measurement

Section 2: Power Supplies and Power Management

Power Supply Topology

One core buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the BCM43903. All regulators are programmable via the PMU. These blocks simplify power supply design for application and WLAN functions in embedded designs.

A single VBAT (3.0V to 4.8V DC maximum) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM43903.

The REG_ON control signal is used to power up the regulators and take the appropriate sections out of reset. The CBUCK, CLDO, LNLDO, and other regulators power up when any of the reset signals are deasserted. All regulators are powered down only when REG_ON is deasserted. The regulators may be turned off/on based on the dynamic demands of the digital baseband.

The BCM43903 provides a low power-consumption mode whereby the CBUCK, CLDO, and LNLDO regulators are shut down. When in this state, the low-power linear regulator (LPLDO1) supplied by the system VIO supply provides the BCM43903 with all required voltages.

BCM43903 Power Management Unit Features

The BCM43903 supports the following Power Management Unit (PMU) features:

- VBAT to 1.35Vout (550 mA maximum) core buck (CBUCK) switching regulator
- VBAT to 3.3Vout (450 mA maximum) LDO3P3
- 1.35V to 1.2Vout (350 mA maximum) CLDO with bypass mode for deep-sleep
- 1.35V to 1.2Vout (55 mA maximum) LDO for BBPLL
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from the low power-consumption mode.

Figure 3 and Figure 4 on page 16 show the regulators and a typical power topology.

Figure 3: Typical Power Topology (Page 1 of 2)

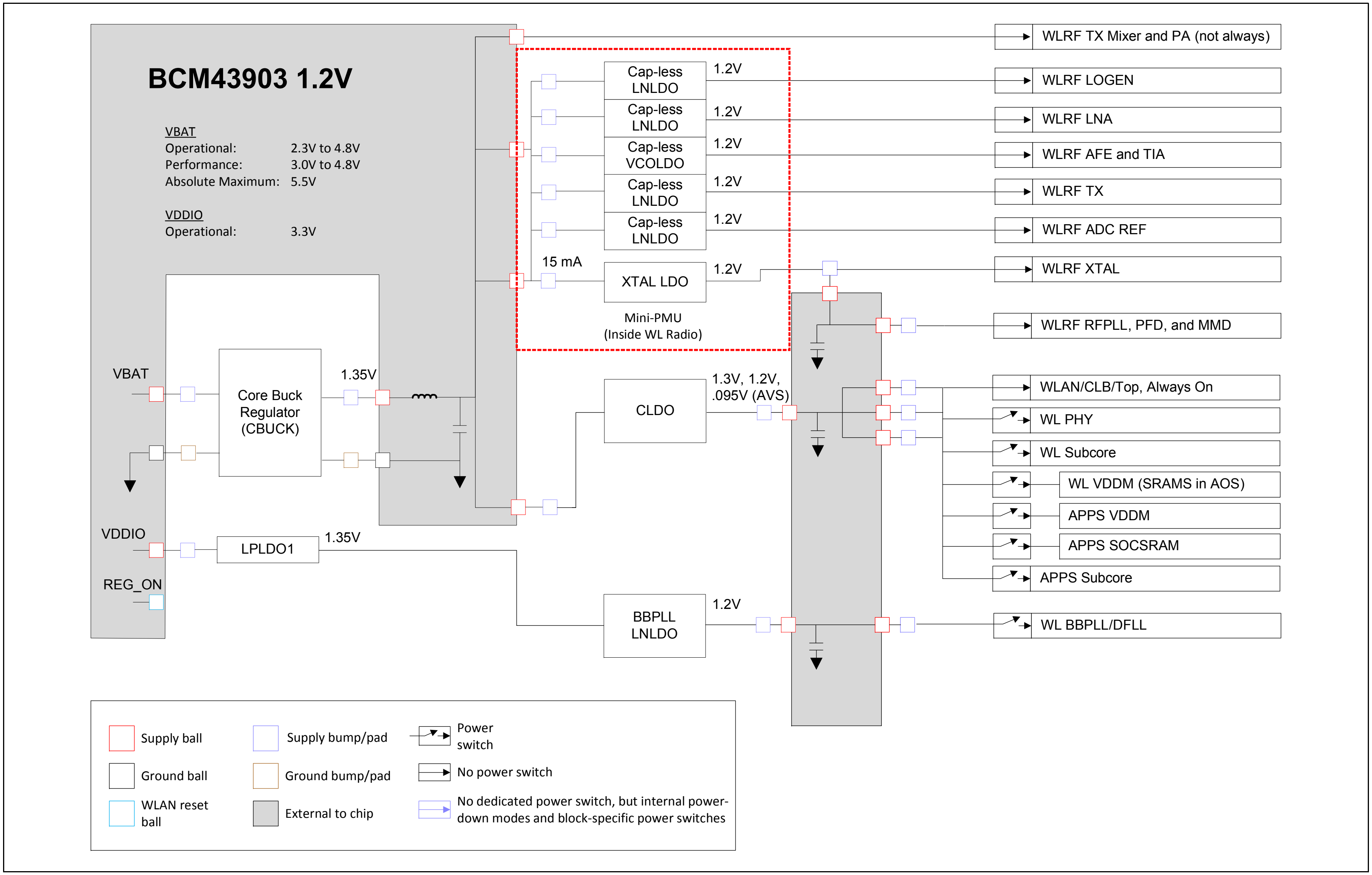
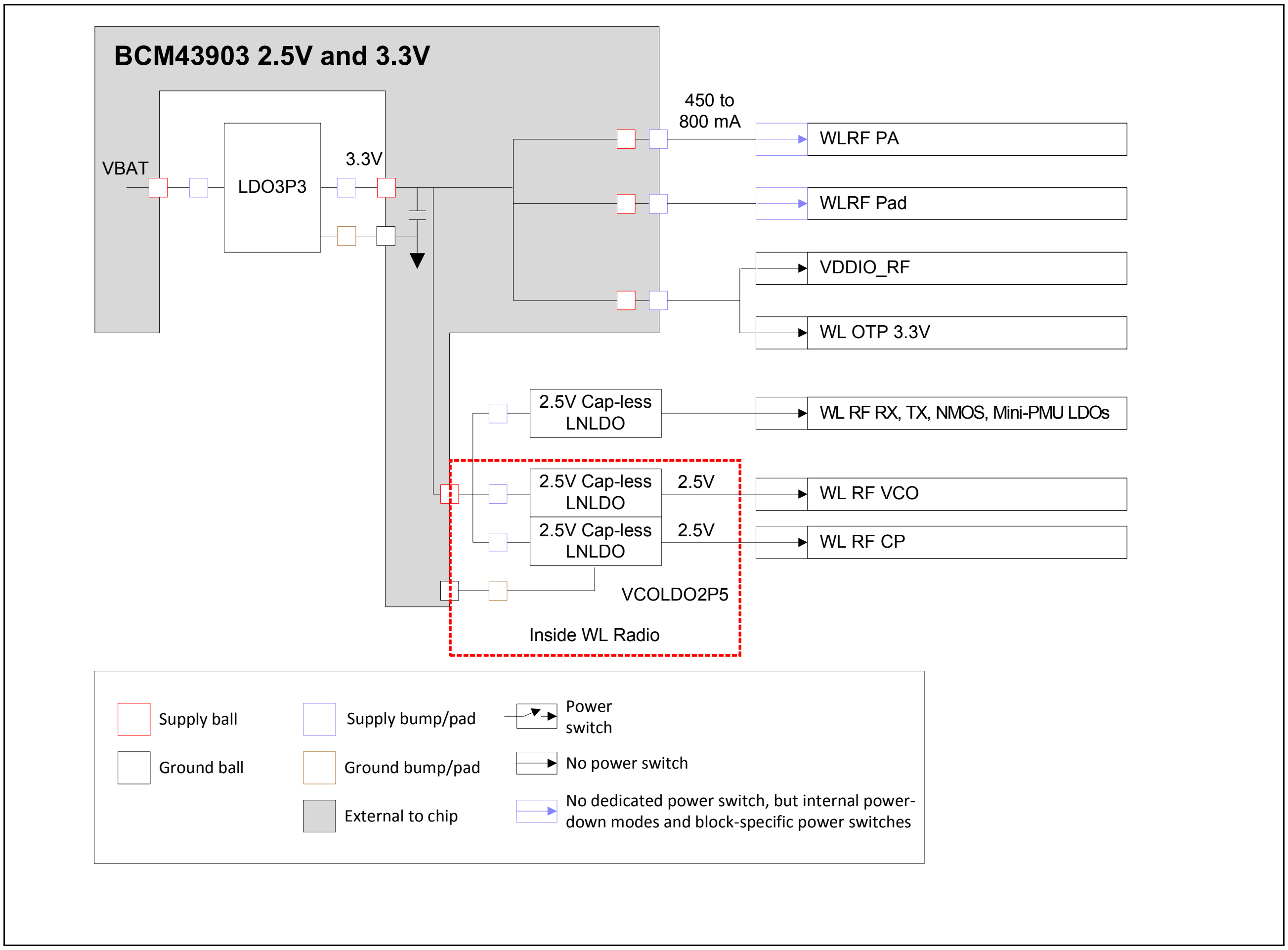


Figure 4: Typical Power Topology (Page 2 of 2)



Power Management

The BCM43903 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43903 includes an advanced Power Management Unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43903 into various power management states appropriate to the environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at a 32.768 kHz LPO clock) in the PMU sequencer are used to turn on and turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) as a function of the mode. Slower clock speeds are used whenever possible.

Table 1 provides descriptions for the BCM43903 power modes.

Table 1: BCM43903 Power Modes

Mode	***Description***
Active	All WLAN blocks in the BCM43903 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
Doze	The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43903 remains powered up in an idle state. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to minimize active power consumption. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
Deep-sleep	Most of the chip, including both analog and digital domains and most of the regulators, is powered off. Logic states in the digital core are saved and preserved in a retention memory in the Always-On domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers or an external interrupt, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
Power-down	The BCM43903 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

PMU Sequencing

The PMU sequencer minimizes system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can come from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource-request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition_on
- transition_off

The timer contains 0 when the resource is enabled or disabled and a nonzero value when in a transition state. The timer is loaded with the time_on or time_off value of the resource after the PMU determines that the resource must be enabled or disabled and decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit of the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, is no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Power-Off Shutdown

The BCM43903 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other system devices remain operational. When the BCM43903 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the BCM43903 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the BCM43903, all outputs are tristated and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM43903 to be fully integrated in an embedded device while taking full advantage of the lowest power-saving modes.

When the BCM43903 is powered on from this state, it is the same as a normal power-up and does not retain any information about its state from before it was powered down.

Power-Up/Power-Down/Reset Circuits

The BCM43903 has two signals (see Table 2) that enable or disable circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 18: “Power-Up Sequence and Timing,” on page 81.

Table 2: Power-Up/Power-Down/Reset Control Signals

Signal	***Description***
REG_ON	This signal is used by the PMU to power up the BCM43903. It controls the internal BCM43903 regulators. When this pin is high, the regulators are enabled and the device is out of reset. When this pin is low, the device is in reset and the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
HIB_REG_ON_IN	This signal is used by the hibernation block to decide whether or not to power down the internal BCM43903 regulators. If HIB_REG_ON_IN is low, the regulators will be disabled. For a signal at HIB_REG_ON_IN to function as intended, HIB_REG_ON_OUT must be connected to REG_ON.

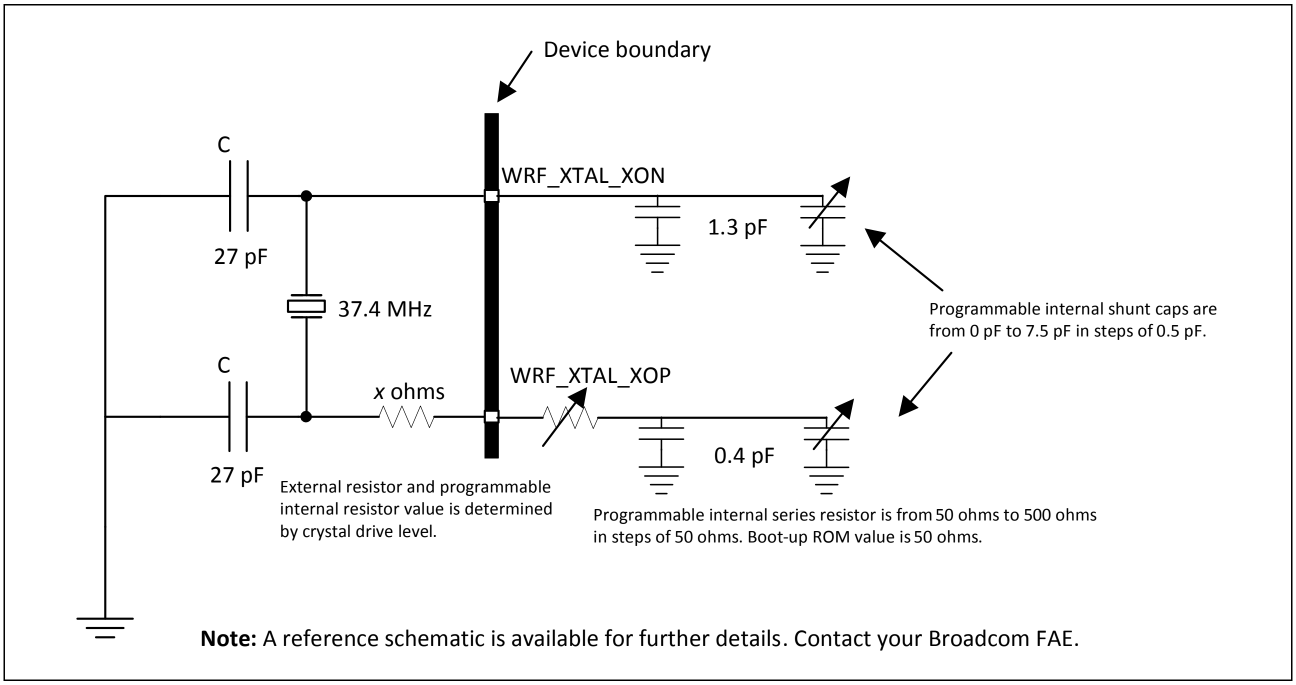
Section 3: Frequency References

An external crystal is used for generating all radio frequencies and normal-operation clocking. As an alternative, an external frequency reference can be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Crystal Interface and Clock Generation

The BCM43903 can use an external crystal to provide a frequency reference. The recommended crystal oscillator configuration, including all external components, is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5: Recommended Oscillator Configuration



Note: A reference schematic is available for further details. Contact your Broadcom FAE.

A fractional-N synthesizer in the BCM43903 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 3 on page 21.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used, provided that it meets the phase noise requirements listed in Table 3.

If used, the external clock should be connected to the WRF_XTAL_XON pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned off when the BCM43903 goes into sleep mode. When the clock buffer turns on and off, there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P35 pin.

Figure 6: Recommended Circuit to Use With an External Reference Clock

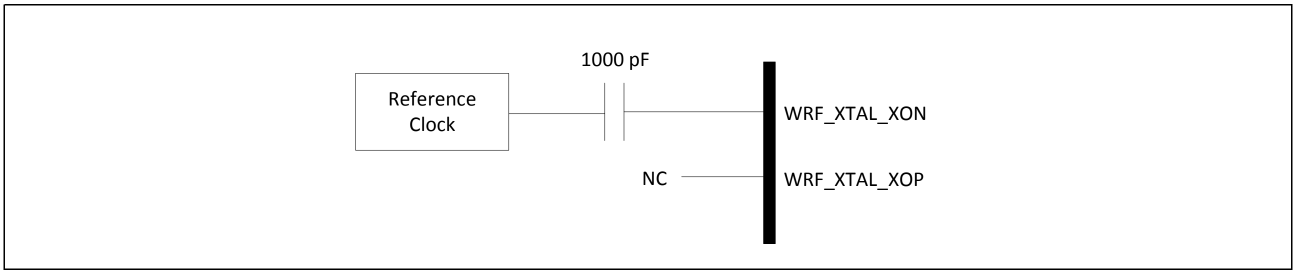


Table 3: Crystal Oscillator and External Clock—Requirements and Performance

		Crystal[a]			*External Frequency Reference*[b c]			
Parameter	***Conditions/Notes***	***Min.***	***Typ.***	***Max.***	***Min.***	***Typ.***	***Max.***	***Units***
Frequency	2.4 GHz band: IEEE 802.11n operation and legacy IEEE 802.11b/g operation	Between 19 MHz and 52 MHz [d]						
Frequency tolerance over the lifetime of the equipment, including temperature[e]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	16	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	μW
Input impedance (WRF_XTAL_XON)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_XON Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_XON Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_XON input voltage (see Figure 6)	IEEE 802.11b/g operation only	–	–	–	400	–	1200	mV_{p-p}

Table 3: Crystal Oscillator and External Clock—Requirements and Performance (Cont.)

Parameter	***Conditions/Notes***	***Crystal***[a]			***External Frequency Reference***[b c]			***Units***
		Min.	***Typ.***	***Max.***	***Min.***	***Typ.***	***Max.***	
WRF_XTAL_XON input voltage (see Figure 6)	IEEE 802.11n AC-coupled analog input	–	–	–	1	–	–	V_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase noise[f] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase noise[f] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz

a. (Crystal) Use WRF_XTAL_XON and WRF_XTAL_XOP.
b. See "External Frequency Reference" on page 21 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. The frequency step size is approximately 80 Hz.
e. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
f. Assumes that external clock has a flat phase noise response above 100 kHz.

Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 19.2, 19.8, 24, 26, 33.6, 37.4, 38.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The BCM43903 must have the reference frequency set correctly in order for any of the external interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Broadcom for more information.

The reference frequency for the BCM43903 may be set in the following ways:

- Set the *xtalfreq=xxxxx* parameter (in Hertz) in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Auto-detect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM43903 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for automatic frequency detection to work correctly, the BCM43903 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 4 on page 23 and is present during a power-on reset.

External 32.768 kHz Low-Power Oscillator

The BCM43903 uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one tradeoff caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 4.

Table 4: External 32.768 kHz Sleep Clock Specifications

Parameter	***LPO Clock***	***Units***
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

[a] When power is applied or switched off.

Section 4: Applications Subsystem

Overview

The Applications subsystem contains the general use CPU, memory, the standalone DMA core, the cryptography core, and the majority of the external interfaces.

Applications CPU and Memory Subsystem

This subsystem has an integrated 32-bit ARM Cortex-R4 processor with an internal 32 KB D-cache and an internal 32 KB I-cache. The ARM Cortex-R4 is a low-power processor that features a low gate count, low interrupt latency, and low-cost debugging capabilities. It is intended for deeply embedded applications that require fast interrupt response features. The ARM Cortex-R4 implements the ARM v7-R architecture and supports the Thumb-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on a MIPS/µW basis. It also supports integrated sleep modes.

Using multiple technologies to reduce cost, the ARM Cortex-R4 enables improved memory utilization, reduced pin overhead, and reduced silicon area. It also has extensive debugging features, including real-time tracing of program execution.

On-chip memory for the CPU includes 1 MB SRAM, 640 KB ROM, and an 8 KB RAM powered independently of the application subsystem.

Memory-to-Memory DMA Core

The BCM43903 memory-to-memory DMA (M2MDMA) engine contains eight DMA channel pairs, each containing one transmit/pull engine and one receive/push engine.

The DMA engine provides general purpose data movement between memories that can be on the device, attached directly to the device, or accessed through a host interface. The transmit/pull engine reads data from the source memory and immediately passes it to the paired receive/push engine, which proceeds to write it to the destination memory. Multiple masters can program the individual channels, and multiple interrupts are provided so that interrupts for different channels can be routed separately to different masters.

Cryptography Core

This core provides general purpose data movement between memories, which may be either on the device, attached directly to the device, or accessed through a host interface. The transmit/pull engine reads data from the source memory and passes it immediately to the paired receive/push engine that proceeds to write it to the destination memory. Multiple masters may program the individual channels, and multiple interrupts are provided so that interrupts for different channels can be routed separately to different masters.

The cryptography block provides a hardware accelerator for enciphering and deciphering data that has undergone processing using standards-based encryption algorithms. The cryptography block includes the following primary features:

- Encryption and hash engines that support single pass AUTH-ENC or ENC-AUTH processing.
- A scalable AES module that supports CBC, ECB, CTR, CFB, OFB, and XTS encryption with 128-, 192-, and 256-bit key sizes.
- A scalable DES module that supports DES and 3DES in ECB and CBC modes.
- An RC4 stream cipher module that supports state initialization, state update, and key-stream generation.
- MD5, SHA1, SHA224, and SHA256 engines that support pure hash or HMAC operations.
- A built-in 512-byte key cache for locally protected key storage.

OTP memory is used to store authentication keys.

Section 5: Applications Subsystem External Interfaces

GPIO

There are 17 general-purpose I/O (GPIO) pins available on the BCM43903. The GPIOs can be used to connect to various external devices.

Upon power-up and reset, these pins are tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions.

Apart from other functions, GPIOs are used to set bootstrap options and use the JTAG interface for debugging during software development.

Broadcom Serial Control

The BCM43903 has two Broadcom Serial Control (BSC[2]) master interfaces for external communication with codecs, DACs, NVRAM, etc. The I/O pads can be configured as pull-ups or pull-ups can be installed on the reference design to support a multimaster on an open drain bus.

JTAG and ARM Serial Wire Debug

The BCM43903 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

The BCM43903 also supports ARM Serial Wire Debug (SWD) for connecting a JTAG debugger directly to both ARM Cortex-R4s. For SWD, the combination of a clock and a bidirectional signal (on a single pin) provides normal JTAG debug and test functionality. The reduced pin-count SWD interface is a high-performance alternative to the JTAG interface.

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[2] Broadcom Serial Control is an I^2C compatible interface.

Table 5 shows the JTAG_SEL and TAP_SEL states for test and debug function selection. Test and debug function selection is independent of the debugging interface (JTAG or SWD) being used.

Table 5: JTAG_SEL and TAP_SEL States for Test and Debug Function Selection

JTAG_SEL State	*TAP_SEL State*	*Test and Debug Function*
0	0	JTAG not used.
0	1	JTAG not used.
1	0	Access the LV tap directly for ATE and bring-up.
1	1	Access either of the ARM Cortex-R4's directly via either the 5-pin JTAG port or the 2-pin SWD configuration.

PWM

The BCM43903 provides up to six independent pulse width modulation (PWM) channels. The following features apply to the PWM channels:

- Each channel is a square wave generator with a programmable duty cycle.
- Each channel generates its duty cycle by dividing down the input clock.
- Both the high and low duration of the duty cycle can be divided down independently by a 16-bit divider register.
- Each channel can work independently or update simultaneously.
- Pairs of PWM outputs can be inverted for devices that need a differential output.
- Continuous or single pulses can be generated.
- The input clock can either be a high-speed clock from a PLL channel or a lower speed clock at the crystal frequency.

Real-Time Clock

The BCM43903 provides a real-time clock (RTC) provided that an accurate 32.768 kHz crystal is used. The RTC generates date/time using the 32.768 kHz reference and is always powered on when the chip is on, except while in Hibernation mode.

The RTC has a precision of seconds and will display the calendar day and time provided the initial start time is programmed correctly. The second, minute, hour, day, month, year, and 24-hour mode can be set individually.

Interrupts can be set on any periodic time event or on specific time events. The PMU uses the RTC interrupt to determine when to wake up the chip.

SPI Flash

The SPI flash interface supports the following features:

- A SPI-compatible serial bus.
- An 80 MHz (maximum) clock frequency.
- Quad I/O, which provides increased throughput to 40 MB/s.
- Support for either ×1 or ×4 addresses with ×4 data.
- 3-bytes and 4-byte addressing modes.
- A configurable dummy-cycle count that is programmable from 1 to 15.
- Programmable instructions output to serial flash.
- An option to change the sampling edge from rising-edge to falling-edge for read-back data when in high-speed mode.

UART

A high-speed 4-wire CTS/RTS UART interface can be enabled by software and has dedicated pins. Provided primarily for debugging during development, this UART enables the BCM43903 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART and provides a FIFO size of 64 × 8 in each direction.

There are two low-speed UART interfaces on the BCM43903. Each functions as a standard 2-wire UART. They are also enabled as alternate functions on GPIOs and can be enabled independently of the 4-wire fast UART.

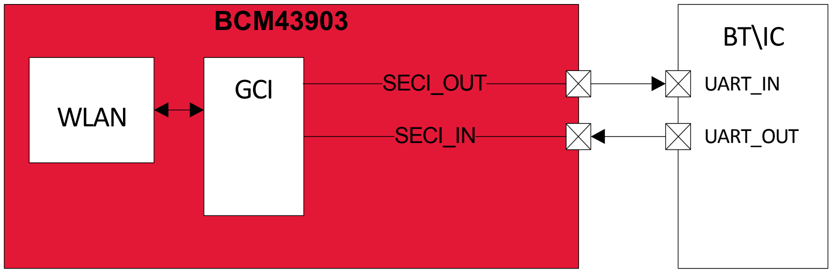
Section 6: Global Functions

External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external colocated wireless device, such as Bluetooth, to manage wireless medium sharing for optimum performance.

Figure 7 shows the coexistence interface.

Figure 7: Broadcom 2-Wire External Coexistence Interface



NOTES:

- SECI_OUT/BT_TXD and SECI_IN/BT_RXD are multiplexed on the GPIOs.
- The 2-wire coexistence interface is intended for future compatibility with the BT SIG 2-wire interface that is being standardized for Core 4.1.

One-Time Programmable Memory

Various hardware configuration parameters can be stored in an internal 6144-bit (768 bytes) One-Time Programmable (OTP) memory that is read by system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP memory device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP memory array can be programmed in a single write-cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits that are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file. The nvram.txt file is provided with the reference board design package.

Hibernation Block

The Hibernation (HIB) block is a self-contained power domain that can be used to completely shut down the rest of the BCM43903. This optional block uses the HIB_REG_ON_OUT pin to drive the REG_ON pin. Therefore, for the HIB block to work as designed, the HIB_REG_ON_OUT pin must be connected to the REG_ON pin. To use the HIB block, software programs the HIB block with a wake count and then asserts a signal indicating that the chip should be put into hibernation. After assertion, the HIB block drives HIB_REG_ON_OUT low for the number of 32 kHz clock cycles programmed as the wake count. After the wake-count timer expires, HIB_REG_ON_OUT is driven high. Other than the logic state of the HIB block, no state is saved in the BCM43903 during hibernation.

System Boot Sequence

The following general sequence occurs after a BCM43903 is powered on:

1. Either REG_ON or HIB_REG_ON_IN is asserted.

Note: For HIB_REG_ON_IN to function as intended, HIB_REG_ON_OUT must be connected to REG_ON.

2. The core LDO (CLDO) and LDO3P3 outputs stabilize.
3. The OTP memory bits are used to initialize various functions, such as PMU trimming, package selection, memory size selection, etc.
4. The APP and WLAN cores are powered up.
5. The XTAL is powered up.
6. The APP and WLAN CPU bootup sequences start.

Section 7: Wireless LAN Subsystem

WLAN CPU and Memory Subsystem

The BCM43903 WLAN section includes an integrated 32-bit ARM Cortex-R4 processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features a low gate count, a small interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than a 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb-2 instruction set.

At 0.19 μW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/μW. It also supports integrated sleep modes.

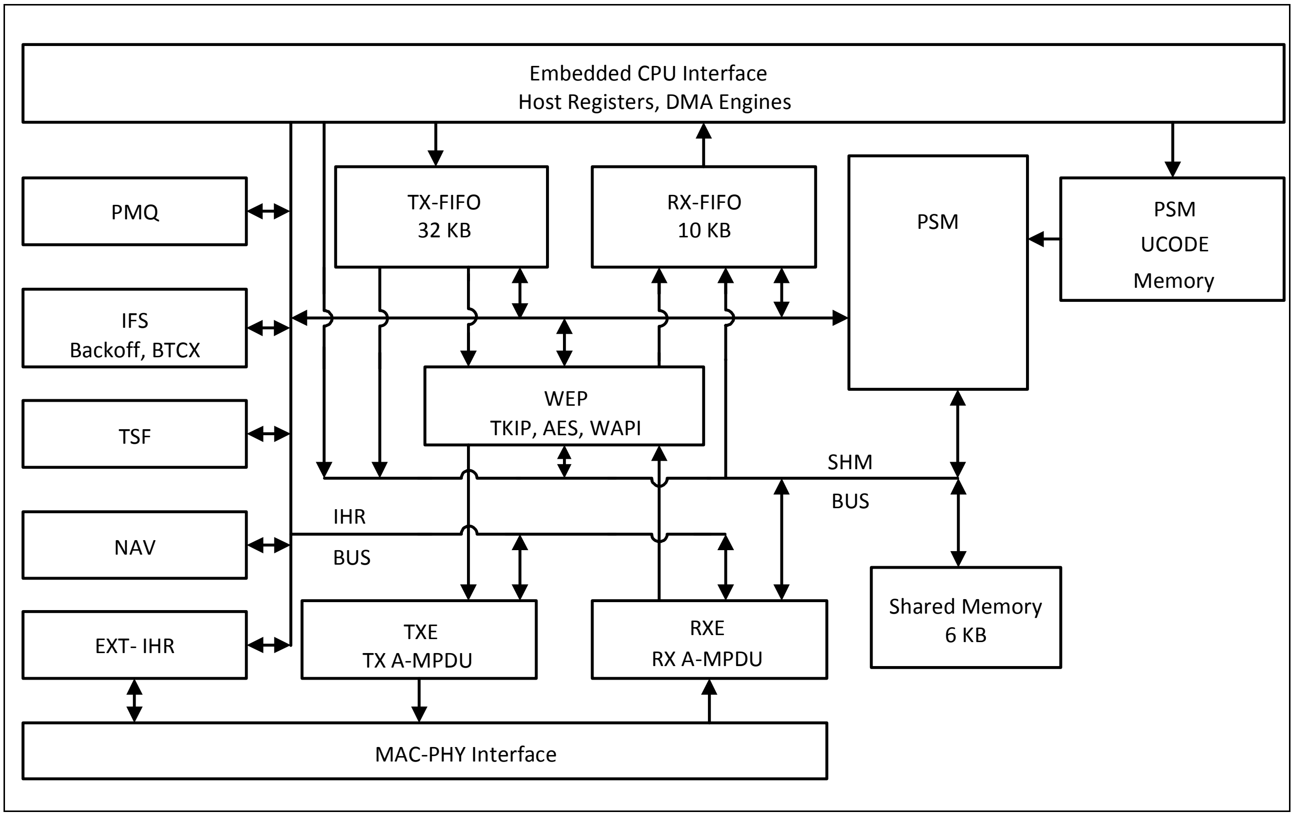
On-chip memory for this CPU includes 576 KB of SRAM and 448 KB of ROM.

IEEE 802.11n MAC

The BCM43903 WLAN media access controller (MAC) is designed to support high-throughput operation with low power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 8.

The following sections provide an overview of the important MAC modules.

Figure 8: WLAN MAC Architecture



The BCM43903 WLAN MAC supports features specified in the IEEE 802.11 base standard and amended by IEEE 802.11n. The key MAC features include:

- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT).
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP), and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality.
- Statistics counters for MIB support.

PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware in order to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, allowing algorithms to be optimized very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are colocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratch-pad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform encryption and decryption as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to use. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with the WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel-access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC has multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe-space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe-spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. When the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface that can be controlled either by the host or the PSM to configure and control the PHY.

IEEE 802.11™ b/g/n PHY

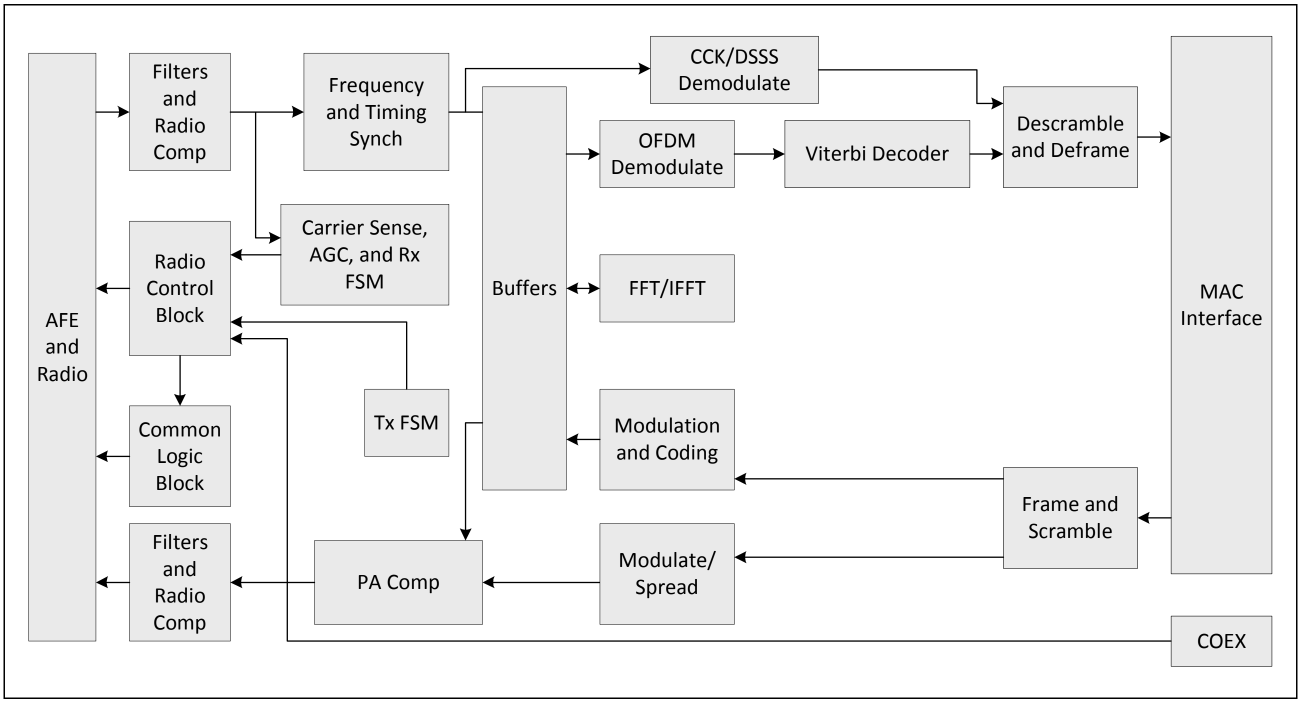
The BCM43903 WLAN digital PHY complies with IEEE 802.11b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 433.3 Mbps for low-power, high-performance, handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of filters, FFTs, and Viterbi-decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sensing and rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier-sensing algorithm provides high throughput for IEEE 802.11b/g hybrid networks with Bluetooth coexistence.

The key PHY features include:

- Programmable data rates from MCS0–7 in 20 MHz channels.
- Support for Optional Short GI and Green Field modes in TX and RX.
- TX and RX LDPC for improved range and power efficiency.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Support for IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power consumption and enhanced sensitivity, range, and reliability.
- Algorithms to improve performance in the presence of externally received Bluetooth signals.
- An automatic gain control scheme for blocking and nonblocking cellular applications.
- Closed loop transmit power control.
- Digital RF chip calibration algorithms to handle CMOS RF chip process, voltage, and temperature (PVT) variations.
- On-the-fly channel frequency and transmit power selection.
- Per-packet RX antenna diversity.
- Available per-packet channel quality and signal-strength measurements.
- Compliance with FCC and other worldwide regulatory requirements.

Figure 9: WLAN PHY Block Diagram



Section 8: WLAN Radio Subsystem

The BCM43903 includes an integrated WLAN RF transceiver that has been optimized for use in 2.4 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Ten RF control signals are available to drive external RF switches. See the reference board schematics for more information.

A block diagram of the radio subsystem is shown in Figure 10 on page 39. Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

Receiver Path

The BCM43903 has a wide dynamic range, direct conversion receiver that employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The 2.4 GHz path has a dedicated on-chip low-noise amplifier (LNA).

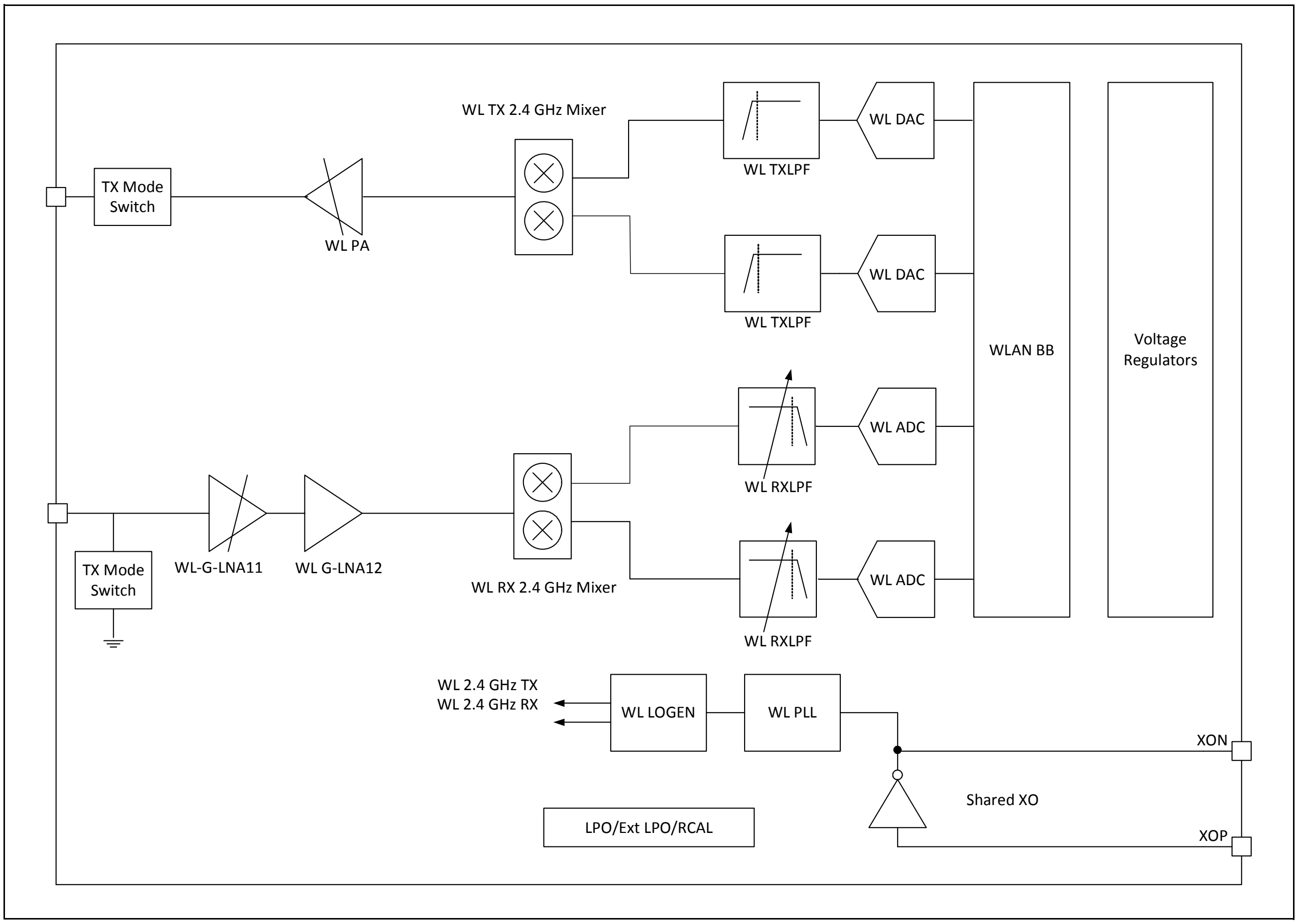
Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. Linear on-chip power amplifiers deliver high output powers while meeting IEEE 802.11b/g/n specifications without the need for external PAs. When using the internal PA, which is required in the 2.4 GHz band, closed-loop output power control is completely integrated.

Calibration

The BCM43903 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically during the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q calibration and VCO calibration are performed on-chip. No per-board calibration is required during manufacturing testing. This helps to minimize the test time and cost in large-volume production environments.

Figure 10: Radio Functional Block Diagram



Section 9: Pinout and Signal Descriptions

Ball Map

Figure 11: 151-Ball WLBGA Map—Top View with Balls Facing Down

	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
12		VDDIO	RF_SW_CTRL_8	RF_SW_CTRL_7	PWR_GND	NC_J12	NC_H12	GPIO_3	GPIO_6	VOUT_3P3	LDO_VDDBAT5V	LDO_VDD1P5	SR_VDDBAT5V	SR_PVSS	12
11	SRSTN	RF_SW_CTRL_9	VSSC	RF_SW_CTRL_1	VSSC	NC_J11	VDDC	NC_G11	GPIO_5	VDDIO	VOUT_LNLDO	VOUT_HSICLDO	VOUT_CLDO	SR_VLX	11
10	JTAG_SEL	NC_N10	RF_SW_CTRL_5	VDDC	RF_SW_CTRL_6	NC_J10	VSSC	GPIO_2	GPIO_4	VDDIO	VSSC	PMU_AVSS	VOUT_CLDO_SENSE	WL_REG_ON	10
9	RF_SW_CTRL_2	RF_SW_CTRL_3	RF_SW_CTRL_0	RF_SW_CTRL_4	VDDIO_RF	VSSC	NC_H9	VSSC	VSSC	VDDIO	GPIO_8	VSSC	I2C0_SDATA	VDDC	9
8	OTP_VDD3P3	AVDD1P2	LPO_XTAL_IN	VSSC	VDDIO_RF	VDDIO			VSSC	GPIO_13	VSSC	I2C0_CLK	UART0_TXD	VDDIO	8
7	WRF_XTAL_XON	WRF_XTAL_GND1P2	AVSS	VDDC	VDDIO		VDDC	VSSC			VSSC	UART0_RXD	UART0_RTS	UART0_CTS	7
6	WRF_XTAL_XOP	WRF_XTAL_VDD1P35	WRF_XTAL_VDD1P2	WRF_SYNTH_VDD3P3	VDDC	VSSC		VDDC	VSSC	SPI0_CS		GPIO_12	SPI0_SISO	SFL_CS	6
5	WRF_PMU_VDD1P35	WRF_SYNTH_VDD1P2	WRF_SYNTH_GND	WRF_VCO_GND	VDDC	VSSC	VDDC		VDDC	GPIO_7		SPI0_MISO	SPI0_CLK	SFL_CLK	5
4	WRF_RX5G_GND	WRF_AFE_VDD1P35	WRF_GENERAL_GND	WRF_EXT_TSSIA	VSSC			VSSC			VDDC	SFL_IO3	SFL_IO2	SFL_IO0	4
3	RF_GND_P3	WRF_GENERAL2_GND	WRF_AFE_GND	WRF_GPAIO_OUT	HIB_REG_ON_IN	HIB_LPO_SELMODE	HIB_WAKE_B	VSSC		VSSC	VDDC	VSSC	SFL_IO1	GPIO_14	3
2	RF_GND_P2	WRF_PA_GND3P3	WRF_TXMIX_VDD	WRF_RX2G_GND	VSSC	HIB_XTALOUT	HIB_XTALIN	VSSC	VDDC	GPIO_9	VSSC	GPIO_16	VSSC	GPIO_15	2
1	WRF_PA_VDD3P3		WRF_PAOUT_2G	WRF_RFIN_2G	VSSC	VDDC	HIB_REG_ON_OUT	HIB_VDDO	VDDC	GPIO_0	GPIO_1	GPIO_10	GPIO_11		1
	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Ball List

Table 6 contains the 151-ball WLBGA net names.

Table 6: WLBGA Net Names

Ball	Net Name
A2	GPIO_15
A3	GPIO_14
A4	SFL_IO0
A5	SFL_CLK
A6	SFL_CS
A7	UART0_CTS
A8	VDDIO
A9	VDDC
A10	REG_ON
A11	SR_VLX
A12	SR_PVSS
B1	GPIO_11
B2	VSSC
B3	SFL_IO1
B4	SFL_IO2
B5	SPI0_CLK
B6	SPI0_SISO
B7	UART0_RTS
B8	UART0_TXD
B9	I2C0_SDATA
B10	VOUT_CLDO_SENSE
B11	VOUT_CLDO
B12	SR_VDDBAT5V
C1	GPIO_10
C2	GPIO_16
C3	VSSC
C4	SFL_IO3
C5	SPI0_MISO
C6	GPIO_12
C7	UART0_RXD
C8	I2C0_CLK
C9	VSSC
C10	PMU_AVSS
C11	VOUT_HSICLDO
C12	LDO_VDD1P5
D1	GPIO_1
D2	VSSC
D3	VDDC
D4	VDDC
D7	VSSC
D8	VSSC
D9	GPIO_8
D10	VSSC
D11	VOUT_LNLDO
D12	LDO_VDDBAT5V
E1	GPIO_0
E2	GPIO_9
E3	VSSC
E5	GPIO_7
E6	SPI0_CS
E8	GPIO_13
E9	VDDIO
E10	VDDIO
E11	VDDIO
E12	VOUT_3P3
F1	VDDC
F2	VDDC
F5	VDDC
F6	VSSC
F8	VSSC
F9	VSSC
F10	GPIO_4
F11	GPIO_5
F12	GPIO_6
G1	HIB_VDDO
G2	VSSC
G3	VSSC
G4	VSSC
G6	VDDC
G7	VSSC

Ball	Net Name
G9	VSSC
G10	GPIO_2
G11	NC_G11
G12	GPIO_3
H1	HIB_REG_ON_OUT
H2	HIB_XTALIN
H3	HIB_WAKE_B
H5	VDDC
H7	VDDC
H9	NC_H9
H10	VSSC
H11	VDDC
H12	NC_H12
J1	VDDC
J2	HIB_XTALOUT
J3	HIB_LPO_SELMODE
J5	VSSC
J6	VSSC
J8	VDDIO
J9	VSSC
J10	NC_J10
J11	NC_J11
J12	NC_J12
K1	VSSC
K2	VSSC
K3	HIB_REG_ON_IN
K4	VSSC
K5	VDDC
K6	VDDC
K7	VDDIO
K8	VDDIO_RF
K9	VDDIO_RF
K10	RF_SW_CTRL_6
K11	VSSC
K12	PWR_GND
L1	WRF_RFIN_2G
L2	WRF_AFE_GND
L3	WRF_GPAIO_OUT
L4	WRF_EXT_TSSIA
L5	WRF_AFE_GND
L6	WRF_SYNTH_VDD3P3
L7	VDDC
L8	VSSC
L9	RF_SW_CTRL_4
L10	VDDC
L11	RF_SW_CTRL_1
L12	RF_SW_CTRL_7
M1	WRF_PAOUT_2G
M2	WRF_TXMIX_VDD
M3	WRF_AFE_GND
M4	WRF_AFE_GND
M5	WRF_AFE_GND
M6	WRF_XTAL_VDD1P2
M7	AVSS
M8	LPO_XTAL_IN
M9	RF_SW_CTRL_0
M10	RF_SW_CTRL_5
M11	VSSC
M12	RF_SW_CTRL_8
N2	WRF_AFE_GND
N3	WRF_AFE_GND
N4	WRF_AFE_VDD1P35
N5	WRF_SYNTH_VDD1P2
N6	WRF_XTAL_VDD1P35
N7	WRF_AFE_GND
N8	AVDD1P2
N9	RF_SW_CTRL_3
N10	NC_N10
N11	RF_SW_CTRL_9
N12	VDDIO
P1	WRF_PA_VDD3P3
P2	RF_GND_P2
P3	RF_GND_P3
P4	WRF_AFE_GND
P5	WRF_PMU_VDD1P35
P6	WRF_XTAL_XOP
P7	WRF_XTAL_XON
P8	OTP_VDD3P3
P9	RF_SW_CTRL_2
P10	JTAG_SEL

Ball	***Net Name***
P11	SRSTN

Signal Descriptions

Table 7 provides the signal name, type, and description for each BCM43903 ball. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, and O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 7: Signal Descriptions

Ball Number	Signal Name	Type	Description
Broadcom Serial Control (BSC) Interfaces			
C8	I2C0_CLK	O	BSC master clock.
B9	I2C0_SDATA	I/O	BSC serial data
Clocks			
P6	WRF_XTAL_XOP	I	XTAL oscillator input.
P7	WRF_XTAL_XON	O	XTAL oscillator output.
M8	LPO_XTAL_IN	I	External sleep clock input (32.768 kHz).
H2	HIB_XTALIN	I	3.3V 32 kHz crystal input
J2	HIB_XTALOUT	O	3.3V 32 kHz crystal output
GPIO Interface (WLAN)			
E1	GPIO_0	I/O	Programmable GPIO pins.
D1	GPIO_1	I/O	
G10	GPIO_2	I/O	
G12	GPIO_3	I/O	
F10	GPIO_4	I/O	
F11	GPIO_5	I/O	
F12	GPIO_6	I/O	
E5	GPIO_7	I/O	
D9	GPIO_8	I/O	
E2	GPIO_9	I/O	
C1	GPIO_10	I/O	
B1	GPIO_11	I/O	
C6	GPIO_12	I/O	
E8	GPIO_13	I/O	
A3	GPIO_14	I/O	
A2	GPIO_15	I/O	
C2	GPIO_16	I/O	

Table 7: Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Ground			
L2, L5, M3, M4, M5, N2, N3, N7, P4	WRF_AFE_GND	GND	AFE ground
M11, K11, H10, D10, J9, G9, F9, C9, L8, F8, D8, G7, D7, J6, F6, J5, K4, G4, G3, E3, C3, K2, G2, D2, B2, K1	VSSC	GND	Core ground for WLAN and APP sections
A12	SR_PVSS	GND	Power ground
C10	PMU_AVSS	GND	Quiet ground
M7	AVSS	GND	Baseband PLL ground
Hibernation Block, Power-Down/Power-Up, and Reset			
A10	REG_ON	I	Used by PMU to power up or power down the internal BCM43903 regulators used by the WLAN and APP sections. Also, when deasserted, this pin holds the WLAN and APP sections in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
K3	HIB_REG_ON_IN	I	Used by the hibernation block to power up or power down the internal BCM43903 regulators. For applications that use the hibernation block, HIB_REG_ON_OUT must connect to REG_ON. Also, when deasserted, this pin holds the WLAN and APP sections in reset.
H1	HIB_REG_ON_OUT	O	REG_ON output signal generated by the hibernation block.
H3	HIB_WAKE_B	I	Wake up chip from hibernation mode.
J3	HIB_LPO_SELMODE	I	Select precise or coarse 32 kHz clock.
P11	SRSTN	I	System reset. This active-low signal resets the backplanes.
JTAG Interface			
P10	JTAG_SEL	I	JTAG select. This pin must be connected to ground if the JTAG interface is not used.
No Connects			
J10, J11, J12, H9, H12, G11, N10, L4	NC_J10, NC_J11, NC_J12, NC_H9, NC_H12, NC_G11, NC_N10, WRF_EXT_TSSIA	–	No connect

Table 7: Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Power Supplies (Miscellaneous)			
P8	OTP_VDD3P3	PWR	OTP 3.3V supply
H11, L10, A9, L7, H7, K6, G6, K5, H5, F5, D4, D3, F2, J1, F1	VDDC	PWR	1.2V core supply for WLAN
N12, E11, E10, E9, J8, A8, K7	VDDIO	PWR	I/O supply
K8, K9	VDDIO_RF	PWR	I/O supply for RF switch control pads (3.3V).
K12	PWR_GND	GND	Power supply ground
G1	HIB_VDDO	PWR	I/O supply for hibernation block
N8	AVDD1P2	PWR	1.2V supply for baseband PLL
Power Supplies (WLAN)			
L6	WRF_SYNTH_VDD3P3	PWR	Synthesizer VDD 3.3V supply
P1	WRF_PA_VDD3P3	PWR	2.4 GHz PA 3.3V VBAT supply
P5	WRF_PMU_VDD1P35	PWR	PMU 1.35V supply
M2	WRF_TXMIX_VDD	PWR	3.3V supply for TX mixer
N5	WRF_SYNTH_VDD1P2	PWR	1.2V supply for synthesizer
N4	WRF_AFE_VDD1P35	PWR	1.35V supply for the analog front end (AFE)
PWM Interface (Alternate Function for GPIOs)			
–	PWM0	O	Pulse width modulation bit 0.
–	PWM1	O	Pulse width modulation bit 1
–	PWM2	O	Pulse width modulation bit 2
–	PWM3	O	Pulse width modulation bit 3
–	PWM4	O	Pulse width modulation bit 4
–	PWM5	O	Pulse width modulation bit 5

Table 7: Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
RF Signal Interface (WLAN)			
L1	WRF_RFIN_2G	I	2.4 GHz WLAN receiver input
P3	RF_GND_P3	GND	RF ground
M1	WRF_PAOUT_2G	O	2.4 GHz WLAN PA output
P2	RF_GND_P2	GND	RF ground
L3	WRF_GPAIO_OUT	I/O	Analog GPIO
RF Switch Control Lines			
M9	RF_SW_CTRL_0	O	Programmable RF switch control lines. The control lines are programmable via the driver and nvram.txt file.
L11	RF_SW_CTRL_1	O	
P9	RF_SW_CTRL_2	O	
N9	RF_SW_CTRL_3	O	
L9	RF_SW_CTRL_4	O	
M10	RF_SW_CTRL_5	I/O	
K10	RF_SW_CTRL_6	I/O	
L12	RF_SW_CTRL_7	I/O	
M12	RF_SW_CTRL_8	I/O	
N11	RF_SW_CTRL_9	I/O	
SPI Flash Interface			
A5	SFL_CLK	O	Flash clock
A4	SFL_IO0	I/O	Flash data
B3	SFL_IO1	I/O	Flash data
B4	SFL_IO2	I/O	Flash data
C4	SFL_IO3	I/O	Flash data
A6	SFL_CS	O	Flash slave select

Table 7: Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
SPI Interface			
Note: The SPI interface can alternatively be configured and used as a BSC interface.			
B5	SPI0_CLK	O	SPI clock
C5	SPI0_MISO	I	SPI data master in
B6	SPI0_SISO	O	SPI data master out
E6	SPI0_CS	O	SPI slave select
UART Interface			
A7	UART0_CTS	I	UART clear-to-send
B7	UART0_RTS	O	UART request-to-send
C7	UART0_RXD	I	UART serial input
B8	UART0_TXD	O	UART serial output
Voltage Regulators (Integrated)			
B12	SR_VDDBAT5V	I	VBAT.
A11	SR_VLX	O	CBUCK switching regulator output
C12	LDO_VDD1P5	I	LNLDO input
D12	LDO_VDDBAT5V	I	LDO VBAT
N6	WRF_XTAL_VDD1P35	I	XTAL LDO input (1.35V)
M6	WRF_XTAL_VDD1P2	O	XTAL LDO output (1.2V)
D11	VOUT_LNLDO	O	Terminate with 2.2 µF capacitor to GND
B11	VOUT_CLDO	O	Output of core LDO
E12	VOUT_3P3	O	LDO 3.3V output
B10	VOUT_CLDO_SENSE	O	Voltage sense pin for core LDO
C11	VOUT_HSICLDO	O	Output of HSIC LDO

Section 10: GPIO Signals and Strapping Options

Overview

This section describes GPIO signals and strapping options. The pins are sampled at power-on reset (POR) to determine various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in Table 9 on page 51. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to ground, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Weak Pull-Down and Pull-Up Resistances

At VDDO = 3.3V ±10%, the minimum, typical, and maximum weak pull-down resistances (for a pin voltage of VDDO) are 37.99 kΩ, 44.57 kΩ, and 51.56 kΩ, respectively. At VDDO = 3.3V ±10%, the minimum, typical, and maximum weak pull-up resistances (for a pin voltage of 0V) are 34.73 kΩ, 39.58 kΩ, and 44.51 kΩ, respectively.

Strapping Options

Table 8 provides the strapping options.

Table 8: Strapping Options

Pin Name	Strap	#	Default Internal Pull During Strap	Description
GPIO_1	GSPI_MODE	D1	PD	Enable gSPI interface
GPIO_7	WCPU_BOOT_MODE	E5	PD	Boot from SoC SROM or SoC SRAM
GPIO_11	ACPU_BOOT_MODE	B1	PD	Boot from tightly coupled memory (TCM) ROM or TCM RAM
GPIO_13	SDIO_MODE	E8	PD	Select either SDIO host mode or SDIO device mode
GPIO_15	VTRIM_EN	A2	PD	Enable PMU voltage trimming
RF_SW_CTRL_5	DAP_CLK_SEL	M10	PD	Select XTAL clock or the test clock (tck) for the debug access port (DAP)
RF_SW_CTRL_7	RSRC_INIT_MODE	L12	PD	PMU resource initialization mode selection

Alternate GPIO Signal Functions

Table 9 provides the alternate signal functions of the GPIO signals.

Table 9: Alternate GPIO Signal Functions

GPIO	*Default*	*JTAG_SEL*	*Default Pull*	*HOLD/PDLOW/PDHIGH*	*Strap*	*Comments*
GPIO_0	–	–	No pull	HOLD	–	8 mA
GPIO_1	–	–	Down	HOLD	GSPI_MODE	8 mA
GPIO_2	GCI_GPIO(0)	JTAG_TCK	No pull	HOLD	–	8 mA
GPIO_3	GCI_GPIO(1)	JTAG_TMS	No pull	HOLD	–	8 mA
GPIO_4	GCI_GPIO(2)	JTAG_TDI	No pull	HOLD	–	8 mA
GPIO_5	GCI_GPIO(3)	JTAG_TDO	No pull	HOLD	–	8 mA
GPIO_6	GCI_GPIO(4)	JTAG_TRST	No pull	HOLD	–	8 mA
GPIO_7	–	–	Down	HOLD	WCPU_BOOT_MODE	8 mA
GPIO_8	GPIO_8	–	No pull	HOLD	–	8 mA
GPIO_9	GPIO_9	–	Down	HOLD		8 mA
GPIO_10	GPIO_10	–	No pull	HOLD	–	8 mA
GPIO_11	–	–	Down	HOLD	ACPU_BOOT_MODE	8 mA
GPIO_12	GPIO_12	–	No pull	HOLD	–	8 mA
GPIO_13	–	–	Down	HOLD	SDIO_MODE	8 mA
GPIO_14	GPIO_14	–	No pull	HOLD	–	8 mA
GPIO_15	–	–	Down	HOLD	VTRIM_EN	8 mA
GPIO_16	–	–	No pull	HOLD	–	8 mA

Section 11: Pin Multiplexing

Table 10 shows the pin multiplexing functions.

Table 10: Pin Multiplexing

Pin	**Function**										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
GPIO_0	GPIO_0	UART0_RXD	I2C1_SDATA	PWM0	SPI1_MISO	PWM2	GPIO_12	GPIO_8	–	PWM4	–
GPIO_1	GPIO_1	UART0_TXD	I2C1_CLK	PWM1	SPI1_CLK	PWM3	GPIO_13	GPIO_9	–	PWM5	–
GPIO_2	GPIO_2	–	–	GCI_GPIO_0	–	–	–	–	TCK	–	–
GPIO_3	GPIO_3	–	–	GCI_GPIO_1	–	–	–	–	TMS	–	–
GPIO_4	GPIO_4	–	–	GCI_GPIO_2	–	–	–	–	TDI	–	–
GPIO_5	GPIO_5	–	–	GCI_GPIO_3	–	–	–	–	TDO	–	–
GPIO_6	GPIO_6	–	–	GCI_GPIO_4	–	–	–	–	TRST_L	–	–
GPIO_7	GPIO_7	UART0_RTS_OUT	PWM1	PWM3	SPI1_CS	I2C1_CLK	GPIO_15	GPIO_11	PMU_TEST_O	–	PWM5
GPIO_8	GPIO_8	SPI1_MISO	PWM2	PWM4	UART0_RXD	–	GPIO_16	GPIO_12	TAP_SEL_P	I2C1_SDATA	PWM0
GPIO_9	GPIO_9	SPI1_CLK	PWM3	PWM5	UART0_TXD	–	GPIO_0	GPIO_13	–	I2C1_CLK	PWM1
GPIO_10	GPIO_10	SPI1_MOSI	PWM4	I2C1_SDATA	UART0_CTS_IN	PWM0	GPIO_1	GPIO_14	PWM2	–	–
GPIO_11	GPIO_11	SPI1_CS	PWM5	I2C1_CLK	UART0_RTS_OUT	PWM1	GPIO_7	GPIO_15	PWM3	–	–
GPIO_12	GPIO_12	I2C1_SDATA	UART0_RXD	SPI1_MISO	PWM2	PWM4	GPIO_8	GPIO_16	PWM0	–	–
GPIO_13	GPIO_13	I2C1_CLK	UART0_TXD	SPI1_CLK	PWM3	PWM5	GPIO_9	GPIO_0	PWM1	–	–
GPIO_14	GPIO_14	PWM0	UART0_CTS_IN	SPI1_MOSI	I2C1_SDATA	–	GPIO_10	–	PWM4	–	PWM2
GPIO_15	GPIO_15	PWM1	UART0_RTS_OUT	SPI1_CS	I2C1_CLK	–	GPIO_11	GPIO_7	PWM5	–	PWM3
GPIO_16	GPIO_16	UART0_CTS_IN	PWM0	PWM2	SPI1_MOSI	I2C1_SDATA	GPIO_14	GPIO_10	RF_DISABLE_L	–	PWM4
RF_SW_CTRL_5	RF_SW_CTRL_5	GCI_GPIO_5	–	–	–	–	–	–	–	–	–
RF_SW_CTRL_6	RF_SW_CTRL_6	UART_DBG_RX	SECI_IN	–	–	–	–	–	–	–	–

Table 10: Pin Multiplexing

Pin	**Function**										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
RF_SW_ CTRL_7	RF_SW_ CTRL_7	UART_ DBG_TX	SECI_OUT	–	–	–	–	–	–	–	–
RF_SW_ CTRL_8	RF_SW_ CTRL_8	SECI_IN	UART_ DBG_RX	–	–	–	–	–	–	–	–
RF_SW_ CTRL_9	RF_SW_ CTRL_9	SECI_OUT	UART_ DBG_TX	–	–	–	–	–	–	–	–
SPI0_MISO	SPI0_MISO	GPIO_17	GPIO_24	–	–	–	–	–	–	–	–
SPI0_CLK	SPI0_CLK	GPIO_18	GPIO_25	–	–	–	–	–	–	–	–
SPI0_MOSI	SPI0_MOSI	GPIO_19	GPIO_26	–	–	–	–	–	–	–	–
SPI0_CS	SPI0_CS	GPIO_20	GPIO_27	–	–	–	–	–	–	–	–
I2C0_SDATA	I2C0_SDATA	GPIO_21	GPIO_28	–	–	–	–	–	–	–	–
I2C0_CLK	I2C0_CLK	GPIO_22	GPIO_29	–	–	–	–	–	–	–	–

Section 12: I/O States

Table 11 provides I/O state information for the signals listed.

The following notations are used in Table 11:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 11: I/O States

Ball Name	*I/O*	*Keeper*[a]	*Active Mode*	*Low Power State/Sleep (All Power Present)*	*Power-down*[b] *(REG_ON Held Low)*	*Out-of-Reset; Before Software Download (REG_ON High)*	*Power Rail*
HIB_REG_ON_IN	I	N	Input; PD (Pull-down can be disabled.)	Input; PD (Pull-down can be disabled.)	Input	Input	–
REG_ON	I	N	Input; PD (Pull-down can be disabled.)	Input; PD (Pull-down can be disabled.)	Input; PD (of 200 kΩ)	Input; PD (of 200 kΩ)	–
GPIO_0	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_1	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_2	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_3	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO

Table 11: I/O States

Ball Name	I/O	Keeper[a]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[b] (REG_ON Held Low)	Out-of-Reset; Before Software Download (REG_ON High)	Power Rail
GPIO_4	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_5	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_6	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_7	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_8	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_9	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_10	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_11	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	Input/Output; PU, PD, or NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	VDDIO
GPIO_12	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_13	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_14	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO

Table 11: I/O States

Ball Name	I/O	Keeper[a]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[b] (REG_ON Held Low)	Out-of-Reset; Before Software Download (REG_ON High)	Power Rail
GPIO_15	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
GPIO_16	I/O	Y	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, or NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	VDDIO
RF_SW_CTRL (0 to 9)	I/O	Y	Output; NoPull	Output; NoPull	High-Z	Output; NoPull	VDDIO_RF

a. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad (WL_REG_ON, for example).

b. In the power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

Section 13: Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 12 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 12: Absolute Maximum Ratings

Parameter	*Symbol*	*Value*	*Unit*
DC supply for VBAT and PA driver supply [a]	VBAT	–0.5 to +5.5	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/O	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO, LNLDO, and LDO[b]	–	–0.5 to 1.575	V
3.3V DC supply voltage for RF analog[c]	VDD3P3RF	–0.5 to 3.6	V
1.35V DC supply voltage for RF analog[d]	VDD1P35RF	–0.5 to 1.5	V
1.2V DC supply voltage for RF analog[e]	VDD1P2RF	–0.5 to 1.26	V
1.2V DC supply voltage for analog circuits[f]	VDD1P2A	–0.5 to 1.26	V
DC supply voltage for the core[g]	VDDC	–0.5 to 1.32	V
DC supply voltage for OTP memory	OTP_VDD3P3	–0.5 to 3.9	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum junction temperature	T_j	125	°C

a. For the SR_VDDBAT5V and LDO_VDDBAT5V supplies.
b. For the LDO_VDD1P5 and WRF_XTAL_VDD1P35 supplies.
c. For the WRF_SYNTH_VDD3P3, WRF_PA_VDD3P3, and WRF_TXMIX_VDD supplies.
d. For WRF_PMU_VDD1P35 and WRF_AFE_VDD1P35 supplies.
e. For the WRF_SYNTH_VDD1P2 supply.
f. For the AVDD1P2 supply.
g. For the VDD supply.

Environmental Ratings

The environmental ratings are shown in Table 13.

Table 13: Environmental Ratings

Characteristic	*Value*	*Units*	*Conditions/Comments*
Ambient temperature (T_A)	–30 to +85	°C	Functional operation
Storage temperature	–40 to +125	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 14: ESD Specifications

Pin Type	*Symbol*	*Condition*	*ESD Rating*	*Unit*
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1.5 kΩ	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 15. Operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 15: Recommended Operating Conditions and DC Characteristics

		Value			
Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for VBAT	VBAT	2.3[a]	3.6	4.8	V
DC supply voltage for digital I/O	VDDIO	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF[b]	3.13	3.3	3.6	V
DC input supply voltage for CLDO, LNLDO, and LDO	–	1.3	1.35	1.5	V
3.3V DC supply voltage for RF analog	VDD3P3RF[c]	3	3.3	3.45	V
1.35V DC supply voltage for RF analog	VDD1P35RF[c]	1.3	1.35	1.5	V
1.2V DC supply voltage for RF analog	VDD1P2RF[c]	1.1	1.2	1.26	V
1.2V DC supply voltage for analog	VDD1P2A[c]	1.1	1.2	1.26	V
DC supply voltage for core	VDDC	1.14	1.2	1.26	V
DC supply voltage for OTP memory	OTP_VDD3P3[b]	2.97	3.3	3.63	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD[c]	1.62	1.8	1.98	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[d]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V

Table 15: Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Input capacitance	C_{IN}	–	–	5	pF

a. The BCM43903 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3V < VBAT < 4.8V.

b. VDD3P3RF, which is an internally generated supply, can drive this node. There is sufficient current and the appropriate state is maintained during hibernation and sleep cycles.

c. Internally generated supply.

d. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

Power Supply Segments

The digital I/O's are placed in physical segments. The supply voltage for each segment can be independently selected.

Table 16 shows the power supply segments and the I/O pins associated with each segment.

Table 16: Power Supply Segments

Power Supply Segment	***Pins***
VDDIO	GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, GPIO_7, GPIO_8, GPIO_9, GPIO_10, GPIO_11, GPIO_12, GPIO_13, GPIO_14, GPIO_15, GPIO_16, I2C0_CLK, I2C0_SDATA, I2C1_CLK, I2C1_SDATA, JTAG_SEL, SFL_CLK, SFL_CS, SFL_IO0, SFL_IO1, SFL_IO2, SFL_IO3, SPI0_CLK, SPI0_CS, SPI0_MISO, SPI0_SISO, SPI1_CLK, SPI1_CS, SPI1_MISO, SPI1_SISO, SRSTN, UART0_CTS, UART0_RTS, UART0_RXD, UART0_TXD
VDDIO_RF	RF_SW_CTRL_0, RF_SW_CTRL_1, RF_SW_CTRL_2, RF_SW_CTRL_3, RF_SW_CTRL_4, RF_SW_CTRL_5, RF_SW_CTRL_6, RF_SW_CTRL_7, RF_SW_CTRL_8, RF_SW_CTRL_9

GPIO, UART, and JTAG Interfaces DC Characteristics

Table 17: GPIO, UART, and JTAG Interfaces

Parameter	***Symbol***	***Minimum***	***Maximum***	***Units***	***Conditions***
Logic input high voltage	V_{IH}	2.0	VDDIO + 0.5	V	–
Logic input low voltage	V_{IL}	–0.5	0.8	V	–
Logic output high voltage	V_{OH}	2.4	–	V	–
Logic output low voltage	V_{OL}	–	0.4	V	–

Section 14: WLAN RF Specifications

Introduction

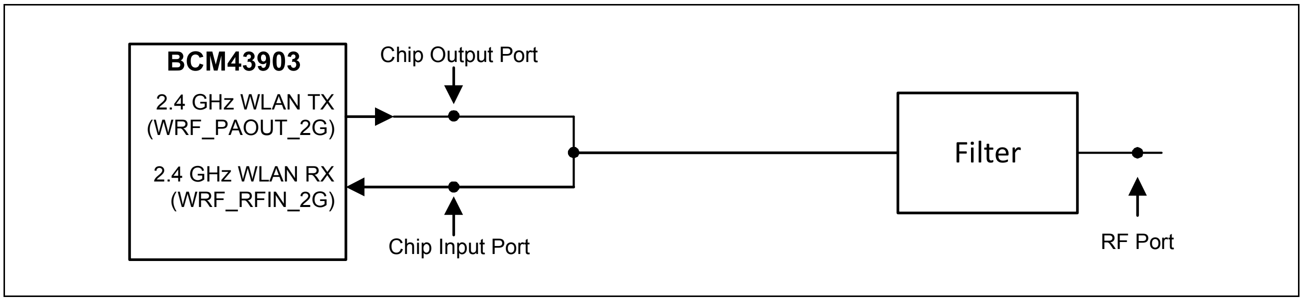
The BCM43903 includes an integrated direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.

Note: Values in this section of the data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 13: "Environmental Ratings," on page 58 and Table 15: "Recommended Operating Conditions and DC Characteristics," on page 59. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 12: Port Locations for WLAN Testing



2.4 GHz Band General RF Specifications

Table 18: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications shown in Table 19 apply at the chip ports, unless otherwise defined.

Table 19: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	–	–98.9	–	dBm
	2 Mbps DSSS	–	–96.0	–	dBm
	5.5 Mbps DSSS	–	–93.9	–	dBm
	11 Mbps DSSS	–	–90.4	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–95.0	–	dBm
	9 Mbps OFDM	–	–93.8	–	dBm
	12 Mbps OFDM	–	–92.7	–	dBm
	18 Mbps OFDM	–	–90.3	–	dBm
	24 Mbps OFDM	–	–87.1	–	dBm
	36 Mbps OFDM	–	–83.6	–	dBm
	48 Mbps OFDM	–	–79.3	–	dBm
	54 Mbps OFDM	–	–78.0	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) [a] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.6	–	dBm
	MCS1	–	–92.1	–	dBm
	MCS2	–	–89.8	–	dBm
	MCS3	–	–86.6	–	dBm
	MCS4	–	–83.0	–	dBm
	MCS5	–	–78.3	–	dBm
	MCS6	–	–76.6	–	dBm
	MCS7	–	–75.0	–	dBm
Input in-band IP3	Maximum LNA gain	–	–8	–	dBm
	Minimum LNA gain	–	+9	–	dBm

Table 19: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	***Condition/Notes***		***Minimum***	***Typical***	***Maximum***	***Unit***
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6, 9, 12 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–2 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps (10% PER, 1024 octets)		–14.5	–	–	dBm
	@ MCS3–7 rates (10% PER, 4095 octets)		–14.5	–	–	dBm
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes.)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
Maximum receiver gain	–	–	–	66	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[b]	Range –95[c] dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	11.5	13	dB

Table 19: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Receiver cascaded noise figure	At maximum gain	–	4	–	dB

a. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.
b. The minimum and maximum values shown have a 95% confidence level.
c. –95 dBm with calibration at time of manufacture, –92 dBm without calibration.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in Table 20 apply at the chip ports.

Table 20: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
RF port TX power EVM[a] (highest power setting, 25°C, and VBAT = 3.6)	DSS/CCK	–9 dB	–	20.5	–	dBm
	OFDM, BPSK	–8 dB	–	20	–	dBm
	OFDM, QPSK	–13 dB	–	20	–	dBm
	OFDM, 16-QAM	–19 dB	–	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	19	–	dBm
	OFDM, 64-QAM (MCS7, HT20)	–27 dB	–	18.5	–	dBm
OFDM EVM[b] (25°C, VBAT = 3.6V)	OFDM, BPSK	5 dBm	–29	–31	–	dB
	OFDM, 64-QAM	5 dBm	–31	–33	–	dB
	MCS7	5 dBm	–33	–35	–	dB
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to 10 dBm to 20 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port TX	$Z_o = 50\Omega$		–	6	–	dB

[a] This specification row indicates the linear power specification as measured from the chip output port. The requirement is in dBm (TX power). The ratio (dB) in the Conditions/Notes column is the EVM.

[b] This specification row indicates the EVM floor. The requirement is in dB (EVM). The power in the Conditions/ Notes column is the TX power specification in dBm.

General Spurious Emissions Specifications

This section provides the TX and RX spurious emissions specifications for the WLAN 2.4 GHz band. The recommended spectrum analyzer settings for the spurious emissions specifications are provided in Table 21.

Table 21: Recommended Spectrum Analyzer Settings

Parameter	***Setting***
Resolution bandwidth (RBW)	1 MHz
Video bandwidth (VBW)	1 MHz
Sweep	Auto
Span	100 MHz
Detector	Maximum peak
Trace	Maximum hold
Modulation	OFDM

Transmitter Spurious Emissions Specifications

2.4 GHz Band Spurious Emissions

20-MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/18 specifications for channel 2442 are listed in Table 22.

- AFE=VCO/18
- AFE=VCO/16
- AFE=VCO/8
- AFE=VCO/6

Table 22: 2.4 GHz Band, 20-MHz Channel Spacing TX Spurious Emissions Specifications [a]

		Frequency (Fch; MHz) Channel 2442	
Spurious Frequency	**Power (dBm)**	**Typical (dBm)**	**Maximum (dBm)**
HD2	–5	–58.7	–56.6
HD3	–5	–71.7	–68.9
HD4	–5	–57.2	–50.2
VCO	–5	–45.7	–43.7
VCOx2	–5	–71.5	–69.0
VCOx3	–5	–85.2	–74.1
AFEx3	–5	–	–
AFEx4	–5	–	–
AFEx5	–5	–	–
AFEx6	–5	–78.4	–73.5
AFEx7	–5	–77.3	–76.1
AFEx8	–5	–73.6	–73.4
AFEx9	–5	–70.9	–69.9
AFEx10	–5	–81.1	–78.8
AFEx11	–5	–70.3	–69.1
AFEx13	–5	–72.0	–71.0
AFEx14	–5	–76.2	–73.8
AFEx15	–5	–79.3	–73.6
AFEx16	–5	–82.5	–77.9
AFEx17	–5	–85.3	–77.7
AFEx19	–5	–83.4	–77.6
AFEx20	–5	–83.9	–76.5
AFEx21	–5	–78.7	–74.9
AFEx22	–5	–82.1	–76.2
AFEx23	–5	–87.1	–77.6

[a] VCO = 1.5 × Fch, where Fch is the center frequency of the channel.

Receiver Spurious Emissions Specifications

Table 23: 2G General Receiver Spurious Emissions

Band	Frequency Range	Typical	Maximum	Unit
2G	2.4 GHz < f < 2.5 GHz	–75.5	–74.1	dBm
	3.6 GHz < f < 3.8 GHz	–52.8	–50.9	dBm

Section 15: Internal Regulator Electrical Specifications

Core Buck Switching Regulator

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.

Note: Functional operation is not guaranteed outside of the specification limits provided in this section.

Table 24: Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Unit
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	4.8[a]	V
PWM mode switching frequency	CCM, load > 100 mA VBAT = 3.6V.	–	4	–	MHz
PWM output current	–	–	–	550	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V.	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static load. Max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 μH inductor with min. effective L > 1.05 μH, cap. + board total – ESR < 20 mΩ, C_{out} > 1.9 μF, ESL<200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak efficiency at 200 mA load.	78	86	–	%
PFM mode efficiency	10 mA load current.	70	81	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V.	–	400	500	μs
External inductor	0806 size, 2.2 μH, DCR = 0.11Ω, ACR = 1.18Ω @ 4 MHz.	–	2.2	–	μH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 μF ±20%, 6.3V.	2.0[b]	4.7	10[c]	μF
External input capacitor	For SR_VDDBAT5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7 μF ±20%, 6.3V.	0.67[b]	4.7	–	μF
Input supply voltage ramp-up time	0 to 4.3V.	40	–	–	μs

[a] The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

[b] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

c. Total capacitance includes those connected at the far end of the active load.

3.3V LDO (LDO3P3)

Table 25: LDO3P3 Specifications

Specification	*Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	4.8[a]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V.	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load.	–	–	85	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max. load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 450 mA.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o + 0.2V$, $V_o = 3.3V$, $C_o = 4.7\ \mu F$, Max load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V.	1.0[b]	4.7	10	µF
External input capacitor	For LDO_VDDBAT5V pin (shared with band gap) ceramic, X5R, 0402, (ESR: 30mΩ–200 mΩ), ± 10%, 10V. Not needed if sharing 4.7 µF VBAT capacitor with SR_VDDBAT5V.	–	4.7	–	µF

[a] The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

[b] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

CLDO

Table 26: CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	350	mA
Output voltage, V_o	Programmable in 10 mV steps. Default = 1.2.V.	0.95	1.2	1.26	V
Dropout voltage	At max. load.	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Quiescent current	No load.	–	26	–	µA
	200 mA load.	–	2.48	–	mA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load.	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA.	–	0.02	0.05	mV/mA
Leakage current	Power down.	–	10	40	µA
	Bypass mode.	–	2	6	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF.	20	–		dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO turn-on time	LDO turn-on time when the rest of the chip is up.	–	140	180	µs
External output capacitor, C_o	Total ESR: 5 mΩ–240 mΩ.	3.76[a]	4.7	–	µF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output.	–	1	2.2	µF

[a] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

LNLDO

Table 27: LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$)dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V.	1.1	1.2	1.275	V
Dropout voltage	At maximum load.	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Quiescent current	No load.	–	44	–	μA
	Max. load.	–	970	990	μA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, 150 mA load.	–	–	5	mV/V
Load regulation	Load from 1 mA to 150 mA.	–	0.02	0.05	mV/mA
Leakage current	Power-down.	–	–	10	μA
Output noise	@30 kHz, 60–150 mA load C_o = 2.2 μF. @100 kHz, 60–150 mA load C_o = 2.2 μF.	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 μF, V_o = 1.2V.	20	–	–	dB
LDO turn-on time	LDO turn-on time when the rest of the chip is up.	–	140	180	μs
External output capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ.	0.5[a]	2.2	4.7	μF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ.	–	1	2.2	μF

[a] Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

BBPLL LDO

Table 28: BBPLL LDO Specifications

Parameter	Conditions and Comments	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. $V_{in} = V_o + 0.15V = 1.35V$ (for $V_o = 1.2V$). The dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V.	1.1	1.2	1.275	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation.	–4	–	+4	%
Output current	Peak load = 80 mA, average = 35 mA	0.1	–	55	mA
Quiescent current	No load	–	10	12	µA
	55 mA load	–	550	570	µA
Line regulation	V_{in} from (V_o + 0.15V) to 1.5V; 200 mA load	–	–	5	mV/V
Load regulation	load from 1mA to 200 mA; $V_{in} \geq (V_o + 0.15V)$	–	0.025	0.045	mV/mA
Leakage current	Powered down. Junction temperature is 85°C.	–	5	20	µA
	Bypass mode	–	0.2	1.5	µA
PSRR	@1 kHz, $V_{in} \geq V_o + 0.15V$, Co = 4.7 µF	20	–	–	dB
Start-up time of PMU	VIO up and steady. Time from REG_ON rising edge to CLDO reaching 99% of V_o.	–	530	700	us
LDO turn-on time	The LDO turn-on time when the rest of the chip is up.	–	140	180	us
Inrush current	Vin=Vo+0.15V to 1.5V, Co=0.47uF, no load	–	60	70	mA
External output capacitor, C_o	Ceramic, X5R, size 0201, max. 6.3V, 20% tolerance	0.27	0.47	–	µF
External input capacitor	Only use an external input capacitor at the LDO_VDD1P5 pin if it is not supplied from the CBUCK output.	–	1	–	µF

Section 16: System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Note: Unless otherwise stated, these values apply for the conditions specified in Table 15: “Recommended Operating Conditions and DC Characteristics,” on page 59.

WLAN Current Consumption

The tables in this subsection show the typical, total current used by the BCM43903. Current values may be measured with the APPS core powered off. The first column of the table, the mode description, will state the power condition of the APPS core.

2.4 GHz Mode

Table 29: 2.4 GHz Mode WLAN Current Consumption

Mode	*V_{BAT} = 3.6V [a] (µA)*	*VDDIO = VDDIO_HIB = 3.3V [a, b] (µA)*
Sleep Modes		
Radio off [c]	3	3
Sleep [d, e]	6	160
IEEE Power Save, DTIM=1, single RX, APPS powered down [f]	2180	160
IEEE Power Save, DTIM=3, single RX, APPS powered down [g]	680	160
IEEE Power Save, DTIM=9, single RX, APPS powered down	233	160
Active Modes		
Continuous RX mode MCS7, HT20, 1SS, APPS powered up [h, i]	57,200	60
CRS-HT20, APPS powered up [j]	55,200	60
Continuous TX mode 1 Mbps, APPS powered up [k]	336,000	60
Continuous TX mode MCS7, HT20, 1SS, 1 TX, APPS powered up [k]	337,900	60
Ping Modes		
Ping to associated access point [k]	336,000	60
Sleep	6	160

[a] Typical silicon.

[b] VIO is specified with all pins idle (not switching) and not driving any loads.

[c] REG_ON is low or the device is in hibernation, and all supplies are present.

d. REG_ON is high. APPS domain is powered down. WLAN domain is in low-power state retention mode. Top level is powered up.
e. Inter-beacon current.
f. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
g. Beacon interval = 307.2 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
h. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
i. Measured using packet engine test mode.
j. Carrier sense (CCA) when no carrier present.
k. Duty cycle is 100%.

Section 17: SPI Flash Characteristics

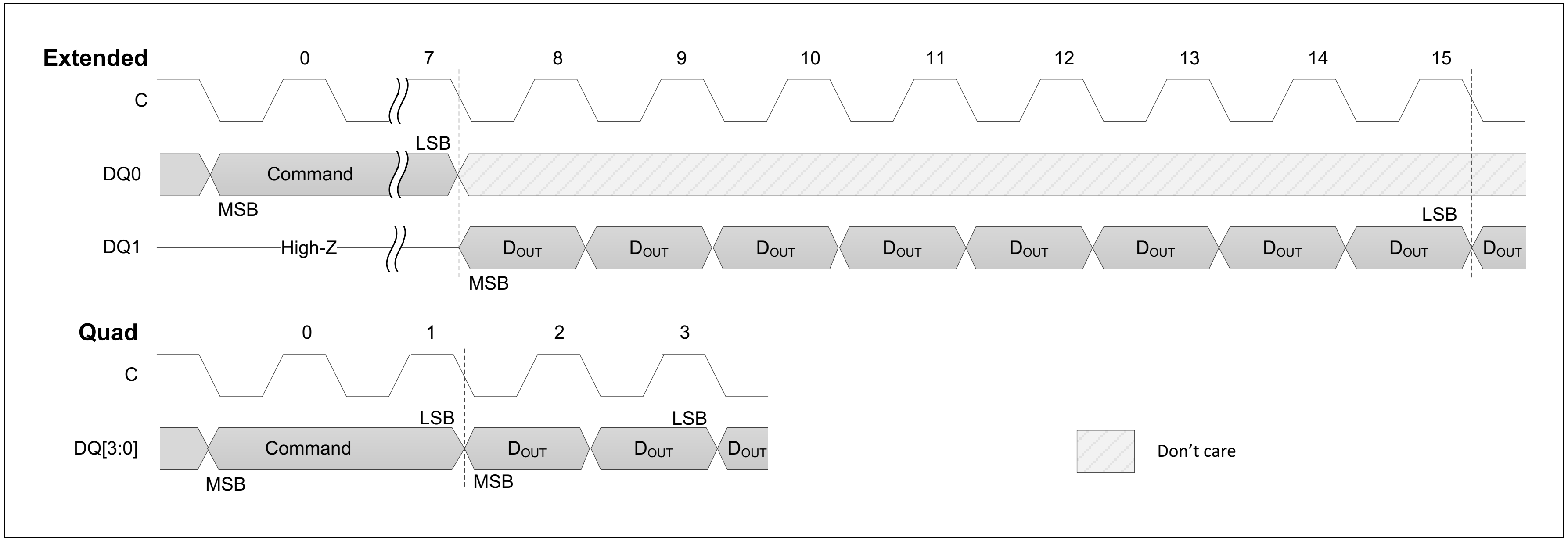
SPI Flash Timing

Read-Register Timing

Figure 13 shows the SPI flash extended and quad read-register timing.

Note: Regarding Figure 13: All Read Register commands except Read Lock Register are supported. A Read Nonvolatile Configuration Register operation will output data starting from the least significant byte.

Figure 13: SPI Flash Read-Register Timing



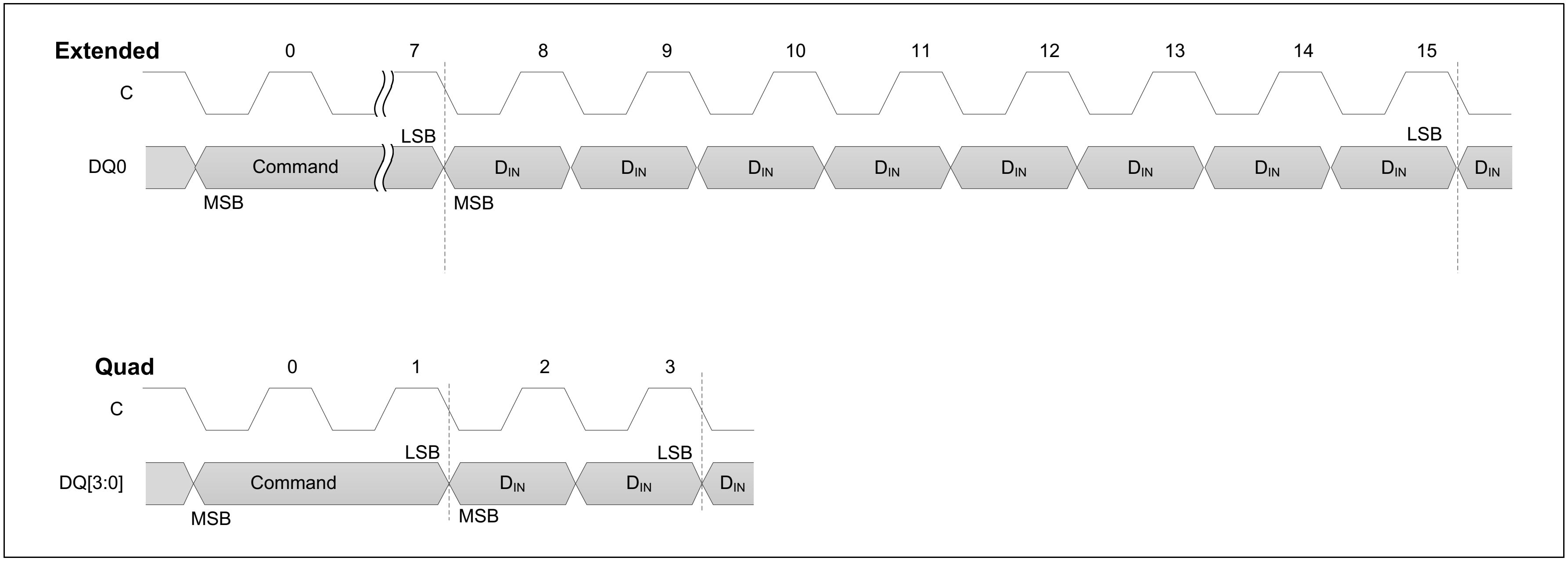
Write-Register Timing

Figure 14 shows the SPI flash extended and quad write-register timing.

Note: Regarding Figure 14:

1. All write-register commands except Write Lock Register are supported.
2. The waveform must be extended for each protocol: to 23 for extended and five for quad.
3. A Write Nonvolatile Configuration Register operation requires data being sent starting from the least significant byte.

Figure 14: SPI Flash Write-Register Timing



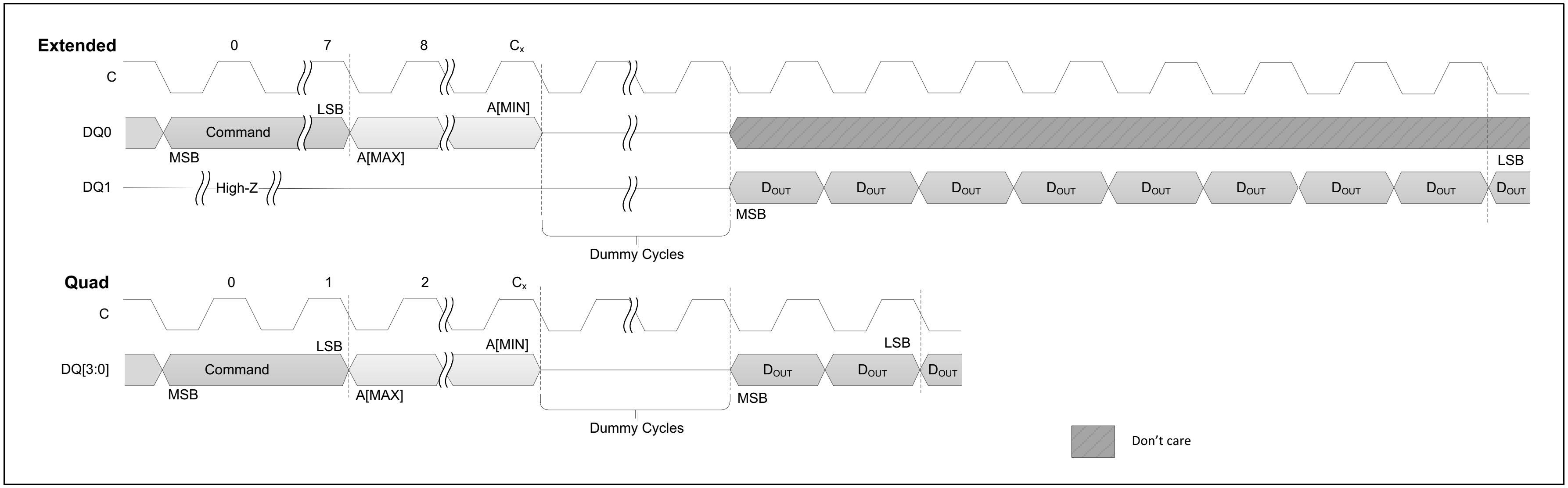
Memory Fast-Read Timing

Figure 15 shows the SPI flash extended and quad memory fast-read timing.

Note: Regarding Figure 15:

1. 24-bit addressing is used, so A[MAX] = A[23] and A[MIN] = A[0].
2. For an extended SPI protocol, $C_x = 7 + (A[MAX] + 1)$.
3. For a quad SPI protocol, $C_x = 1 + (A[MAX] + 1)/4$.

Figure 15: Memory Fast-Read Timing



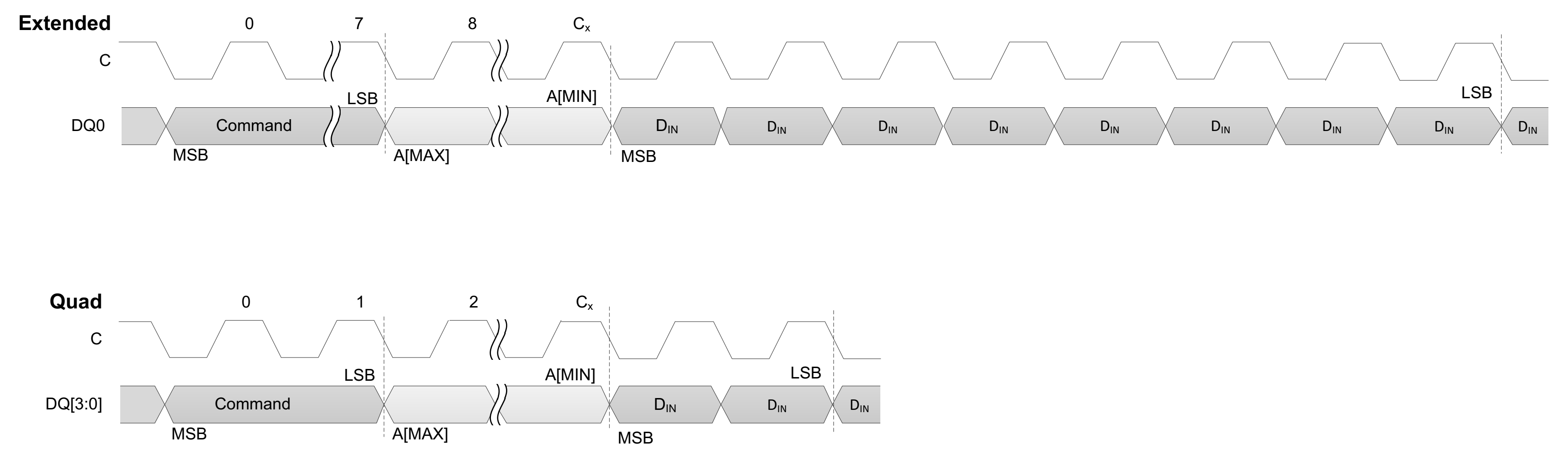
Memory-Write Timing

Figure 16 shows the SPI flash extended and quad memory-write (Page Program) timing.

Note: Regarding Figure 16:

1. For an extended SPI protocol, $C_x = 7 + (A[MAX] + 1)$.
2. For a quad SPI protocol, $C_x = 1 + (A[MAX] + 1)/4$.

Figure 16: Memory-Write Timing



SPI Flash Parameters

The combination of Figure 17 and Table 30 provide the SPI flash timing parameters.

Figure 17: SPI Flash Timing Parameters Diagram

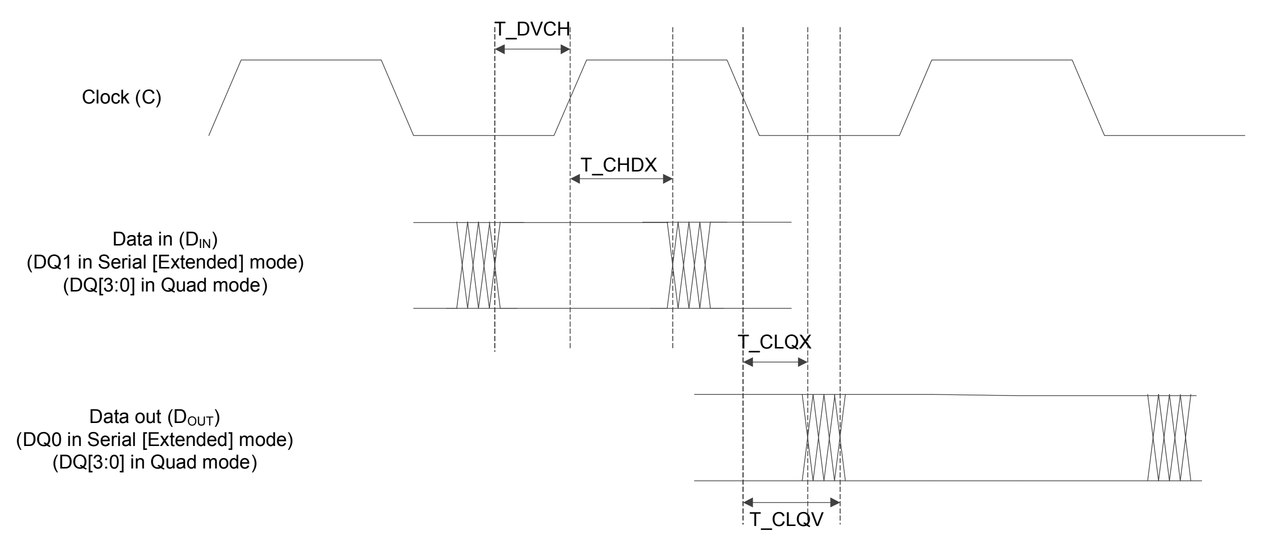


Table 30: SPI Flash Timing Parameters

Parameter	*Description*	*Minimum*	*Maximum*	*Units*
T_DVCH	Data setup time	2	–	ns
T_CHDX	Data hold time	3	–	ns
T_CLQX	Output hold time	1	–	ns
T_CLQV	Output valid time (with a 10 pF load)	–	5	ns

Section 18: Power-Up Sequence and Timing

Sequencing of Reset and Regulator Control Signals

The BCM43903 has two signals that allow the host to control power consumption by enabling or disabling the internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 18 and Figure 19 on page 82). The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

- **REG_ON**: Used by the PMU to power-up the BCM43903. It controls the internal BCM43903 regulators. When this pin is high, the regulators are enabled and the device is out of reset. When this pin is low the regulators are disabled.
- **HIB_REG_ON_IN**: Used by the Hibernation (HIB) block to power up the internal BCM43903 regulators. If the HIB_REG_ON_IN pin is low, the regulators are disabled. For the HIB_REG_ON_IN pin to work as designed, HIB_REG_ON_OUT must be connected to REG_ON.

Note: The BCM43903 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.

Note: The 10%–90% VBAT rise time should not be faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

Control Signal Timing Diagrams

Figure 18: REG_ON = High, No HIB_REG_ON_OUT Connection to REG_ON

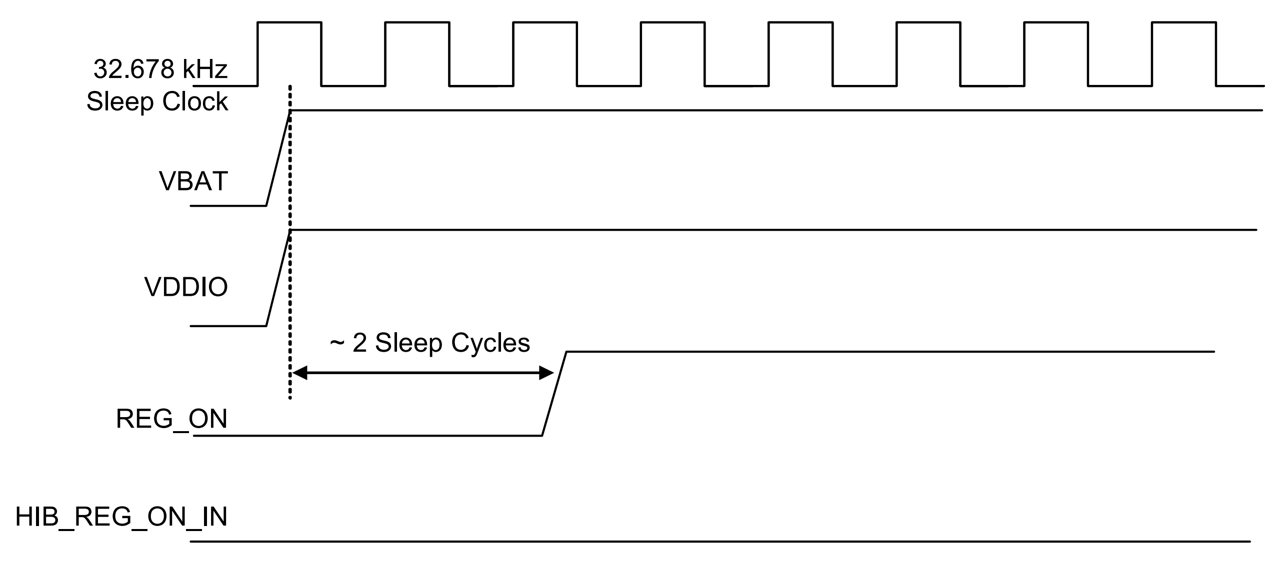
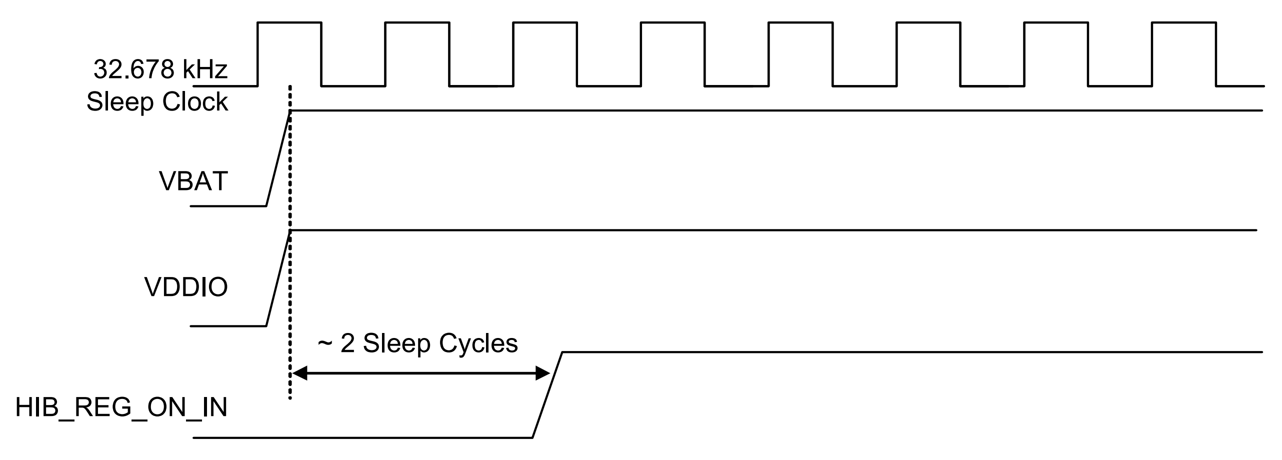


Figure 19: HIB_REG_ON_IN = High, HIB_REG_ON_OUT Connected to REG_ON



Section 19: Thermal Information

Package Thermal Characteristics

Table 31: Package Thermal Characteristics[a]

Characteristic	*WLBGA*
θ_{JA} (°C/W) (value in still air)	31.72
θ_{JB} (°C/W)	3.95
θ_{JC} (°C/W)	2.16
Ψ_{JT} (°C/W)	4.3
Ψ_{JB} (°C/W)	9.28
Maximum Junction Temperature T_j (°C)	113.9
Maximum power dissipation (W)	1.38

[a] No heat sink, TA = 70°C. This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51–7. Air velocity is 0 m/s.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

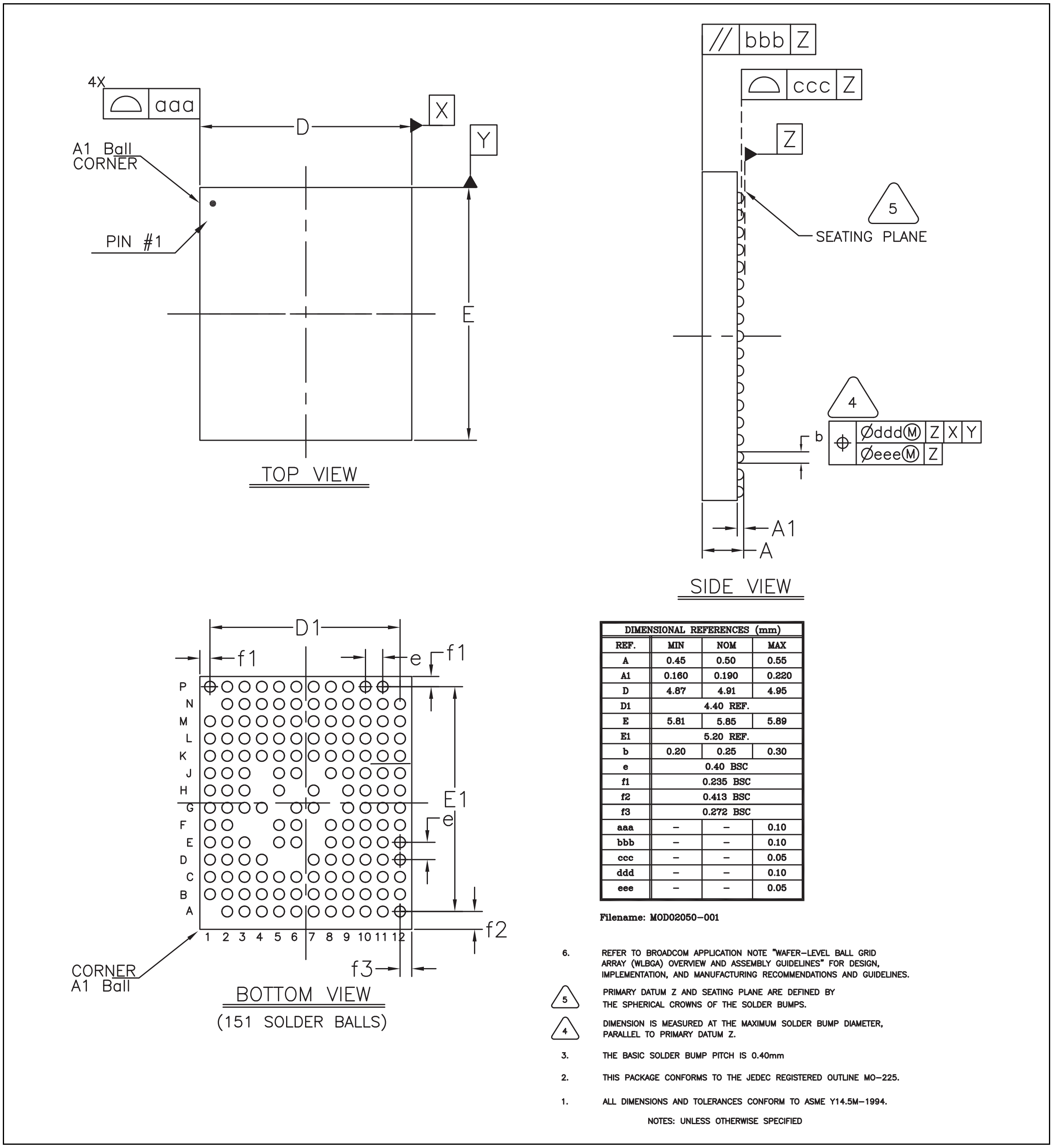
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see Table 13: “Environmental Ratings,” on page 58.

Section 20: Mechanical Information

Figure 20: WLBGA Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.87	4.91	4.95
D1	4.40 REF.		
E	5.81	5.85	5.89
E1	5.20 REF.		
b	0.20	0.25	0.30
e	0.40 BSC		
f1	0.235 BSC		
f2	0.413 BSC		
f3	0.272 BSC		
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD02050–001

6. REFER TO BROADCOM APPLICATION NOTE "WAFER–LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

△5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

△4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 21: Ordering Information

Part Number	*Package*	*Description*	*Operating Ambient Temperature*
BCM43903KUBG	4.91 mm x 5.85 mm, 0.4 mm ball pitch, 151-pin WLBGA	–	–30°C to +85°C

Broadcom
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