ARIZONA MICROTEK, INC.

AZ10E142
AZ100E142

ECL/PECL 9-bit Shift Register

FEATURES

- 700 MHz Minimum Shift Frequency
- 9-Bit for Byte-Parity Application
- Asynchronous Master Reset
- Dual Clocks
- Operating Range of 4.2V to 5.46V
- 75kΩ Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10E142 & MC100E142

PACKAGE AVAILABILITY

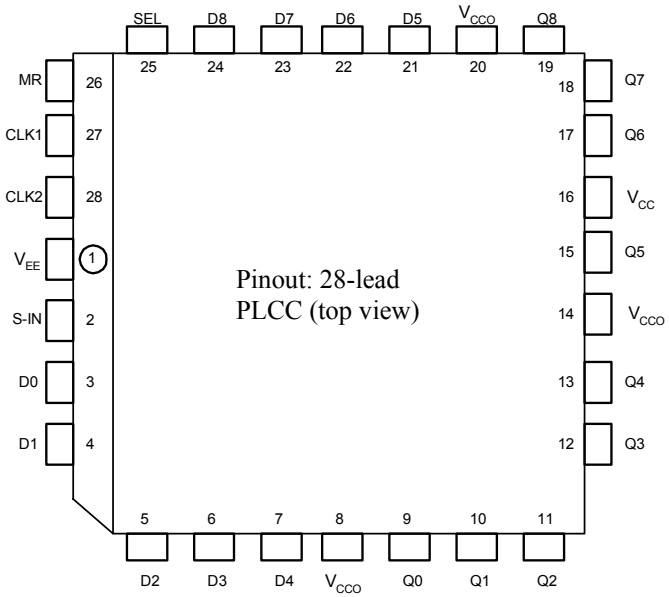
PACKAGE	PART NO.	MARKING
PLCC 28	AZ10E142FN	AZM10E142
PLCC 28 T&R	AZ10E142FNR2	AZM10E142
PLCC 28	AZ100E142FN	AZM100E142
PLCC 28 T&R	AZ100E142FNR2	AZM100E142

DESCRIPTION

The AZ10/100E142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0-D8 accept parallel input data, while S-IN accepts serial input data. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

The SEL (Select) input pin is used to switch between the two modes of operation – SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.



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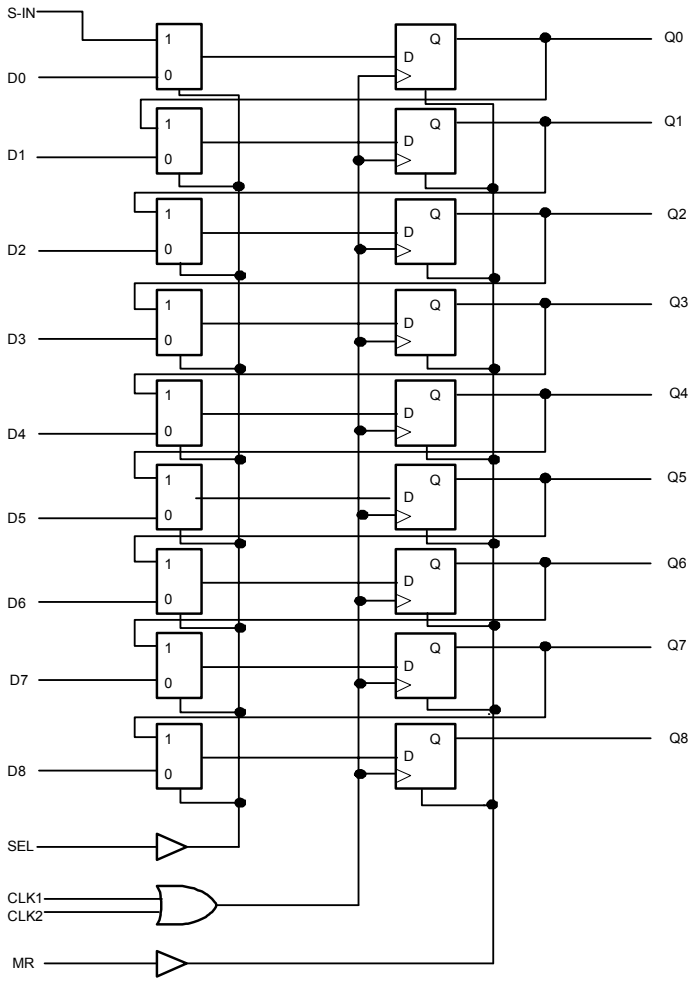
FUNCTION TABLE

SEL	MODE
L	Load
H	Shift

PIN DESCRIPTION

PIN	FUNCTION
D0 – D8	Parallel Data Inputs
S – IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0 – Q8	Data Outputs
V_{CC} , V_{CCO}	Positive Supply
V_{EE}	Negative Supply

LOGIC SYMBOL



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +8.0	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-8.0 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

10K ECL DC Characteristics (V_{EE} = -4.94V to -5.46V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
V_{OL}	Output LOW Voltage[1]	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V_{IH}	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		120	145		120	145		120	145		120	145	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

10K PECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3920		4110	3980		4160	4020		4190	4090		4280	mV
V_{OL}	Output LOW Voltage[1,2]	3050		3350	3050		3370	3050		3370	3050		3405	mV
V_{IH}	Input HIGH Voltage[1]	3770		4110	3830		4160	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage[1]	3050		3500	3050		3520	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		120	145		120	145		120	145		120	145	mA

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K ECL DC Characteristics (V_{EE} = -4.2V to -5.46V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		120	145		120	145		120	145		138	165	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = V_{CCO} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage[1]	3190		3525	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current		120	145		120	145		120	145		138	165	mA

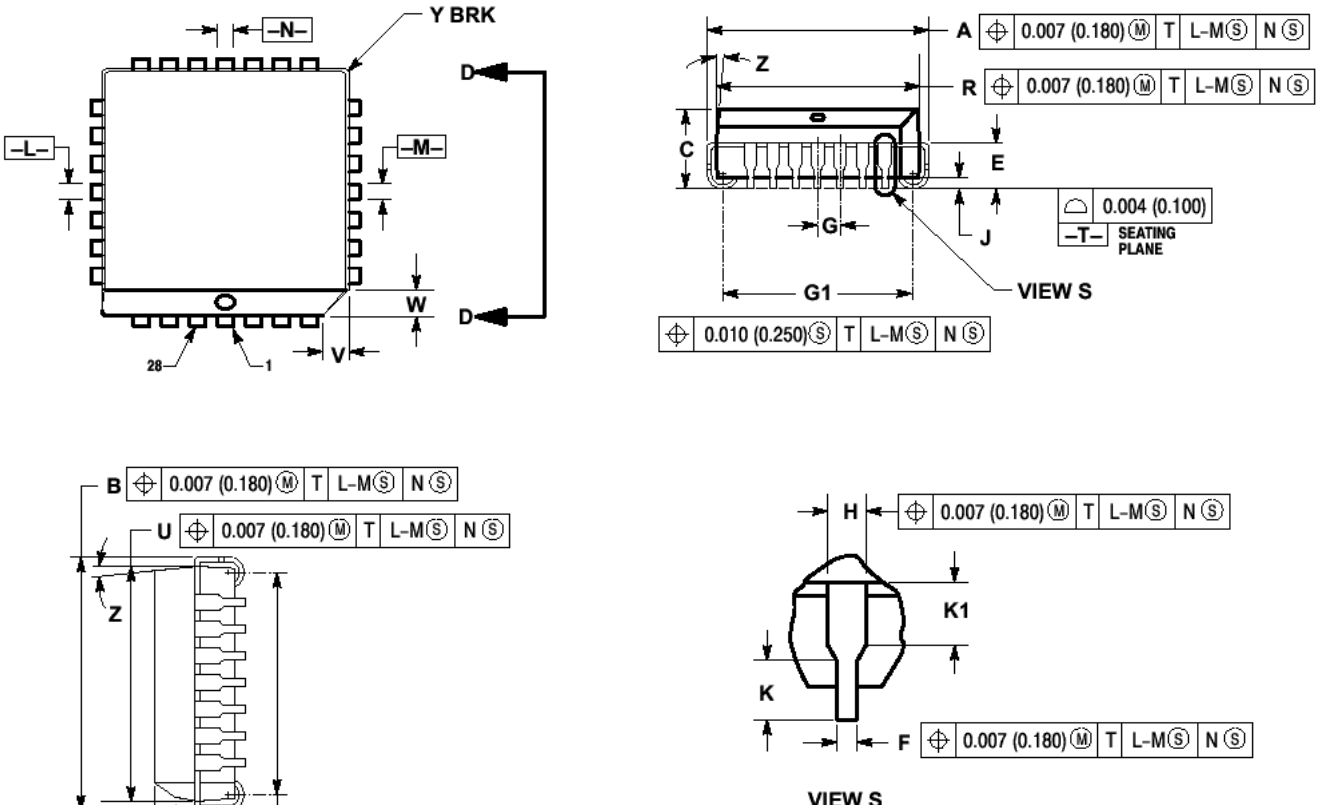
1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = 10E(-4.94V to -5.46V), 100E(-4.2V to -5.46V); V_{CC} = V_{CCO} = GND or V_{EE} = GND, V_{CC} = V_{CCO} = 10E(+4.94V to +5.46V), 100E(+4.2V to +5.46V))

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		700	900		MHz
t_{PLH} / t_{PHL}	Propagation Delay to Output CLK1, CLK2	600	800	1000	600	800	1000	600	800	1000	600	800	1000	ps
	MR	600	800	1000	600	800	1000	600	800	1000	600	800	1000	
t_S	Setup Time D	50	-100		50	-100		50	-100		50	-100		ps
	SEL	300	150		300	150		300	150		300	150		
t_H	Hold Time D	300	100		300	100		300	100		300	100		ps
	SEL	75	-150		75	-150		75	-150		75	-150		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width CLK1,CLK2, MR	400			400			400			400			ps
t_{SKEW}	Within-Device Skew[1]		75			75			75			75		ps
t_r / t_f	Rise/Fall Times 20% - 80%	300		800	300		800	300		800	300		800	ps

1. Within-device skew is defined as identical transitions on similar paths through a device.

PACKAGE DIAGRAM
PLCC 28



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
T		0.50		0.020
Z	2^{O}	10^{O}	2^{O}	10^{O}
G1	10.42	10.92	0.410	0.430
K1	1.02		0.040	

NOTES:
1. DATUMS –L-, -M-, AND –N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALOWABLE MOLD FLASH IS 0.010mm (0.250in.) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKGE BOTTOM BY UP TO 0.012mm (0.300in.). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025mm (0.635in.).