PU61C56

Silicon N-Channel Power F-MOS (with built-in zener diode)

Features

- Avalanche energy capability guaranteed
- Withstanding high electrostatic voltage
- Low-voltage drive possible

Applications

- Non-contact relay
- Solenoid drive
- Motor drive
- Control equipment
- Switching mode regulator

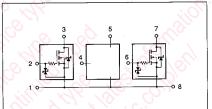
■ Absolute Maximum Ratings (T_C=25°C)

Parameter		Symbol	Rating	Unit	
Drain-Source breakdown voltage		V _{DSS}	37±7	V	
Gate-Source voltage		V _{GSS}	±20	V ·	
Drain current	DC	I_D	±6	A	
	Pulse	I_{DP}	±12	Α	
Avalanche energy capability		EAS*	200	mJ	
Allowable power dissipation	T _C =25℃	D	15	w	
	Ta=25℃	P_{D}	2.4		
Channel temperature		T _{ch}	150	,°C	
Storage temperature		T _{stg}	-55 to +150	${\mathfrak C}$	

^{*}L=11.2mH, $I_L=6$ A, $V_{DD}=50$ V, 1 pulse

Unit: mm 20 2±0.3 4.0±0.2 0.8±0.25 0.5±0.15 2.5±40.2 7×2.54=17.78±0.25 G: Gate D: Drain S: Source 8-Lead Plastic SIL Package

■ Internal Connection

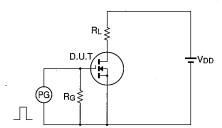


Power Tr. Arrays

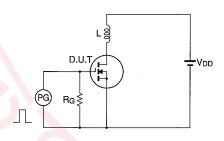
■ Electrical Characteristics (T_C=25°C)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Drain-Source cut-off current	I _{DSS}	$V_{DS}=25V, V_{GS}=0$	$Q_{D,i}$ (4)		10	μ A
Gate-Source leakage current	I _{GSS}	$V_{GS}=\pm 20V, V_{DS}=0$			10	μ A
Drain-Source breakdown voltage	$V_{\rm DSS}$	$I_D=1$ mA, $V_{GS}=0$	30		44	V
Gate threshold voltage	V _{th}	$V_{DS}=10V$, $I_D=1mA$	1.2		2.5	V
Drain-Source ON-resistance	R _{DS(on)} 1	$V_{GS}=10V$, $I_D=3A$		110	140	mΩ
	R _{DS(on)} 2	$V_{GS}=4V$, $I_D=3A$		160	220	$m\Omega$
Forward transadmittance	Y _{fs}	$V_{DS}=10V$, $I_{D}=3A$	2.5	4		S
Diode forward voltage	V _{DSF}	$I_{DR}=6A$, $V_{GS}=0$			-1.7	V
Input capacitance	Ciss	V _{DS} =10V, V _{GS} =0, f=1MHz		40		pF
Output capacitance	Coss			300		pF
Feedback capacitance	C _{rss}		-	20		pF
Turn-on time	t _{on}	TI TOTT I OA		1		μs
Fall time	t _f	$V_{GS}=10V$, $I_D=3A$		2		μs
Turn-off time (delay time)	t _{d (off)}	$V_{DD}=30V, R_{L}=10\Omega$		1		μs
Channel-Case heat resistance	R _{th (ch-c)}				8.33	°C/W

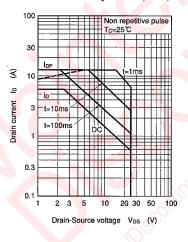
Switching measurement circuit



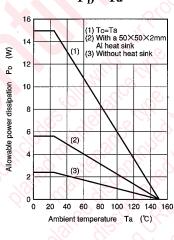
Avalanche capability test circuit



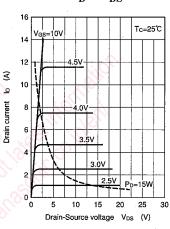
Area of safe operation (ASO)



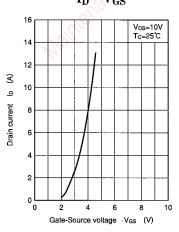
 P_D —Ta



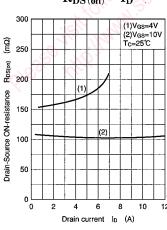
 $I_D - V_{DS}$



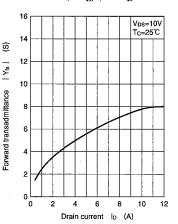
 $I_D - V_{GS}$

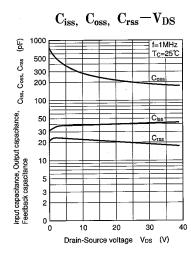


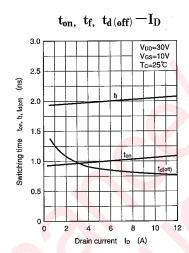
 $R_{DS(on)}-I_D$

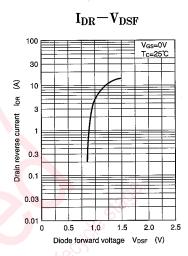


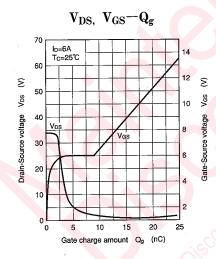
 $\mid \mathbf{Y}_{\mathrm{fs}} \mid -\mathbf{I}_{\mathrm{D}}$











Pow Tr. Array

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