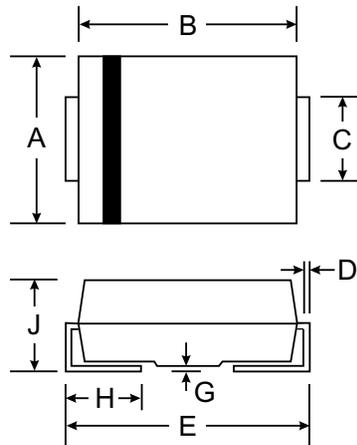


Features

- Metal-Semiconductor junction with guard ring
- Epitaxial construction
- Low forward voltage drop, low switching losses
- High surge capability
- For use in low voltage, high frequency inverters free wheeling, and polarity protection applications
- The plastic material carries U/L recognition 94V-0

Mechanical Data

- Case: JEDEC SMC, molded plastic
- Terminals: Solderable per MIL-STD-202, method 208
- Polarity: Color band denotes cathode
- Weight: 0.007 ounces, 0.21 grams
- Mounting position: Any



SMC		
Dim	Min	Max
A	5.40	6.22
B	6.10	7.11
C	2.92	3.18
D	0.15	0.40
E	7.55	8.13
G	0.10	0.21
H	0.76	1.52
J	2.00	2.62
All Dimensions in mm		

Maximum Ratings and Electrical Characteristics

Rating at 25 °C ambient temperature unless otherwise specified.
 Single phase, half wave, 60 Hz, resistive or inductive load.
 For capacitive load, derate current by 20%.

		S5820	S5821	S5822	UNITS
Maximum recurrent peak reverse voltage	V_{RRM}	20	30	40	V
Maximum RMS voltage	V_{RMS}	14	21	28	V
Maximum DC blocking voltage	V_{DC}	20	30	40	V
Maximum average forward rectified current @ $T_L = 90^\circ C$	$I_{F(AV)}$	3.0			A
Peak forward surge current 8.3ms single half-sine-wave superimposed on rated load @ $T_J = 125^\circ C$	I_{FSM}	80.0			A
Maximum instantaneous forward voltage @ 3.0A (Note 1) @ 9.4A	V_F	0.475 0.85	0.50 0.90	0.525 0.95	V
Maximum reverse current @ $T_A = 25^\circ C$ at rated DC blocking voltage @ $T_A = 100^\circ C$	I_R	2.0 20.0			mA
Typical junction capacitance (Note2)	C_J	250			pF
Typical thermal resistance (Note3)	$R_{\theta JA}$	20			$^\circ C/W$
Operating junction temperature range	T_J	- 55 ---- + 125			$^\circ C$
Storage temperature range	T_{STG}	- 55 ---- + 150			$^\circ C$

NOTE: 1. Pulse test : 300 μ s pulse width, 1% duty cycle.
 2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.
 3. Thermal resistance junction to ambient

FIG.1 – FORWARD DERATING CURVE

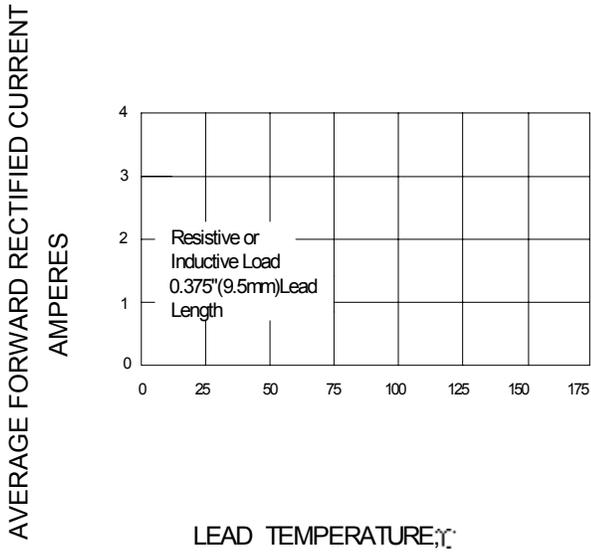


FIG.2 – PEAK FORWARD SURGE CURRENT

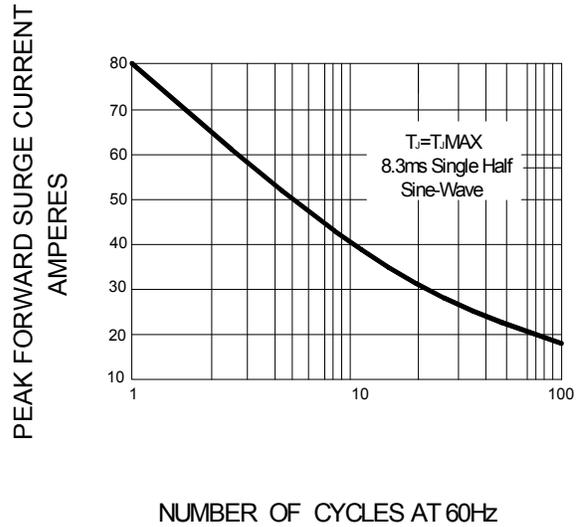


FIG.3 – TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

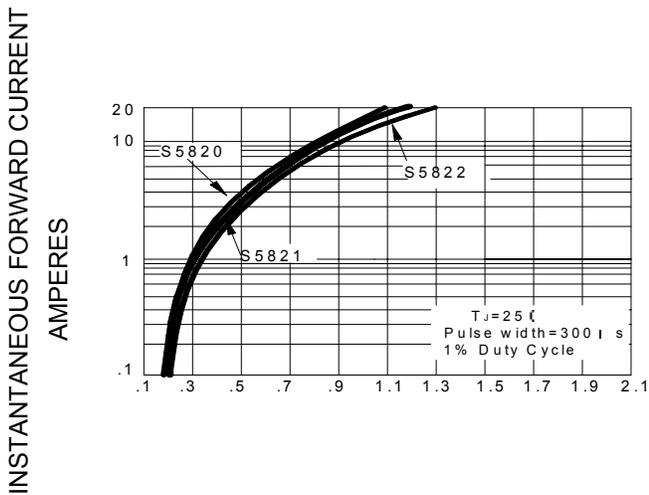


FIG.4 – TYPICAL JUNCTION CAPACITANCE

