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April 1st, 2010
Renesas Electronics Corporation

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HD74HC78

Dual J-K Flip-Flops

(with Preset, Common Clear and Common Clock)

REJ03D0553-0200
 (Previous ADE-205-425)
 Rev.2.00
 Oct 06, 2005

Description

This flip-flop is edge sensitive to the clock input and change state on the negative transition of the clock pulse. Each flip-flop has independent J, K, and preset inputs and Q and \bar{Q} outputs. Two flip-flops are controlled by a common clear and a common clock. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.






Features

- High Speed Operation: t_{pd} (Clock to Q) = 20 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC78FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74HC78RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

		Inputs			Outputs	
Preset	Clear	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{*1}	H^{*1}
H	H		L	L	No change	
H	H		L	H	L	H
H	H		H	L	H	L
H	H		H	H	Toggle	
H	H	L	X	X	No change	
H	H	H	X	X	No change	
H	H		X	X	No change	

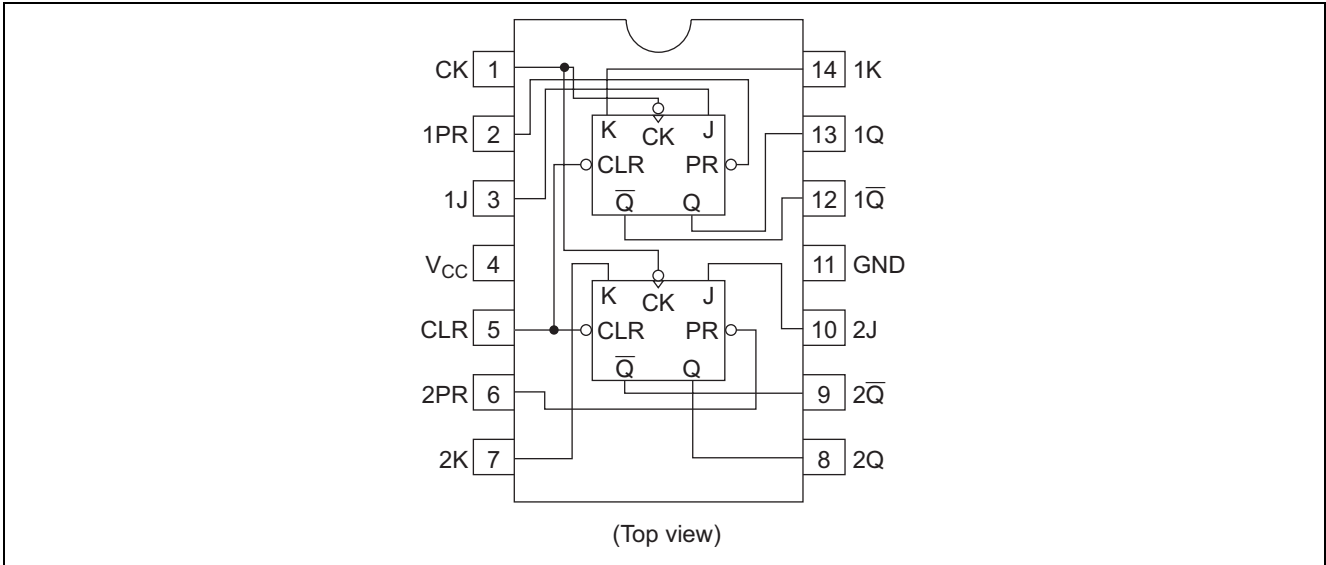
H: High level

L: Low level

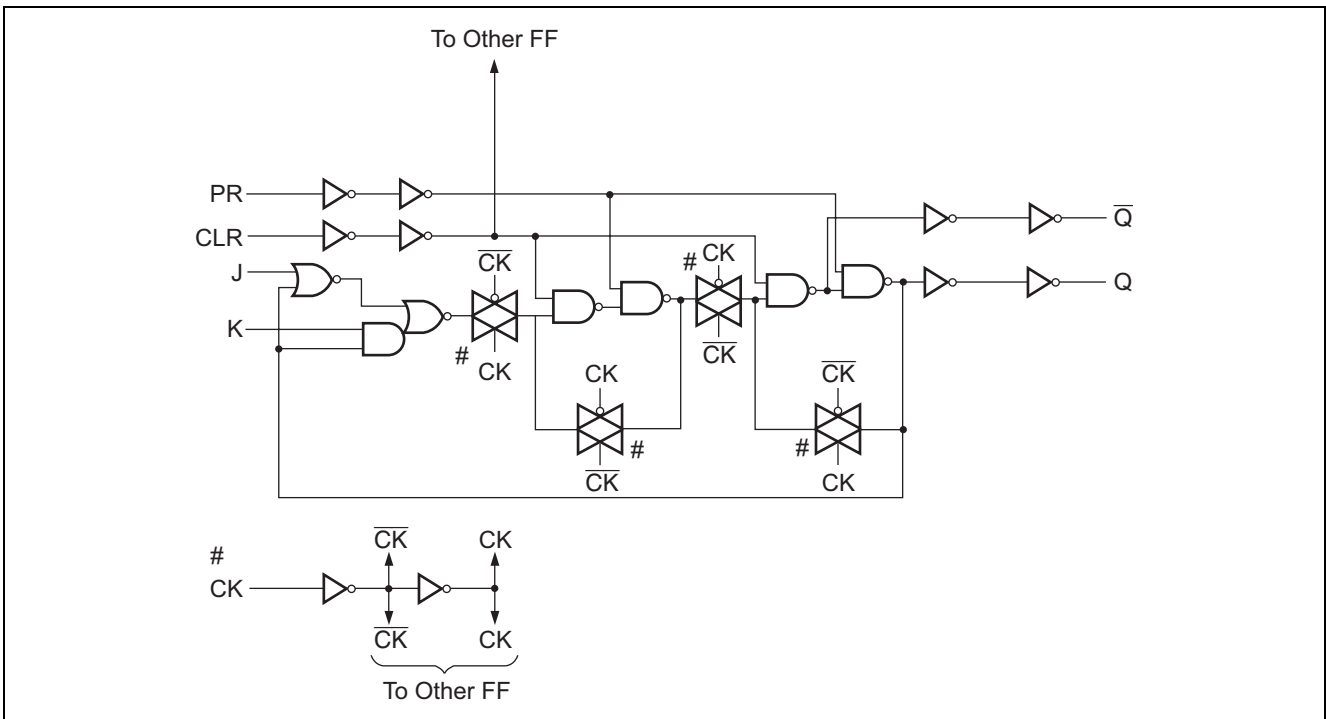
X: Irrelevant

Note: 1. Q and \bar{Q} will remain High as long as Preset and Clear are Low, but Q and \bar{Q} are unpredictable, if Preset and Clear go High simultaneously.

Pin Arrangement



Logic Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time *1	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

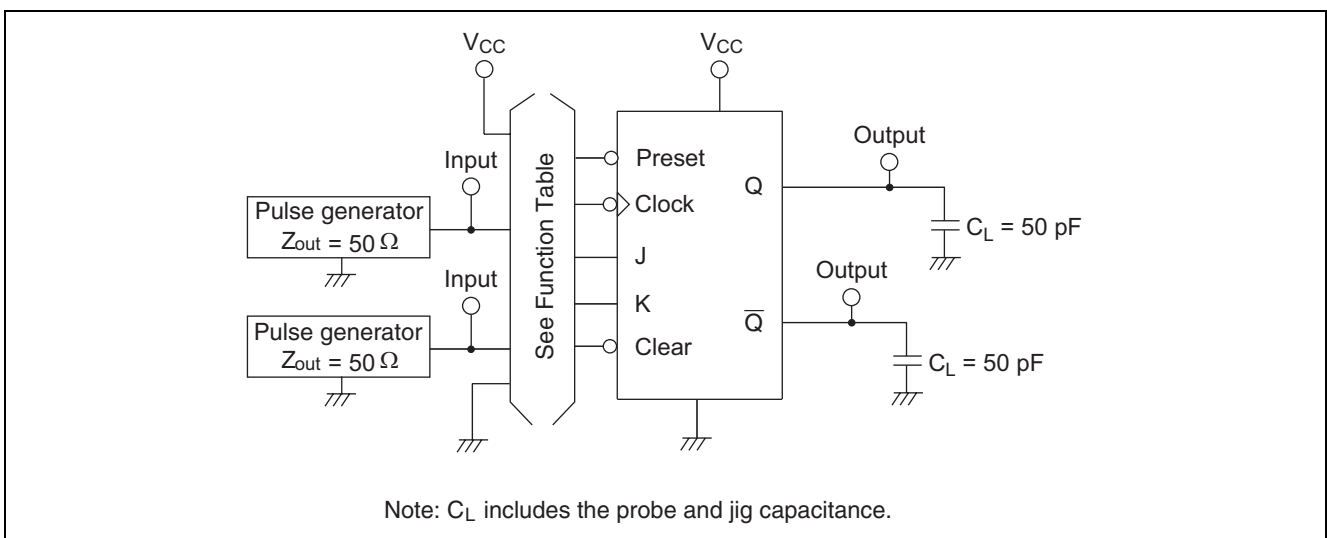
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V_{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$	
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$	
		4.5	4.18	—	—	4.13	—				
		6.0	5.68	—	—	5.63	—				
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33				$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33				$I_{OL} = 5.2\ \text{mA}$
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND		
Quiescent supply current	I_{CC}	6.0	—	—	2.0	—	20	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0\ \mu\text{A}$		

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

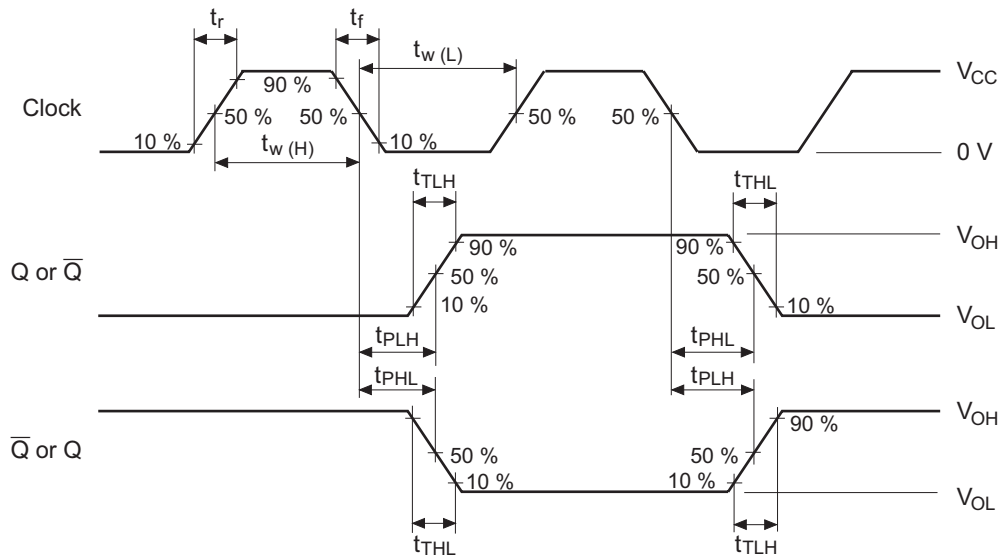
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz			
		4.5	—	—	30	—	24				
		6.0	—	—	35	—	28				
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	150	—	190	ns	Clock to Q or \bar{Q}		
		4.5	—	20	30	—	38				
		6.0	—	—	26	—	33				
				2.0	—	—	140	—	175	ns	Clear to Q or \bar{Q}
				4.5	—	18	28	—	35		
				6.0	—	—	24	—	30		
				2.0	—	—	140	—	175	ns	Preset to Q or \bar{Q}
				4.5	—	18	28	—	35		
				6.0	—	—	24	—	30		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Preset, Clear, Clock		
		4.5	16	8	—	20	—				
		6.0	14	—	—	17	—				
Setup time	t_{su}	2.0	100	—	—	125	—	ns	J or K to Clock		
		4.5	20	2	—	25	—				
		6.0	17	—	—	21	—				
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to J or K		
		4.5	5	-1	—	5	—				
		6.0	5	—	—	5	—				
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	Preset or Clear to Clock		
		4.5	20	0	—	25	—				
		6.0	17	—	—	21	—				
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns			
		4.5	—	5	15	—	19				
		6.0	—	—	13	—	16				
Input capacitance	C_{in}	—	—	5	10	—	10	pF			

Test Circuit

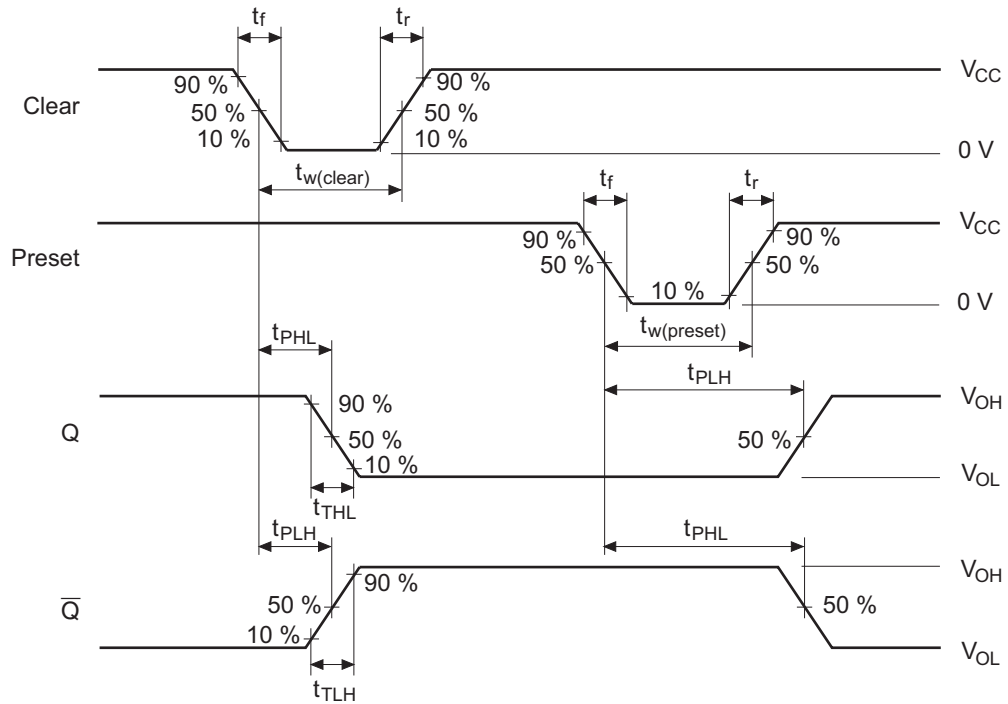


Waveforms

• Waveform – 1

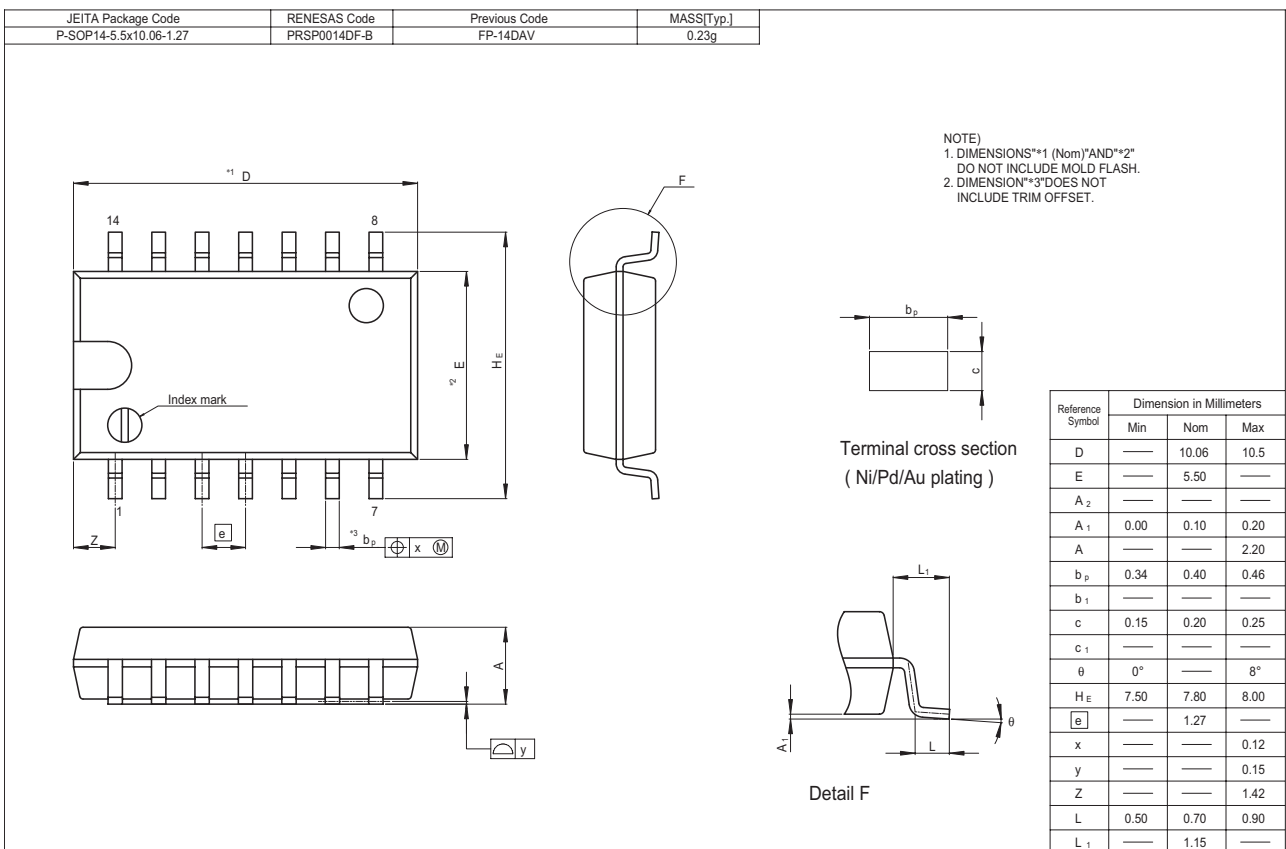
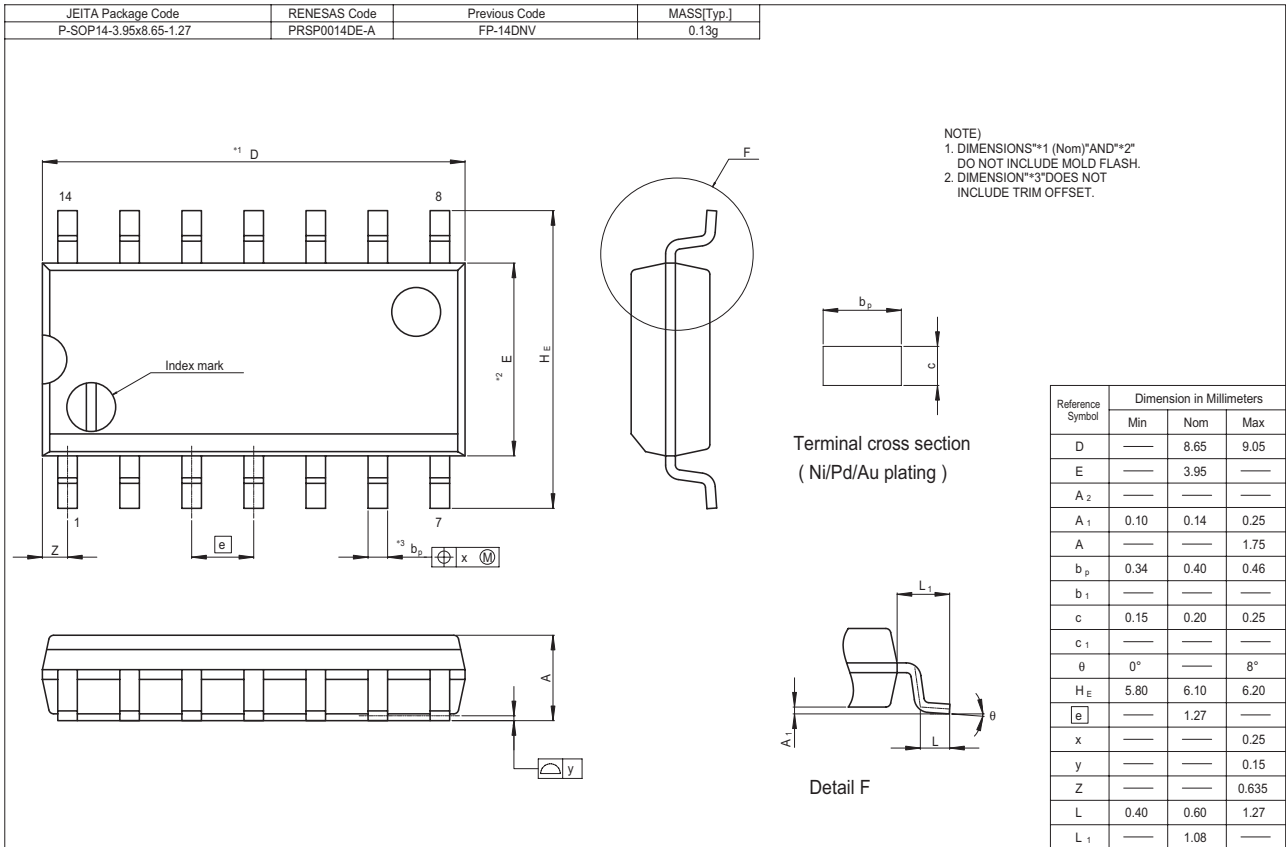


• Waveform – 2



- Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions



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