



## Low Voltage Differential (LVD) SCSI 27 Line Regulator Set

### Features

- SCSI SPI-2 (Ultra 2) LVD SCSI 27 Line Low Voltage Differential Regulator
- 4.0V to 5.25V Operation
- Integrated Regulator Set for LVD SCSI
- Differential Failsafe Bias

### Applications

- SCSI cable
- SCSI card
- Disk Array
- Industrial PC
- POS

### Description

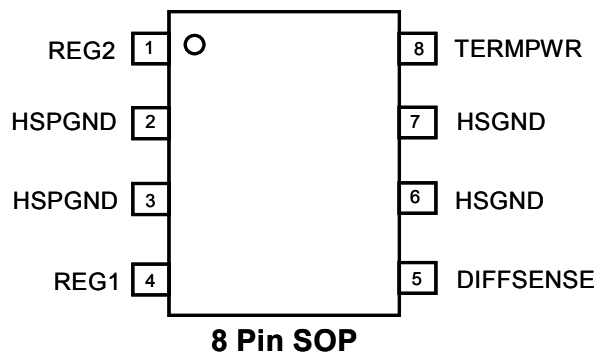
The G261 LVD Regulator set is designed to provide the correct reference voltages and bias currents for LVD termination resistor networks (475Ω, 121Ω, and 475Ω) The device also provides a 1.3V output for DIFFSENSE signaling. With the proper resistor network, the G261 solution will meet the common mode impedance, differential mode impedance, differential bias voltage and common mode voltage requirements of SPI-2 (Ultra2).

This device contains two sink / source reference voltage regulators, a 1.3V buffered output and protection features. The protection features include thermal shutdown and active current limiting circuitry. The G261 is offered in 16pin SOP.

### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
G261P1	-40°C~80°C	8 Pin SOP

### Pin Configuration





Absolute Maximum Ratings

TERMPWR.....6V
Package Dissipation.....1W
Junction Temperature.....-55°C to 150°C
Storage Temperature.....-65°C to 150°C

Recommended Operating Conditions

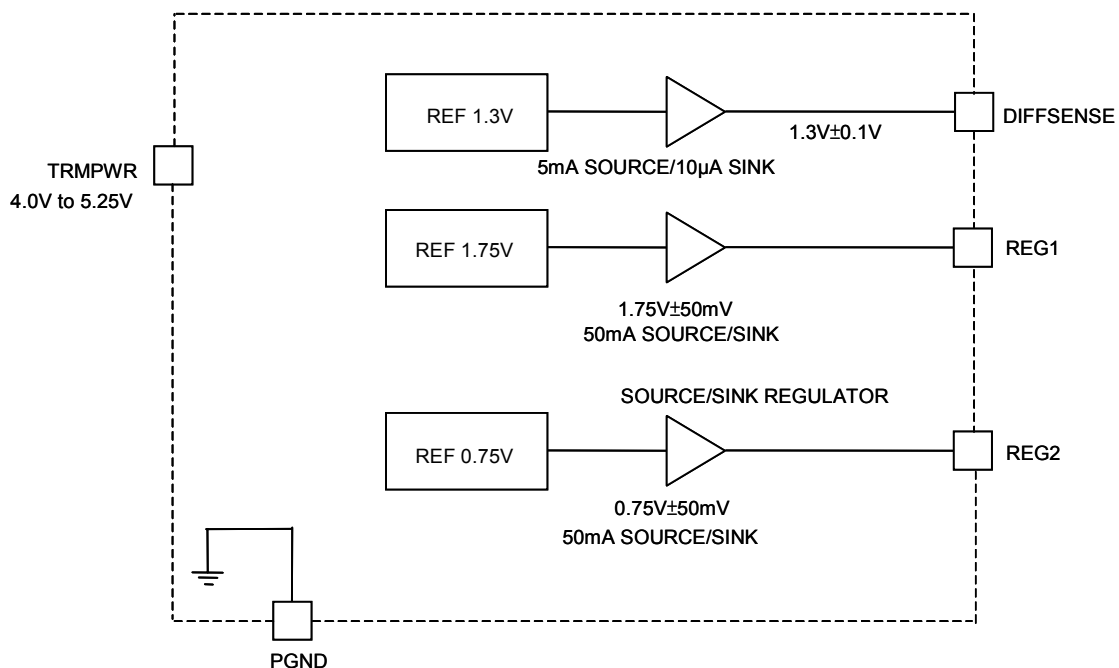
TERMPWR Voltage.....4.0V to 5.25V

Electrical Characteristics

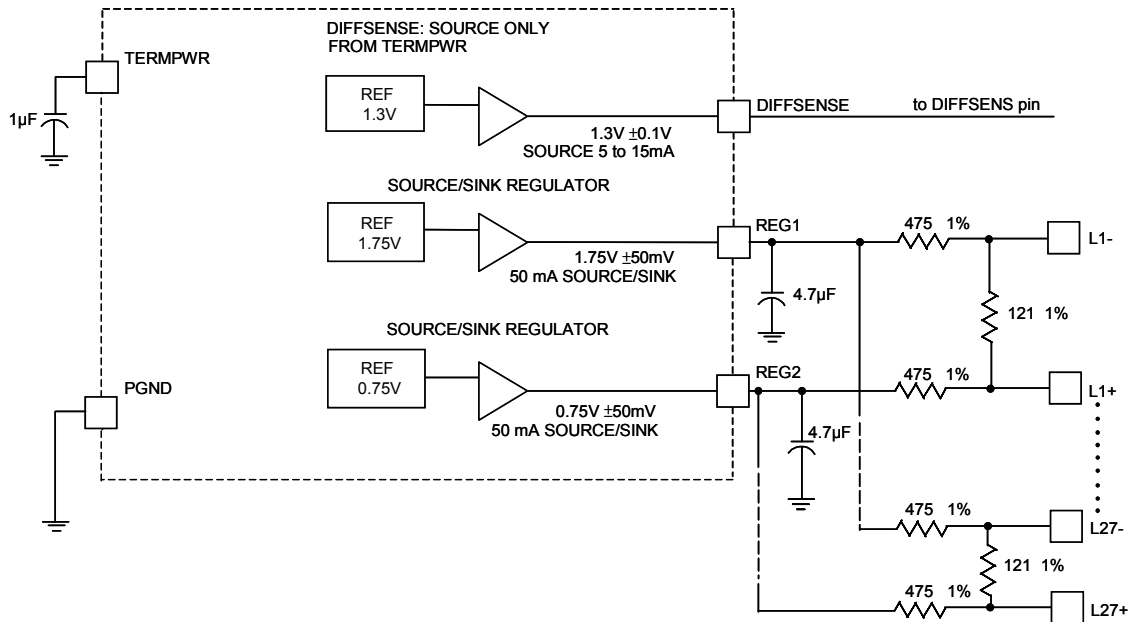
Unless otherwise specified these specifications apply for TA= 0°C to 70°C,TERMPWR=5V.

Table with 6 columns: PARAMETER, TEST CONDITIONS, MIN, TYP, MAX, UIMITS. Rows include TERMPWR Supply Current Section and Regulator Section.

Block Diagram



**Application Information**



**Figure 1. LVD SCSI Discrete Resistor Stack**

**Table1. Resistor Network v.s Standard**

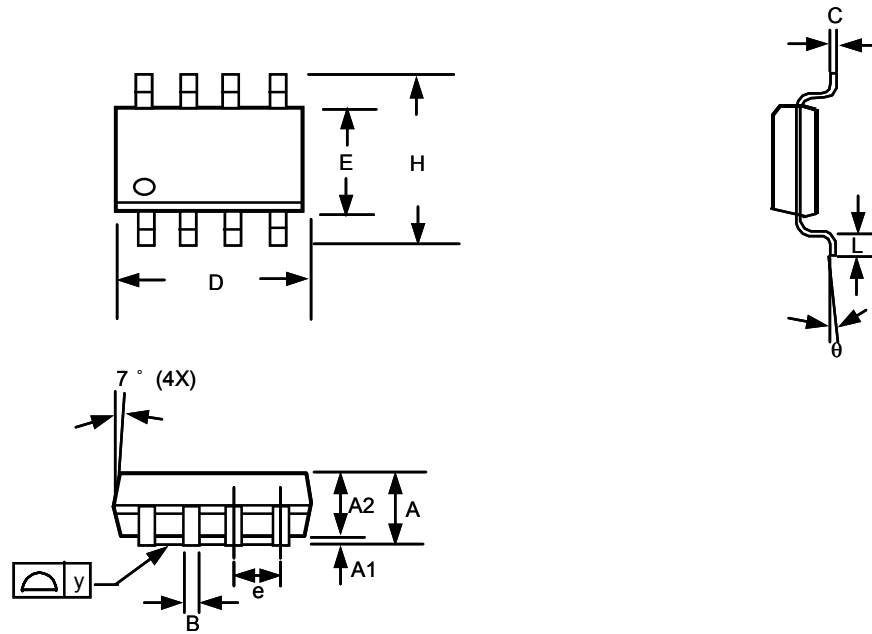
Outputs	Specification
107.3Ω Diff	100Ω to 110Ω
112.9mV Diff Bias	100mV to 125mV
237Ω Common Mode	100Ω to 300Ω
1.25V Common Mode	1.2V to 1.30V

**Application Note:** The resistor network, along with the 1.75V and 0.75V references will give the correct differential impedance, bias voltage, common mode impedance and common mode voltage as show in Table 1.

**Layout guideline:**

1. For stable operation, the 1µF capacitor on TERMPWR pin and 4.7µF capacitors on REG1 and REG2 pins must be placed within 0.25 inch of their respective pins.
2. The PCB trace length from Lx- and Lx+ to the connector pins (all 27pairs) must be of equal length, in order to minimize the signal skew among these pairs. In addition, these traces must be as short as possible, in order to minimize capacitance.

## Package Information



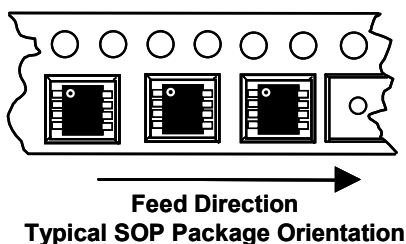
**8-Pin SOP**

**Note:**

- 1.Package body sizes exclude mold flash and gate burrs
- 2.Dimension L is measured in gage plane
- 3.Tolerance 0.10mm unless otherwise specified
- 4.Controlling dimension is millimeter converted inch dimensions are not necessarily exact.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	----	1.45	----	----	0.057	----
B	0.33	----	0.51	0.013	----	0.020
C	0.19	----	0.25	0.007	----	0.010
D	4.80	----	5.00	0.189	----	0.197
E	3.80	----	4.00	0.150	----	0.157
e	----	1.27	----	----	0.050	----
H	5.80	----	6.20	0.228	----	0.244
L	0.40	----	1.27	0.016	----	0.050
y	----	----	0.10	----	----	0.004
$\theta$	0°	----	8°	0°	----	8°

## Taping Specification



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