COMPUTER LABS
ANALOG DEVICES

DGM-1040 and -1080
D/A Deglitchers

General

Deglitchers are normally used to eliminate the non-linear effects of "glitches" from the output of D/A converters. The Computer Labs DGM Series of Deglitchers may be used with almost any type of D/A converter to generate an output signal with extremely high spectral purity. These Deglitchers have been used for television signal reproduction, CRT displays, waveform generation, and automatic test equipment, to name a few.

The Problem

In most instances, fast-settling D/A converters are current-switching types, rather than voltage types. In this type of converter, any input bit changing causes a change in the output current of the converter.

The input circuits for current-switching D/A's, and their TTL or DTL driving logic, are subject to the characteristic of saturated logic which causes propogation delay for negative-going inputs to be different from the delay for positive-going inputs.

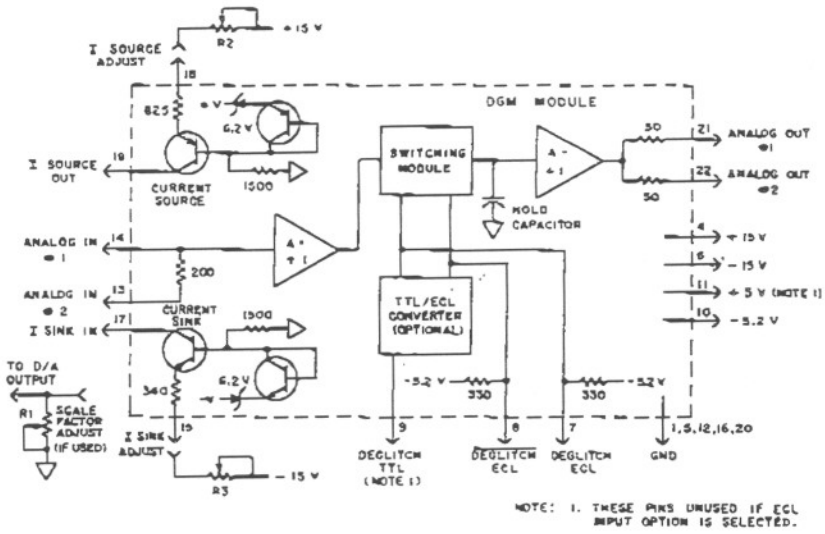
As a result of this phenomenon, time skew of the individual current switches within the D/A converter is worst when one or more input bits are out of phase with the others. This is true even for ideal inputs in which the digital input bits arrive simultaneously; if there is time skew among the bit inputs, the problem becomes even more pronounced.

These differences among the internal switches cause a discontinuity or "glitch" in the output current of the D/A converter. The true "worst case" glitch always occurs at the switching point of the Most Significant Bit (MSB) or the center point of the output range, because nearly equal and opposite currents are being switched.

In addition to this inescapable switching transient in the output,

Features

- 15 nsec acquisition time.
- 0.01% linearity.
- Directly interfaces with ultra high-speed, current-output D/A's.
- TTL or ECL compatible.
- DGM plus D/A costs less than any "deglitched" D/A available.



DGM SERIES BLOCK DIAGRAM

most current-output D/A converters also have a maximum output voltage limitation.

Part of this limitation may be the result of high output capacitance and/or resistance; this characteristic can be "masked" in data sheets if settling time is specified with an impractically-low impedance load.

Even D/A converters which have low output capacitance and/or resistance will have a maximum output voltage limitation which is established by saturation of the internal switching transistors.

This internal saturation, in turn, generally precludes operating the current-switching D/A converter as effectively in a unipolar mode as it can be operated in a bipolar output mode.

NOTE: Additional details on the characteristics of current-switching, fast-settling D/A Converters are included in "Notes on Fast-settling D/A Converters", which are part of the data sheet on the Computer Labs MDS/MDP Series D/A's.

The Solution

When first exposed to the undesirable effect of analog discontinuities in the outputs of current-switching D/A converters, many users erroneously assume two straight-forward approaches will solve the problem. At the input, minimizing time skew among the data bit inputs will be a useful technique. At the output, the use of a filter may also appear to be a neat "solution" to the problem.

Unfortunately, no amount of time alignment on the input bits will overcome the physical laws associated with the propogation delays of saturated logic discussed earlier. In addition, a filter designed for eliminating the "glitch" at the major carry point will not be optimized for transients at other points of the output, nor will it change the relationship of transient amplitudes; this is because the glitch is a function of signal dynamics. As a result, a multitude of intermodulation products are formed; some of these IM products appear in the video pass-band as spurious signals, and increased noise level.

Besides these considerations, no amount of minimizing time skew

AC CHARACTERISTICS

	DGM-1040	DGM-1080	
Acquisition Time	15 nsec	75 nsec	See Fig. 2&3
Sample Rate (max)	30 MHz	11 MHz	
Sample Delay TTL	10 nsec	10 nsec	See Fig. 2
ECL	6 nsec	6 nsec	
Droop Rate	8 mV/usec	1 mV/usec	
Harmonic Distortion	>60 dB	>60 dB	
Feedthru Rejection	>60 dB	>70 dB	
Pedestal	10 mV	2 mV	See Fig. 1
Residual Glitch	30 mV	20 mV	See Fig. 1
Output Noise Level	0.2 mV (RMS)	0.1 mV (RMS)	

DGM-1040 & DGM-1080

DC CHARACTERISTICS

Gain	.975
Offset	Adjustable to zero
Offset Drift	100 ppm/°C
Linearity	±0.01%
Current Source Current	7.5 mA max
Current Sink Current	19 mA max

ANALOG INPUT CHARACTERISTICS

Input Voltage	±2 V
Input Impedance	1 megohm
Input Bias Current	0.05 nA

ANALOG OUTPUT CHARACTERISTICS

Output Voltage (no load)	±2 V
Output Current	±50 mA
Output Impedance	50 ohms

DEGLITCH STROBE CHARACTERISTICS

Optionally either of the following:

TTL single line input		
"0" = track	0 to +0.4 V	2 standard TTL loads
"1" = hold	+2.4 to +4 V	
ECL 2 line complementary		
"0" = track	-1.7 V	These inputs are each terminated with a 330 ohm pull-down resistor to -5.2 V.
"1" = hold	-0.8 V	

POWER REQUIREMENTS

+15 V @ 100 mA w/o current source connected
-15 V @ 100 mA w/o current source connected
+5 V @ 20 mA } TTL input option
-5.2 V @ 80 mA }
-5.2 V @ 24 mA ECL input option

PHYSICAL CHARACTERISTICS

Package Size	2.3" by 2.3" by 0.43" 58 mm by 58 mm by 11 mm
Weight	3 oz 85 grams
Pins	0.040 diameter gold plated
Case	diallyl phthalate per MIL-M-14 type SDG-F

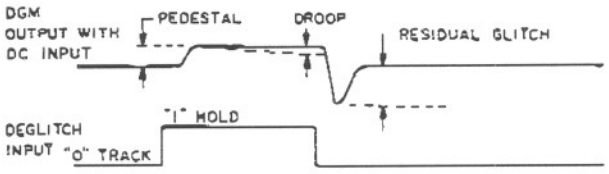


FIG. 1
DGM OUTPUT – DC INPUT

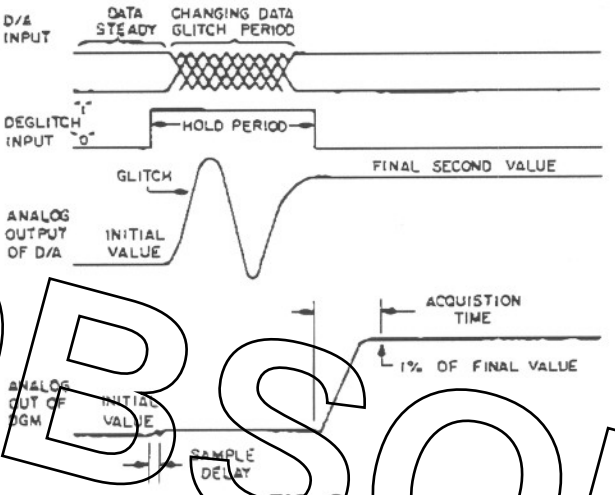


FIG. 2
DGM OUTPUT – D/A INPUT

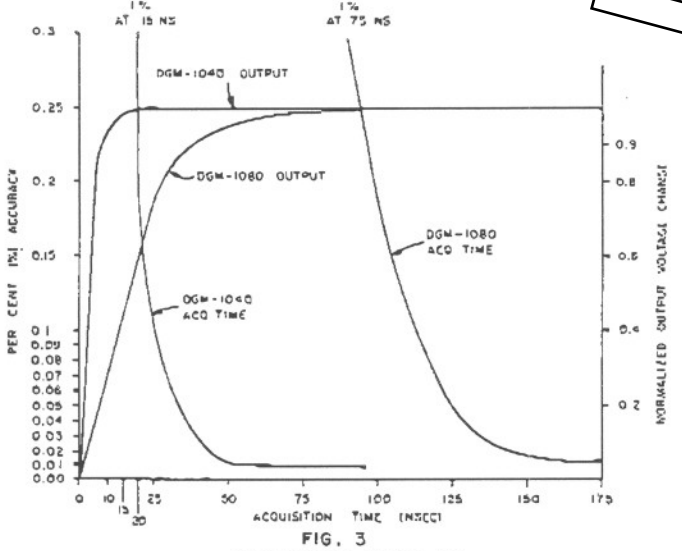
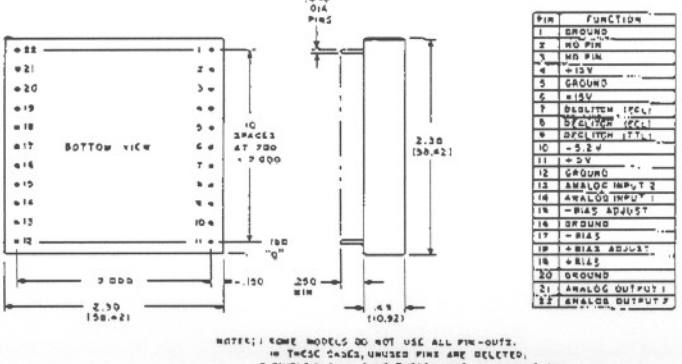


FIG. 3
ACQUISITION TIME VS.
SETTLING ACCURACY



PIN	FUNCTION
1	GROUND
2	NO PIN
3	NO PIN
4	+15V
5	GROUND
6	+15V
7	DEGLITCH (ECL)
8	DEGLITCH (ECL)
9	DEGLITCH (TTL)
10	-5.2V
11	+5V
12	GROUND
13	ANALOG INPUT 2
14	ANALOG INPUT 1
15	-BIAS ADJUST
16	GROUND
17	-BIAS
18	+BIAS ADJUST
19	+BIAS
20	GROUND
21	ANALOG OUTPUT 1
22	ANALOG OUTPUT 2

NOTES: 1 SOME MODELS DO NOT USE ALL PIN-OUTS.
IN THESE CASES, UNUSED PINS ARE DELETED.
2 DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS.

and/or filtering the output will overcome the output voltage limitations imposed by internal switching transistor saturation.

An optimum solution to the problem of glitches would cause the glitch to remain constant, regardless of the transition points on the input data. As an example, it should remain the same for the transition from 0 000 000 001 to 1 000 000 000; as it is for the transition from 1 000 000 000 to 1 000 000 001; or any other two input words.

Ideally, an optimum solution to the glitch problem would also permit using the full current drive capabilities of the current-switching D/A converter in both bipolar and unipolar modes of operation.

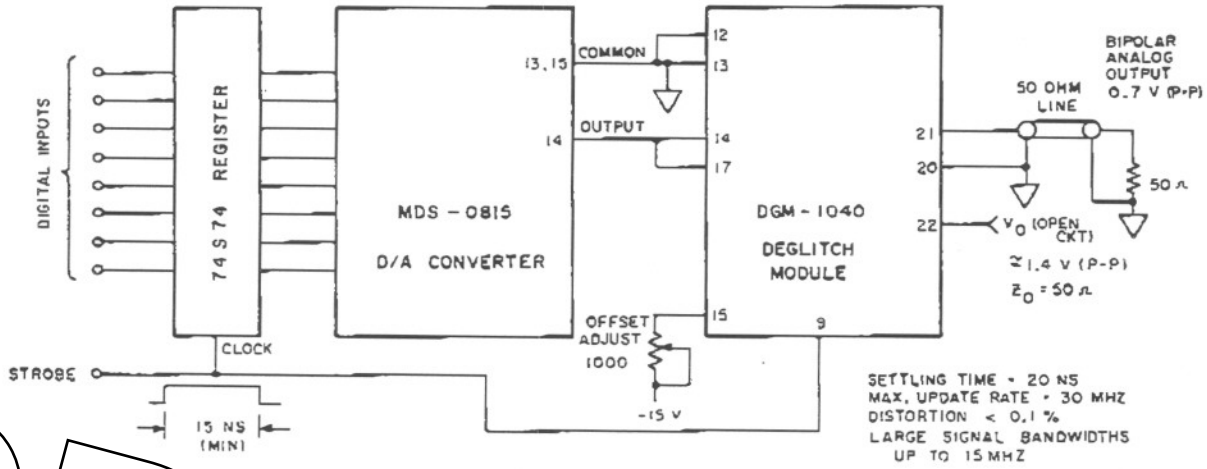
The purpose of the Computer Labs DGM modules is to reduce the amplitude of the glitch to an acceptable level, and more importantly, to provide a constant-amplitude glitch. This will hold the area under the curve at a constant value; **the modules are not intended to get rid of all glitches per se.**

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line, i.e., a single-line spectrum at the sample rate frequencies, and harmonics of the sample frequency.

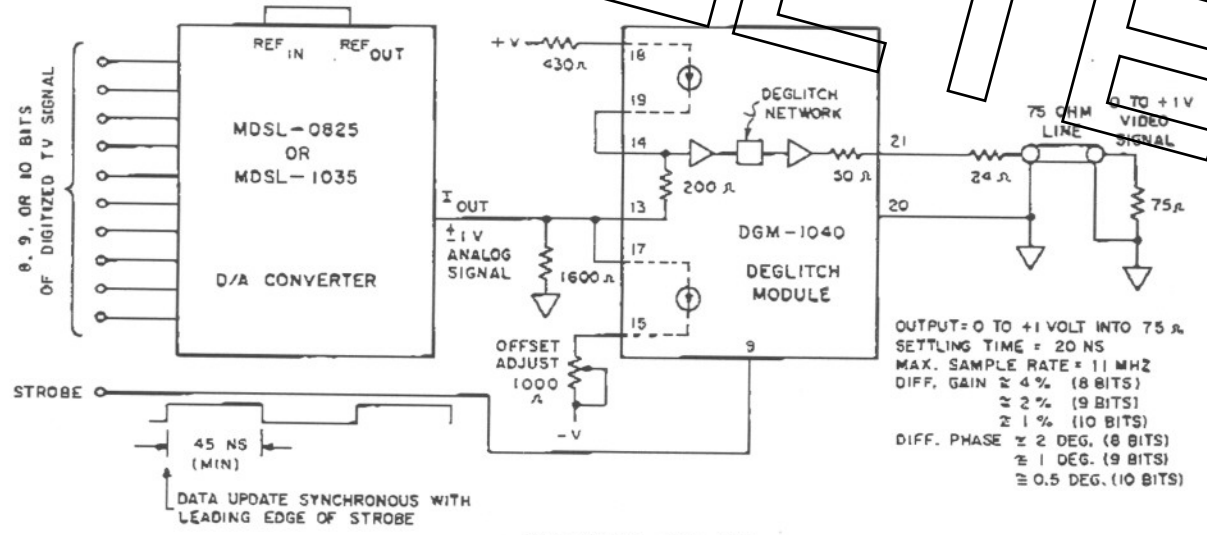
The deglitcher circuits effectively eliminate the intermodulation products discussed earlier. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is $q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

The DGM modules also incorporate an internal adjustable current sink, to adjust the D/A output for bipolar operation. In addition, an internal voltage shifter consisting of a current source and a precision resistor allows using the bipolar output drive capabilities of the D/A converter for unipolar positive applications. These features permit 0V to +2V unipolar outputs. An internal buffer amplifier buffers output loading from the D/A module, permitting a constant 50-ohm output impedance.

NOTE: Additional information and pictures on deglitching are included in "Notes on 'Deglitching'" which are part of the data sheet on the Computer Labs TVDA Series D A's.



ULTRA FAST DEGLITCHED D/A CONFIGURATION



DEGLITCHED D/A FOR
TELEVISION SIGNAL REPRODUCTION

ORDERING INFORMATION

DGM-1040 or DGM-1080 are normally supplied with TTL "deglitch" input. For balanced ECL input, specify ECL Input on P.O. or add suffix "ECL" to part number.

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