Marvell Avastar 88W8790 SoC

Bluetooth/FM Single-Chip SoC

PRODUCT OVERVIEW

The Marvell® Avastar™ 88W8790 is a highly integrated system-on-a-chip (SoC) that integrates Bluetooth and FM radio functions. It is specifically designed to support high throughput data rates for next-generation products and is part of the Marvell Avastar family of wireless devices. The Avastar family includes single-function and multi-function radios that establish new industry benchmarks for power consumption, wireless performance, solution footprint and advanced features.

The Marvell Avastar 88W8790 is designed to support Bluetooth 3.0 (also supports Bluetooth 2.1 + EDR features) and both FM transmit and receive (digital encoder/decoder FM radio with RDS/RBDS) operation.

The 88W8790 supports generic interfaces including SDIO, SPI (G-SPI), high-speed UART, and PCM for connecting the Bluetooth core to the host processor.

For FM Tx/Rx, the device supports Inter-IC Sound (I2S) / analog stereo audio interfaces. An I2C-compatible interface is available to connect the FM Tx/Rx to the host processor, as well. The FM Tx/Rx can also share the host interface with Bluetooth.

The device supports a coexistence interface for external, co-located 2.4 GHz radios.

The 88W8790 is available in two TFBGA package options.

BLOCK DIAGRAM

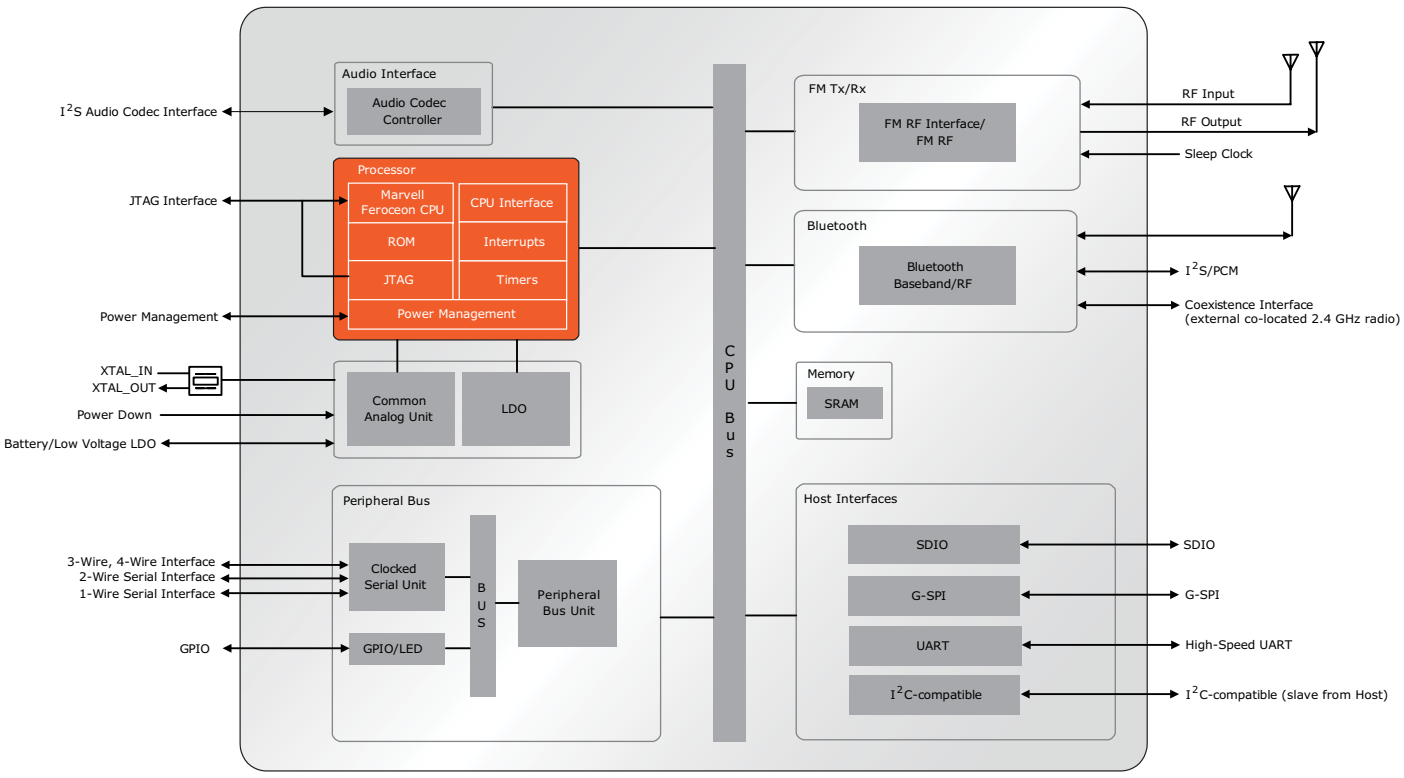

Fig 1. Avastar 88W8790 SoC Block Diagram [1]

1. Antenna can be used as an option to enhance performance

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SPECIFICATIONS

APPLICATIONS
- Bluetooth/FM enabled cellular handsets
- Portable audio/video devices and accessories
- Personal navigation devices
- Personal digital assistants
- Gaming platforms

GENERAL FEATURES
- Simultaneous and independent Bluetooth, and FM Tx/Rx operation
- Coexistence with cellular and other on-chip radios
- Low power dissipation
- CMOS and low-swing sine wave input clock
- Digital audio interfaces (I2S and PCM)
- 12, 13, 19.2, 24, 26, 38.4, and 52 MHz crystal clock support with auto-frequency detection using external 32.768 KHz CMOS-level sleep clock
- Power management with external sleep clock support for FM Tx/Rx operation
- Sleep and standby modes for low power operation
- Fully compatible with Marvell Power Management device(s)

PACKAGING
- 64-pin TFBGA

PROCESSOR
- CPU
  - Integrated Marvell Feroceon® CPU (ARMv5TE-compliant)
  - 64 MHz maximum CPU clock speed

MEMORY
- Internal SRAM for Tx frame queues/Rx data buffers
- Boot ROM
- ROM patching capability

BLUETOOTH
- Bluetooth 3.0 (also compliant with Bluetooth 2.1 + EDR)
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth
- Digital audio interfaces including PCM interface for voice applications and I2S for digital stereo applications
- Baseband and radio BDR and EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), and 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) including Packet Loss Rate (PLR)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard UART, G-SPI, and SDIO HCI transport layer

BLUETOOTH (continued)
- HCI layer verified to function with major profile stack vendors
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (i.e., hold, sniff modes)
- Enhanced low power scan mode
- Dynamic Transmit Power Control (TPC)
- Channel Quality Driven (CQD) data rate
- SBC off load for A2DP streaming
- Wideband Speech Support

FM RADIO
- Worldwide FM band—76–108 MHz
- Full Tx/Rx operation with main clock as well as 32.768 kHz external sleep clock
- Channel spacing/frequency step size (50 kHz steps)
- Stereo analog and digital (I2S) output for Rx
- Stereo digital (I2S) input for Tx

FM Rx PATH
- FM/RDS/RBDS receiver
- Automatic frequency control (AFC)
- Auto search tuning
- Softmute
- Audio mute
- Mono/stereo blending (signal dependent)
- Digital FM demodulation
- RDS data buffer
- FM audio routed internally as SCO source
- Programmable pre/de-emphasis (50/75 µs)
- TMC (traffic alert) supported
- Enable/disable stereo mode
- FM audio option to turn off CPU if no RDS
- Audio silence detection
- Alternate frequency

FM Tx PATH
- FM/RDS/RBDS transmitter
- RDS data buffer
- High Tx output power (+125 dBµVrms) for loop antenna
- Auto scan for channel selection
- Auto channel sync through RDS
- Audio mute
- Audio Automatic Gain Control (AGC)
- Compensation for 32 kHz clock error

COEXISTENCE
- Coexistence interface for external, co-located 2.4 GHz radio
  - Marvell 3/4-wire interface
  - WL_ACTIVE 3/4-wire interface
  - WL_ACTIVE 2-wire interface

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HOST INTERFACES

- SDIO device interface (1-bit SDIO transfer mode at full clock range up to 25 MHz)
- G-SPI device interface
- High speed UART interface
- Optional I2C-compatible slave interface for FM control

PERIPHERAL BUS INTERFACES

- Clocked Serial Unit (CSU)
  - 3-Wire, 4-Wire Serial Interface
  - 2-Wire Serial Interface
  - 1-Wire Serial Interface
- General Purpose Input Output (GPIO)

AUDIO INTERFACES

- Audio Codec Interface
  - Marvell Class D Audio Amplifier
  - TWSI interface for Audio Codec programming
  - I2S (Inter-IC Sound) interface for audio data connection to Digital-to-Analog Converters (DAC)
  - Master and slave mode for I2S, MSB, and LSB audio interfaces
  - Tri-state I2S interface capability
- PCM Interface
  - Master or slave mode
  - PCM bit width size of 8 bits or 16 bits
  - Up to 4 slots with configurable bit width and start positions
  - Short frame and long frame synchronization
  - Tri-state PCM interface capability

TEST

- On-chip diagnostic information

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