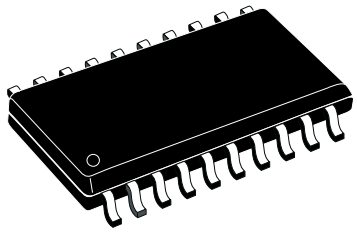
STFC01

Integrated current limiter

Datasheet - preliminary data



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Features

- Wide range of supply voltage: from 10 to 52 V DC (can be extended above 120 V with external components)
- Very low DC current: typ.1.5 mA
- External current limitation setting
- 3 modes of operation
  - Retriggerable
  - Foldback
  - Latched
- Configurable trip-off and recovery times
- Smart current limitation for repetitive overload
- Embedded current sense
- Configurable undervoltage protection
- Floating ground

Description

The STFC01 is an integrated current limiter designed to work with an external P-channel power MOSFET.

It can be used as a universal solution to protect a power supply (from 10 V) from anomalous external current demands (for example, if the load is in latch-up condition).

It can protect or replace conventional fuses and can also be used to control loads.

The STFC01 features 3 user-configurable operating modes (retriggerable, latch, foldback), with different behaviors in case of overload/short-circuit events.

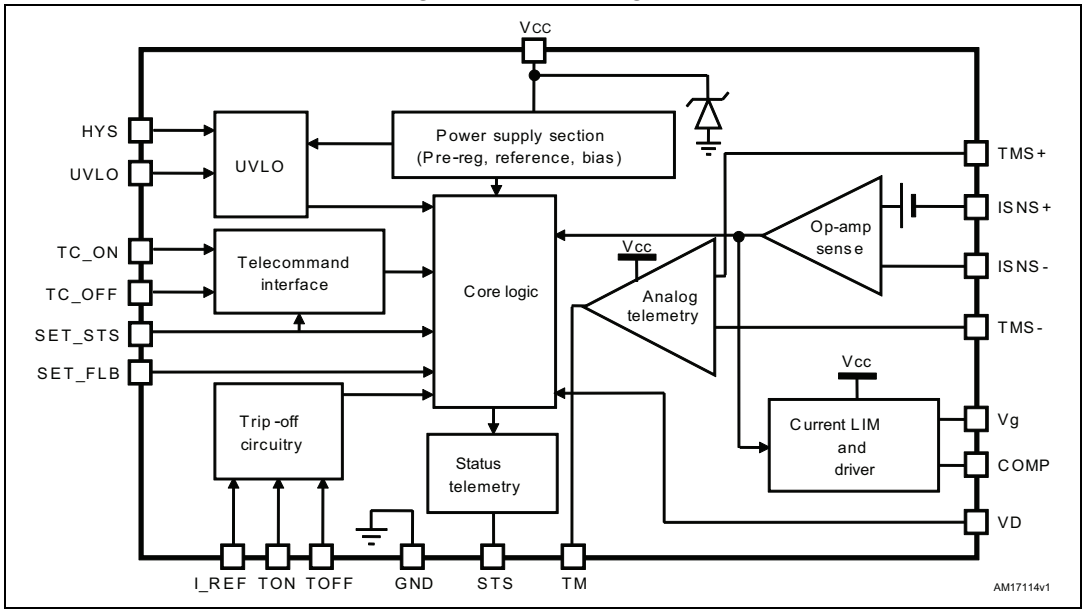
All key parameters of the application, including the current limit, the trip-off, recovery times and the undervoltage protection, are user-configurable, making the STFC01 suitable for a wide range of applications. Because of its floating ground, it can even be used on power buses with voltage above its maximum specification 52 V supply voltage.

The status and control pins allow the remote control of the device and the load.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

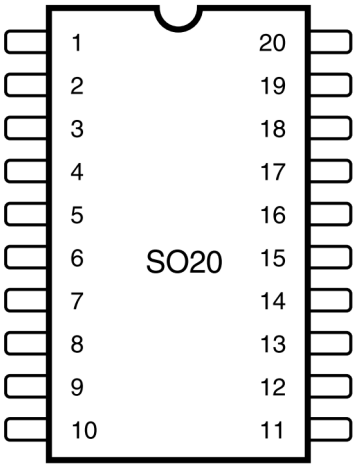


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Table 1. Pin description

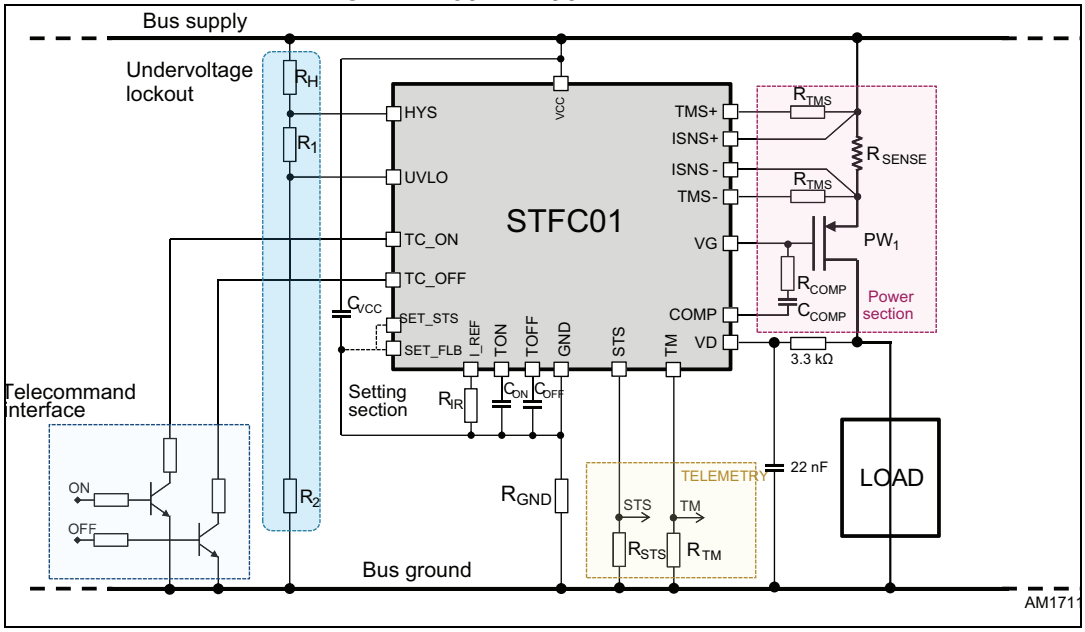
Pin	Name	Type	Description
1	SET_STS	Digital input	Configuration pin. If shorted to GND, the current limiter at power-up is OFF. If connected to V_{CC}, the current limiter at power-up is normally ON.
2	TC_OFF	Digital input	Telecommand interface input for OFF pulsed signal.
3	SET_FLB	Digital input	Configuration pin. If connected to V_{CC}, the foldback mode is enabled.
4	TON	Analog output	Used to set the trip-off time T_{ON}. A C_{ON} capacitor is connected between this pin and GND.
5	TOFF	Analog output	Used to set T_{OFF} recovery time. This pin has a double functionality. If C_{OFF} capacitor is connected between this pin and GND, it sets the T_{OFF} value in retriggerable mode. If the pin is shorted to GND, the device is configured in latched mode.
6	I_REF	Analog input/output	Used to set the current reference. An external high precision resistor is connected between this pin and GND in order to set the current reference.
7	GND	Power supply	Ground. Return of the bias current and zero voltage reference for all internal voltages. Connected to the main bus ground through a decoupling resistor to operate in floating ground configuration.

Table 1. Pin description (continued)

Pin	Name	Type	Description
8	VD	Analog input	Sense pin of the external MOSFET drain voltage used to detect current limitation. A small series resistor can be useful to reduce power dissipation.
9	STS	Digital output	Telemetry digital status. A resistor has to be connected between the pin and the main bus ground.
10	TMS+	Analog input	Non-inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS+ and this pin to guarantee the requested accuracy on the output source current for the analog telemetry.
11	TMS-	Analog input	Inverting input of the telemetry circuit. An accurate external resistor is connected between ISNS and this pin to guarantee the requested accuracy on the output source current for the analog telemetry.
12	TM	Analog output	Output source current for the analog telemetry. A resistor has to be connected between this pin and the main bus ground.
13	COMP	Analog output	Output pin for current limitation loop compensation.
14	V_g	Analog output	MOSFET gate driver output.
15	ISNS-	Analog input	Inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (negative) end of the external current sense resistor.
16	ISNS+	Analog input	Non-inverting input of the op-amp current limitation loop. The pin is tied directly to the hot (positive) end of the external current sense resistor.
17	V_{CC}	Power supply	Supply input voltage.
18	HYS	Analog output	External setting of the UVLO hysteresis. A resistor has to be connected between the main bus and this pin.
19	TC_ON	Digital input	Telecommand interface input for ON pulsed signal.
20	UVLO	Analog input	External setting of the UVLO turn-on threshold. The pin has to be tied to the midpoint of a resistor divider sensing the supply voltage vs. main bus ground.

3 Typical application diagram

Figure 3. Typical application circuit



Note: R_{GND}, R_{STS} and R_{TM} resistors are very important for the application safety. Please refer to Section 7: Application guidelines for their implementation.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Maximum junction temperature	150	°C
V_{HBM}	ESD capability, human body model	2 k	V
SET_STS	Digital input	-0.3 to (V_{CC} + 0.3)	V
TC_OFF	Digital input	-32.6 to (V_{CC} + 0.3)	V
SET_FLB	Digital input	-0.3 to (V_{CC} + 0.3)	V
TON	Analog output	-0.3 to + 4.6	V
TOFF	Analog output	-0.3 to + 4.6	V
I_REF	Analog input/output	-0.3 to + 4.6	V
GND	Device ground	-	
VD	Analog input	-32.6 to (V_{CC} + 0.3)	V
STS	Digital output	-32.6 to (V_{CC} + 0.3)	V
TMS+	Analog input	-0.3 to (V_{CC} + 0.3)	V
TMS-	Analog input	-0.3 to (V_{CC} + 0.3)	V
TM	Analog output	-32.6 to (V_{CC} + 0.3)	V
COMP	Analog output	-0.3 to (V_{CC} + 0.3)	V
V_g	Analog output	-0.3 to (V_{CC} + 0.3)	V
ISNS-	Analog input	-0.3 to (V_{CC} + 0.3)	V
ISNS+	Analog input	-0.3 to (V_{CC} + 0.3)	V
V_{CC}	Power supply	-0.3 to + 54.0	V
HYS	Analog output	-0.3 to (V_{CC} + 0.3)	V
TC_ON	Digital input	-32.6 to (V_{CC} + 0.3)	V
UVLO	Analog input	-0.3 to (V_{CC} + 0.3)	V

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	40	°C/W
R_{tj-a}	Thermal resistance junction-case	40	°C/W

5 Electrical characteristics

T_J = - 40 °C to 125 °C, V_{CC} = 37 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	System operating supply voltage		10		52	V
Supply current and UVLO						
V_Z	V_{CC} vs. GND internal clamp voltage		18.0	19.6	21.2	V
I_{CC}ON	Supply current, on-state	V_{CC} - GND < V_Z		1.5	3	mA
I_{CC}OFF	Supply current, off-state	V_{CC} - GND < V_Z		1.5	3	mA
V_{TH}	Undervoltage lockout turn-on threshold (2)	R1 = 20 kΩ, R2 = 220 kΩ, Rh = 1.6 kΩ	28	30	32	V
	Undervoltage lockout hysteresis (2)		1.8	2	2.2	V
Current limitation						
I_{LIM}	Current limitation sense voltage threshold (between ISNS+ and ISNS-)		90	100	110	mV
Driver						
V_gON	Gate voltage range, on-state			V_{CC}-12		V
V_gOFF	Gate voltage range, off-state				V_{CC}	
I_g	Gate source current	SET_STS low V_g = V_{CC} - 1 V	20			mA
	Gate sink current	SET_STS high V_g = V_{CC} - 9 V			-20	mA
Trip-off function						
T_{ON}	Trip-off time	R_{I_REF} = 120 kΩ C_{ON} = 10 nF		1.2		ms
T_{OFF}	Recovery time	R_{I_REF} = 120 kΩ C_{ON} = 10 nF C_{OFF} = 47 nF		112		
Switching times						
T_{DELAY}	Delay time (from TC_ON to V_{OUT} = 0 to 10%)	Latched-OFF configuration (see *Table 8*)		29		ms
T_{RISE}	Rise time (V_{OUT} from 10% to 90%)			40		
T_{FALL}	Fall time (V_{OUT} from 90% to 10%)			30		
$T_{STORAGE}$	Storage time (from TC_OFF to V_{OUT} = 10%)			47		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Telecommand						
V_{TC_ON/TC_OFF}	Telecommand input voltage turn-on/off		2	2.8	3.6	V
T_{pulse}	Telecommand minimum pulse time		30	100		µs
T_{pulse_noise}	Telecommand immunity pulse time				10	µs
Telemetry						
V_{TM}	Telemetry output voltage range	R_{SENSE} = 100 mΩ R_{TMS} = 5 kΩ R_{TM} = 240 kΩ I_{SENSE}= 500 mA		2.4		V
$V_{TM(OFF)}$	Telemetry output voltage range, off-state	R_{SENSE} = 100 mΩ R_{TMS} = 5 kΩ R_{TM} = 240 kΩ I_{SENSE}= 0 mA		MGND		V
Status						
V_{STATUS}	STS output voltage range	R_{STS} = 50 kΩ		5		V
$V_{STATUS(OFF)}$	STS output voltage range, off-state			MGND		

Note: The operating range of current limitation and load depends on the current capability of the power MOSFET. This range can be extended to higher values according to the current capability of the power MOSFET.

Undervoltage lockout threshold calculation (see Figure 3):

$V_{ON} = V_{TH} = 2.5\ V * ((R_1+R_2) / R_1)$; $V_{OFF} = 2.5\ V * ((R_1 + R_2 + R_H) / (R_1 + R_H))$;

$V_{HY} = V_{TH} - V_{OFF}$

MGND is the main bus ground voltage.

6 Device description and operation

The STFC01 (integrated current limiter) is a versatile monolithic device used as a high-side gate driver or intelligent power switch driver, to give current limitation and protect the main bus in case of excessive current demands.

The device can operate with a supply voltage range from 10 V to 52 V. An undervoltage lockout circuitry guarantees the appropriate power supply integrity. Because of the wide spectrum of load voltage that can be requested, this device can be configured to protect a broad variety of loads.

In case of overload, the device behavior changes according to its configured mode of operation:

- If the current limiter is configured in retriggerable mode, after the trip-off time, the device switches off and remains in this state for a recovery time that is externally programmable. Once this time elapses, the device switches cyclically on and off again while the overload persists.
- If configured in foldback mode, in case of overload, the device provides current limitation, with a value decreasing with the output voltage, reaching a fixed and safe value even if a short-circuit persists.
- If configured in latched mode, the device has the current limitation feature for an externally configurable time, called trip-off time, and if the overcurrent condition exceeds this time, the device switches off. In this case, the device may be switched on again, through the telecommand pin only.

The core of the device consists of the driver block, designed to drive an external P-channel power MOSFET connected as high-side configuration. Current sensing, current limitation detection, remote control, telemetry and protection functions are also included allowing the design of high reliability systems.

Thanks to the remote monitor and telecommand interface features, the STFC01 performs the full control and the partitioning of each load connected to the device.

6.1 Supply voltage, startup and undervoltage lockout

The device can be directly supplied with a voltage range from 10 V to 52 V. A Zener diode chain is embedded to clamp the voltage level between V_{CC} and GND at 20 V (typ. 19.6 V).

The device can be configured to power up either in OFF or ON-state, depending on the configuration of SET_STS pin.

Table 5. Power-up settings

SET_STS	Mode
GND	OFF @ power-up
V_{CC}	ON @ power-up

If the device is configured ON at power-up (SET_STS pin is connected to V_{CC}), when the supply bus reaches the turn-on threshold, the device is ready to drive the MOSFET. There is no point in receiving the ON command by the telecommand interface to enable the device.

If the device is configured OFF at power-up (SET_STS pin is connected to GND), when the supply bus reaches the turn-on threshold, the device waits for the ON command on the telecommand interface to switch on.

The UVLO circuit protects the device from an incorrect bias condition. The setting of the disconnection and reconnection thresholds (turn-off and turn-on) is performed by R_H-R_1-R_2 external resistor divider connected between V_{CC} and the main bus ground (MGND).

The connection point between R_1 and R_2 is tied to the ULVO pin (*Figure 3*).

Hysteresis is implemented to avoid undesired oscillations caused by bus voltage transients. The hysteresis value can be set through the connection of the resistor R_H between V_{CC} and HYS pin (*Figure 3*).

R_1, R_2 and R_H can be chosen using the following equations:

Equation 1

$$V_{ON} = 2.5 \cdot \frac{R_1 + R_2}{R_1}$$

Equation 2

$$V_{OFF} = 2.5 \cdot \frac{R_1 + R_2 + R_H}{R_1 + R_H}$$

Equation 3

$$V_{HYS} = V_{ON} - V_{OFF}$$

where:

- V_{ON} is the undervoltage lockout turn-on threshold
- V_{OFF} is the undervoltage lockout turn-off threshold
- V_{HYS} is the undervoltage lockout hysteresis

In *Equation 1*, V_{ON} is obtained assuming that R_H is greater than the drain-to-source ON resistor of the internal switch connected between HYS and V_{CC} pads (switch embedded in the device used to short the R_H resistor and whose ON-resistance acts in parallel to R_H). The value of this resistor is about 160 Ω.

An internal masking time ignores bus undervoltage events lower than 50 µs. This allows the device to be protected from the turn-off in case of glitches or transient noise occurring on the main supply bus. If a masking time value, higher than 50 µs, is needed, an external capacitor can be connected between the main supply bus and UVLO pin.

Once UVLO event is triggered and recovered, the device restarts according to the configuration defined by SET_STS pin.

6.2 Modes of operation

When an overcurrent event occurs, the device detects this condition and the trip-off timer starts. The device drives the external MOSFET to limit the current across the load (current limitation mode) and if the overcurrent condition lasts more than T_{ON} trip-off time, at the end of T_{ON} period, the external MOSFET turns off. Instead, if the overcurrent event lasts for an interval shorter than T_{ON}, the device limits the current for the duration of the fault and recovers as soon as the overcurrent condition disappears (MOSFET is driven to its low-ohmic status with the channel well-saturated).

T_{ON} trip-off time can be set through C_{ON} external capacitor connected between T_{ON} and GND pin, as shown in the application diagram (*Figure 3*). C_{ON} capacitor is charged with I_{REF} constant current whose value is externally set by R_{IR} resistor connected between I_REF and GND pins, so that T_{ON} trip-off time value is defined by the following equation.

Equation 4

$$T_{ON} = C_{ON} * R_{IR}$$

C_{ON} capacitor charging phase starts as soon as the overcurrent event is detected by I_{REF} constant current value, externally set by R_{IR} resistor connected between I_REF and GND pin.

At the end of a current limitation period (either T_{ON} time has elapsed and the MOSFET is switched off or the overcurrent event has disappeared), the discharging phase of the C_{ON} capacitor starts with a current which is 20 times smaller than the charging phase. With this high charge/discharge ratio, if the overcurrent event occurs frequently and each time for a shorter period than T_{ON} trip-off time, the MOSFET turns off (after a number of overcurrent events). In this manner, the device implements a sort of memory of overcurrent events whose single duration is shorter than T_{ON}, thus avoiding dangerous thermal stress to the MOSFET (hiccup mode).

The procedure can be latched or retriggerable and depends on how TOFF pin is connected.

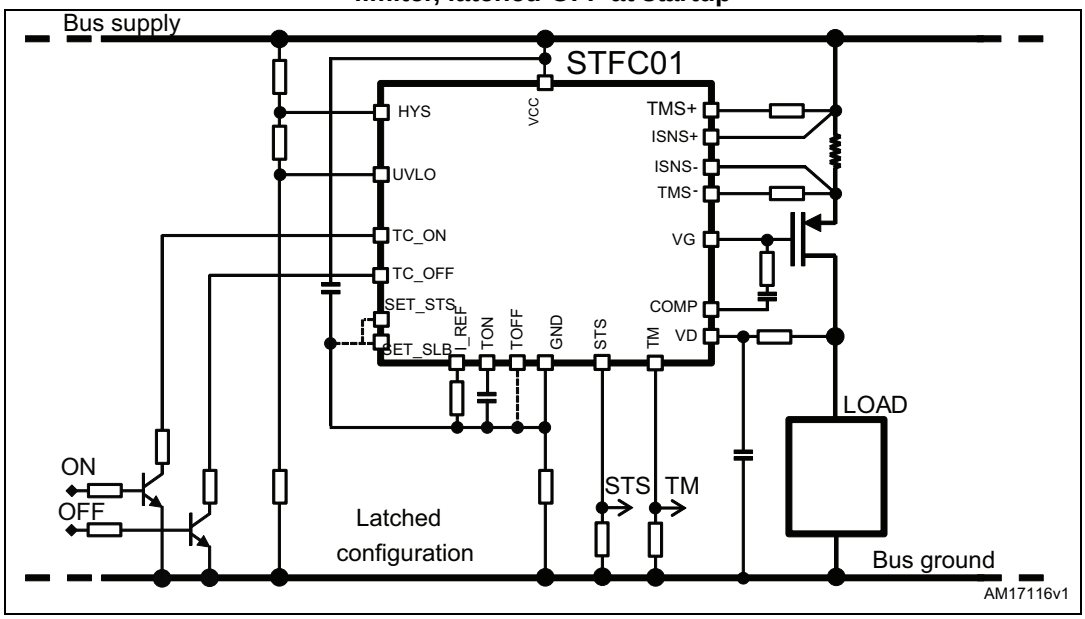
Table 6. TOFF pin settings

TOFF	Mode
GND	Latched
C_{OFF}	Retriggerable

6.2.1 Latched mode

The device is configured as a latched current limiter (see *Figure 4*) when TOFF pin is shorted directly to GND. In this mode, if the duration of the overcurrent event is longer than trip-off time, the external MOSFET latches off and remains off until the reset is given by either the telecommand interface or UVLO activation/deactivation cycle. When the device is configured as a latched current limiter, the use of the telecommand interface is required. Moreover, if this configuration mode is set, the start-up mode of the device can be selected between latched-OFF (the device is OFF at power-up) and latched-ON (the device is ON at power-up) using SET_STS pin. *Figure 4* refers to latched-OFF start-up mode selection.

Figure 4. Typical application diagram with the STFC01 configured as latched current limiter, latched-OFF at startup



Note: *R_{GND}, R_{STS} and R_{TM} resistors are very important for the safety of the application. Please refer to Section 7: Application guidelines for their implementation.*

6.2.2 Retriggerable mode

The device is configured as a retriggerable current limiter (see *Figure 5*) when C_{OFF} external capacitor is connected between TOFF pin and GND. In retriggerable mode, if the duration of the overcurrent is longer than T_{ON} trip-off time, the external MOSFET is switched off (as when the latched mode is selected) but the MOSFET stays off during the recovery time T_{OFF}. When T_{OFF} time elapses, the device restarts autonomously to its normal condition, turning on again the MOSFET.

T_{ON} trip-off time, as well as T_{OFF} recovery time, can be externally set through C_{OFF} external capacitor connected between TOFF and GND pin, as shown in the application diagram with the STFC01 configured as a retriggerable current limiter (*Figure 5*). C_{OFF} capacitor is charged with a constant current whose value is a fraction (1/20) of I_{REF} (externally set by R_{IR} resistor connected between I_REF and GND pin). C_{OFF} capacitor charging phase starts as soon as T_{ON} time has elapsed, therefore T_{OFF} time is equal to C_{OFF} charging time defined by:

Equation 5

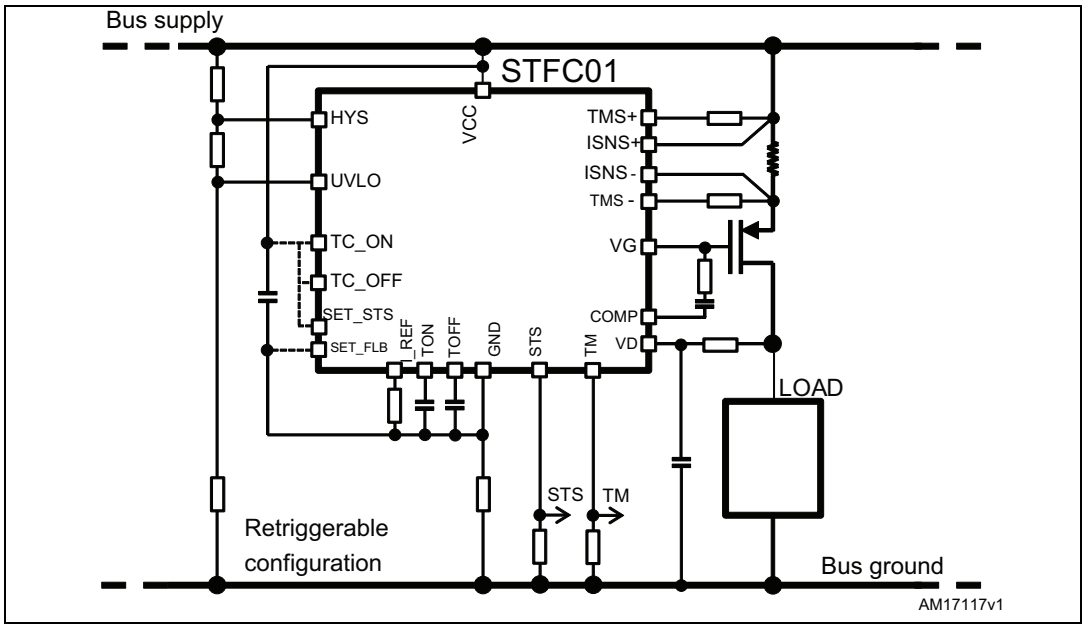
$$T_{OFF} = 20 * R_{IR} * C_{OFF}$$

For safety reasons, C_{OFF} capacitor is quickly discharged. T_{OFF} is generated not only after a current limitation event whose duration is longer than T_{ON} time, but also after any event that turns off the device.

When the device is configured as a retriggerable current limiter, the following settings are recommended:

– to select the option ON at power-up, connecting SET_STS pin to V_{CC}
– to disable the telecommand interface, connecting TC_ON and TC_OFF pins to V_{CC}

Figure 5. Typical application diagram with the STFC01 configured as retriggerable current limiter



Note: R_{GND}, R_{STS} and R_{TM} resistors are very important for the safety of the application. Please refer to Section 7: Application guidelines for their implementation.

6.2.3 Foldback mode

The device can be configured as a foldback current limiter through SET_FLB configuration pin (see *Figure 6*).

Table 7. Foldback mode setting

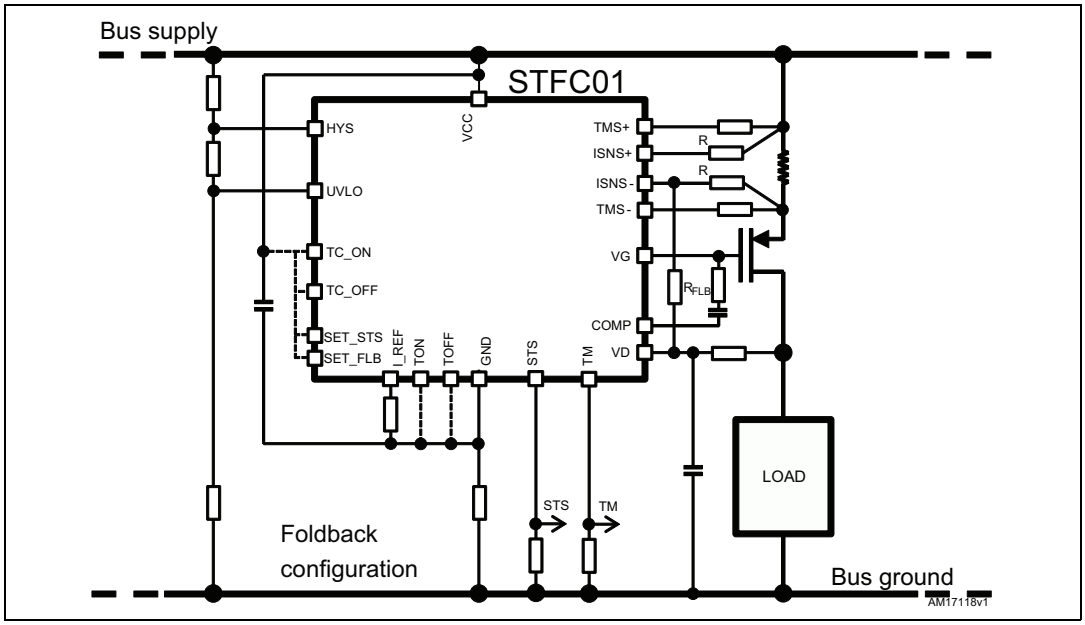
SET_FLB	Mode
GND	Foldback mode disabled
V_{CC}	Foldback mode enabled

A foldback current limiter is a special device that never turns off, otherwise the application could be compromised. When an overcurrent event is detected, the device implements the current limitation feature whose value depends on the output voltage, reaching a small and safe value even if a short-circuit on the load occurs and remains. If the foldback mode is selected:

– select the option ON at power-up, connecting SET_STS pin to V_{CC}
– disable trip-off function, connecting TON and TOFF pin to GND
– disable the telecommand interface, connecting TC_ON and TC_OFF pin to V_{CC}

When configured as a foldback current limiter, additional resistors have to be connected between VD and ISNS- pin and each end of R_{SENSE} resistor, ISNS- and ISNS+ (see *Figure 6*).

Figure 6. Typical application diagram with the STFC01 configured as a foldback current limiter



Note: R_{GND}, R_{STS} and R_{TM} resistors are very important for the safety of the application. Please refer to Section 7: Application guidelines for their implementation.

The device can be configured in different modes using suitable combinations of the configuration pins quoted in the table below.

Table 8. Device configuration truth table

Configuration	SET_FLB	SET_STS	TC_ON	TC_OFF	TON	TOFF	Status at power-up
Latched-OFF	0	0	Telecommand	Telecommand	C_{ON}	GND	OFF @ power-up
Latched-ON	0	1	Telecommand	Telecommand	C_{ON}	GND	ON @ power-up
Retriggerable	0	1	V_{CC}	V_{CC}	C_{ON}	C_{OFF}	ON @ power-up
Foldback	1	1	V_{CC}	V_{CC}	GND	GND	ON @ power-up

6.3 Current sense/limitation

The voltage drop on the external R_{SENSE} resistor (see *Figure 3*) is continuously monitored (by ISNS+ and ISNS- pins) and compared with a fixed 100 mV internally generated threshold. If the voltage drop on R_{SENSE} surpasses 100 mV, the current demand becomes excessive and the timer counts the trip-off time T_{ON} and the device enters the current limitation mode. In this condition, the limitation control loop is enabled to force V_g to the proper voltage level, limiting the current to the load. RC compensation network could be connected between V_g and COMP pin to improve the loop stability.

The current limitation threshold can be externally set according to the application requirements by R_{SENSE} resistor. When configured as either retriggerable or latched current limiter, it is:

Equation 6

$$I_{LIM} = 100mV/R_{SENSE}$$

where I_{LIM} is the limitation current, R_{SENSE} resistor can be chosen by:

Equation 7

$$R_{SENSE} = 100mV/100I_{LIM}$$

if configured as a foldback current limiter (see *Figure 6*), it is:

Equation 8

$$I_{LIM} = \frac{100mV - \frac{R}{R_{FLB}}(V_{CC} - V_D)}{R_{SENSE}}$$

6.3.1 Repetitive overload events

In case of repetitive overload events each one, having a duration $t < T_{ON}$, a “memory” of the previous current limitation events, keeps the junction temperature of the external MOSFET at safety level. This function, working both in latched and retriggerable modes, is depicted in the following figures.

Figure 7. Behavior under repetitive overloads

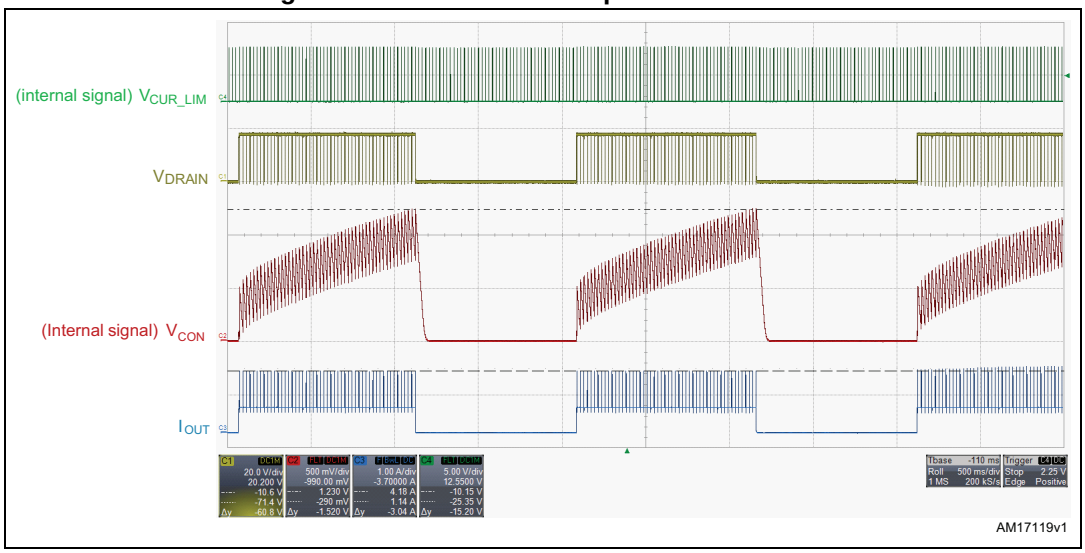
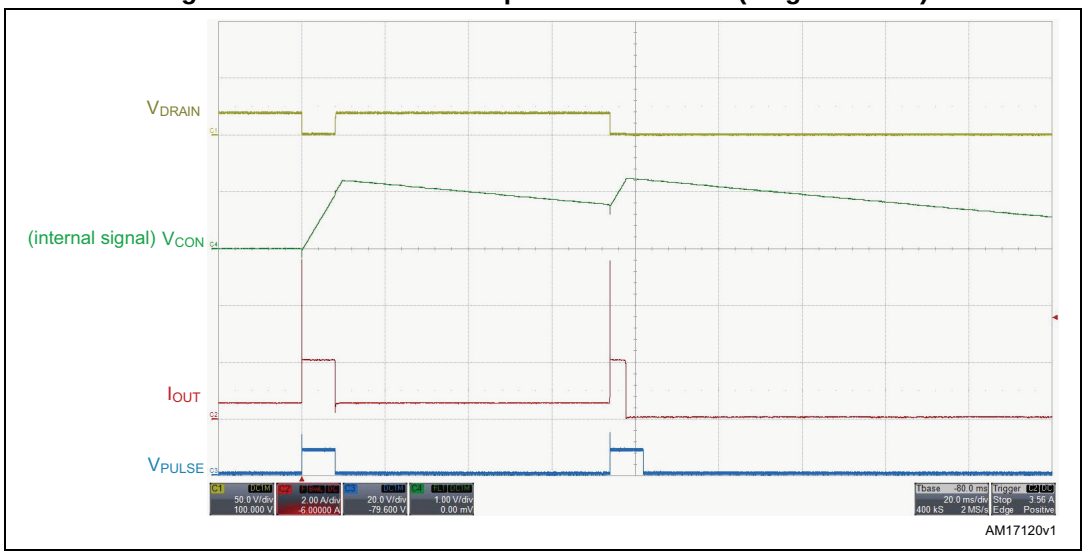


Figure 8. Behavior under repetitive overloads (magnification)



6.4 Gate driving

The driver circuit is designed to drive an external P-channel power MOSFET (connected in high-side configuration) providing on V_g pin a voltage signal in the range from V_{CC} to V_{CC}-12 V.

When the device works in normal operating mode (which means the device is neither OFF nor in current limitation mode) V_g node is pulled down and the gate of the external MOSFET is internally clamped about 12 V below the supply voltage V_{CC} making the channel of the MOSFET well-saturated.

- When the MOSFET has to be switched OFF, V_g goes up to V_{CC}
- When the MOSFET is in current limitation mode, V_g voltage is defined by the limitation control loop

6.5 Telecommand interface

The STFC01 can be enabled or disabled by two digital signals through TC_ON and TC_OFF pins. If the voltage on TC_ON pin is forced low for a typical pulse time of 100 µs, the device switches on. In the same way, a low voltage for a typical pulse time of 100 µs forced on TC_OFF pin switches off the device. To have a more robust implementation, unwanted ON/OFF pulses, having a short duration (shorter than 10 µs), are ignored to have a sort of noise immunity of the telecommand system.

In case of contemporaneous application of ON and OFF commands, OFF command has the priority, which means that in case of a failure of the telecommand interface resulting in a permanent on-state, the device can be switched off by sending the OFF command.

6.6 Floating ground configuration

As mentioned in *Section 6.1*, a Zener diode chain is embedded to clamp the voltage level between V_{CC} and GND at about V_Z = 20 V (typ. 19.6 V).

If the operating supply bus is $V_{CC} < V_Z$, the Zener clamp is OFF and the total current consumption of the device is about 1.5 mA @ V_{CC} ~ 19.4 V, near the ON threshold for the clamp.

If the operating supply bus is $V_{CC} > V_Z$, the Zener clamp is ON and the current consumption of this Zener diode chain is added to the previous current consumption of the device.

In order to benefit from the floating ground feature and therefore to improve the device performance in terms of power line rejection, the device should operate with the Zener clamp active.

A good trade-off is to establish a total current consumption of 2 mA, therefore the floating ground resistor is sized according to the following resistor.

Equation 9

$$R_{GND} = \frac{V_{cc} - V_z}{I_{cc}}$$

where:

V_{CC} = system operating supply voltage

V_Z = V_{CC} vs. GND internal clamp voltage

I_{CC} = supply current whose recommend value is 2 mA

The implementation of the floating ground feature is useful to avoid the collapse of the bus supply vs. the bus ground, compromising the application as a result of a possible short of the supply line vs. ground inside the device.

In case of a short-circuit inside the device, the external R_{GND} resistor (*Figure 3*) connected between GND pin and the main bus ground has to sustain the overall voltage between the bus supply and ground. The power dissipation of this resistor has to be sized properly to dissipate the power according to the steady-state value of the supply bus. Additional single point failure protection recommendations can be found in *Section 7: Application guidelines*.

6.7 Status telemetry

The status telemetry circuit gives information about the device status. This information can be retrieved by monitoring STS output pin.

When ON command is received through TC_ON pin or the device turns on because of the undervoltage event to a normal operation mode, STS output is forced high.

STS output is forced low when one of the following events occurs.

- The device turns off the external MOSFET as a consequence of a current limitation event
- OFF command is received through TC_OFF pin to turn off the device
- OFF command is received through TC_OFF pin to reset a latch condition

Table 9. Telemetry digital status pin

STS	Mode
Low	Device is in off-state
High	Device is in on-state

STS is an open drain pin, which is able to source a 100 µA fixed current, so that an external resistor R_{STS} (*Figure 3*) has to be connected between STS pin and the main bus ground. R_{STS} value has to be chosen according to the desired high voltage level (V_{H_STS}) as per below equation.

Equation 10

$$R_{STS} = V_{H-STS} / (100 \mu \Lambda)$$

6.8 Analog current sense telemetry

The telemetry circuit gives some information about the current across the load. This circuit provides on TM pin a source current whose value is proportional to the current flowing from the bus supply line to the load. The voltage drop on R_{TM} external resistor (*Figure 3*),

connected between TM pin and the main bus ground, is proportional to the current load, performing a current/voltage conversion.

This function is implemented by sensing the voltage drop on the external R_{SENSE} resistor through R_{TMS} resistor connected to TMS+ and TMS- pin.

Equation 11

$$I_{RTM} = I_{RSENSE} \cdot \frac{R_{SENSE}}{R_{TMS}}$$

Equation 12

$$R_{TM} = \frac{V_{TM}}{I_{RTM}} = \frac{V_{TM}}{I_{SENSE}} \cdot \frac{R_{TMS}}{R_{SENSE}}$$

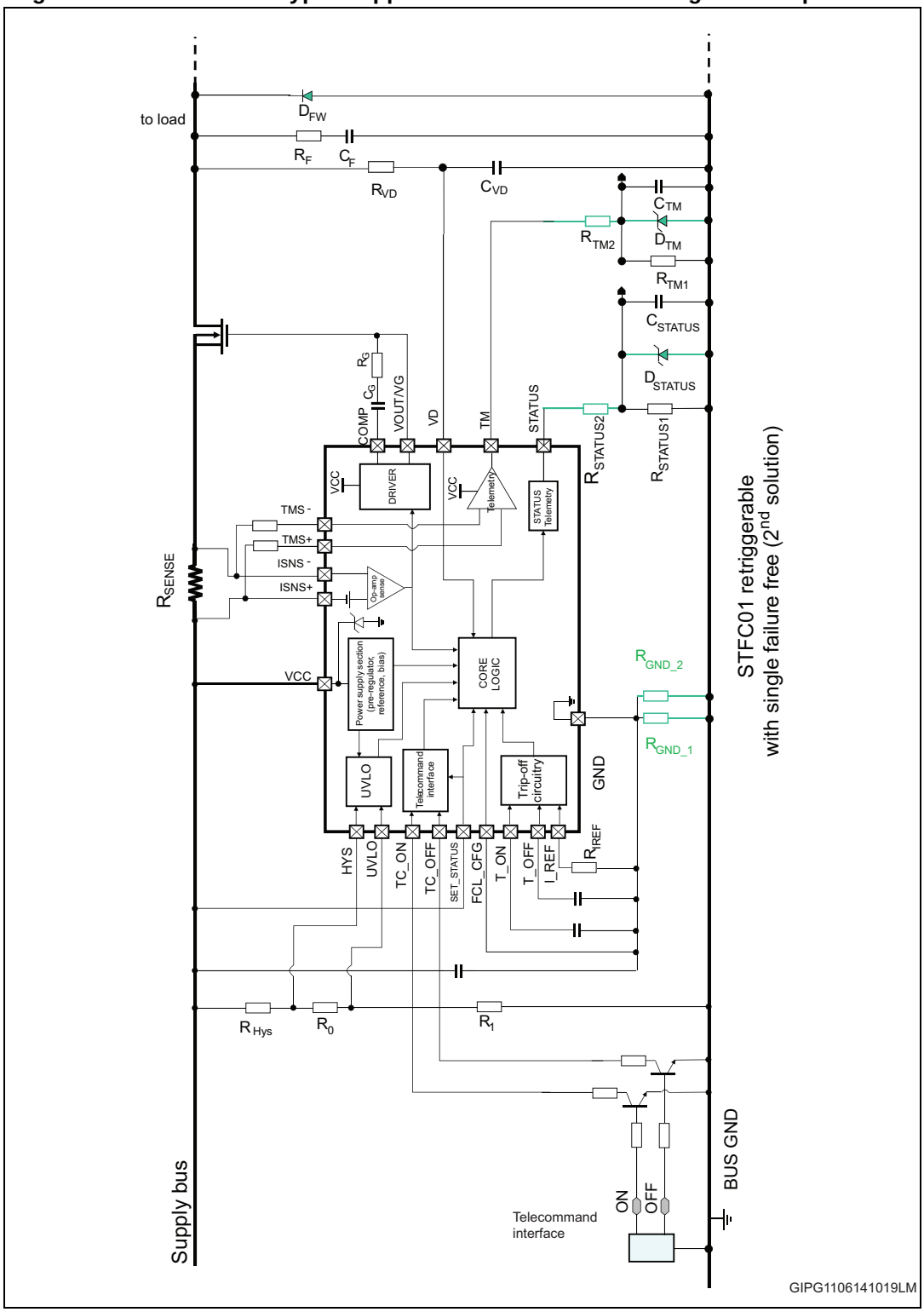
where V_{TM} is the voltage drop on R_{TM} external resistor that has to be monitored to have information on the corresponding I_{RSENSE} current.

7 Application guidelines

In a floating ground configuration, the application can be protected from single point failures of the resistor connected between GND and the GND bus (R_{GND}), and the telemetry resistors (R_{STS} and R_{TM}). In fact, in case of failure of these resistors, damage may occur to the device itself and to the other devices connected to the same bus.

The figure below shows a typical implementation of the protection described above, with additional components named: R_{GND_1}, R_{GND_2}, D_{STATUS}, $R_{STATUS2}$, D_{FW}, D_{TM}.

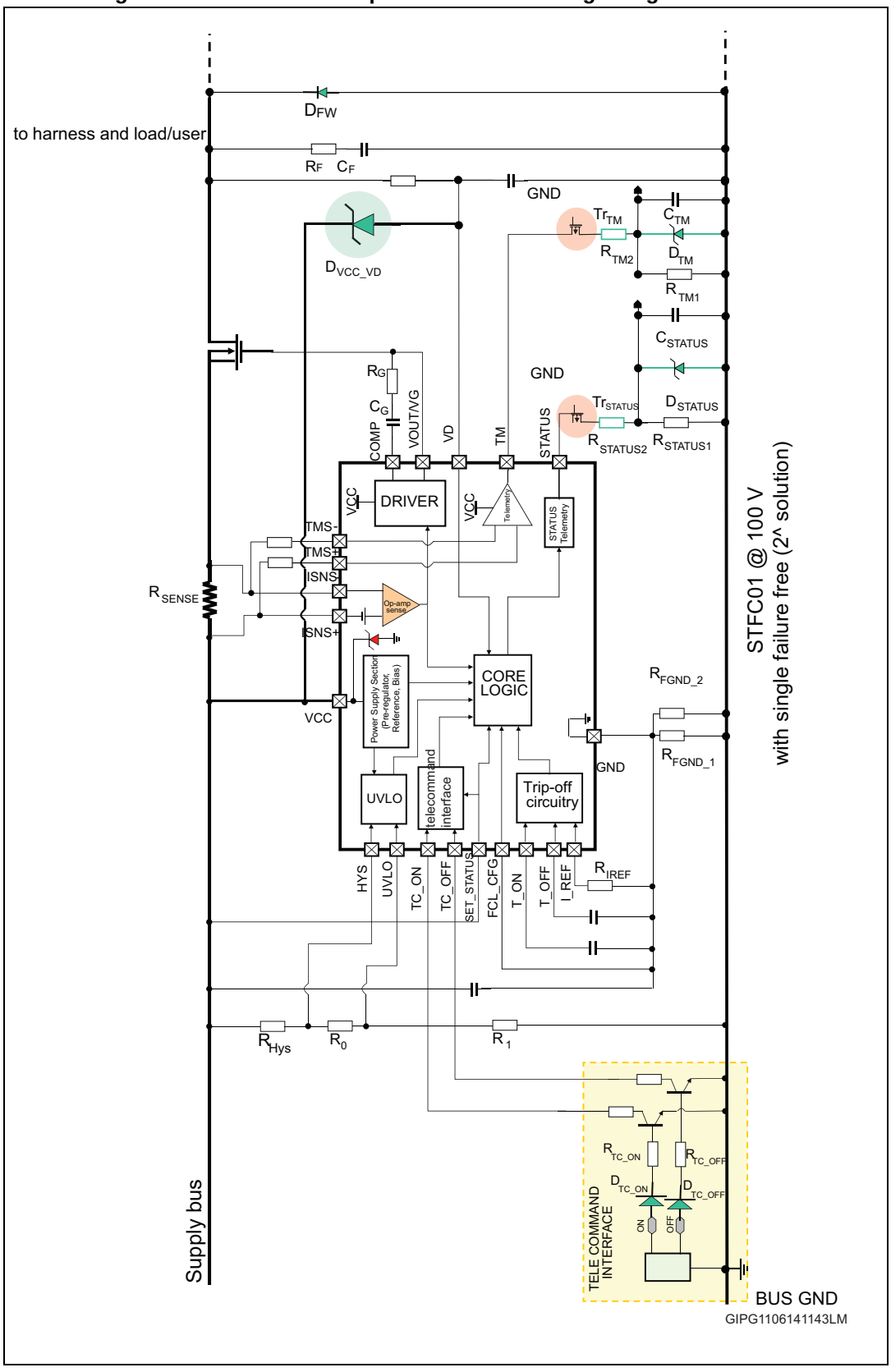
Figure 9. Recommended typical application schematic with single failure protection



7.1 Guidelines for operation at high voltage

The device withstands up to 52 V between BUS_SUPPLY and BUS_GND. Nevertheless it is possible, by adding external components, to work at a bus supply higher than 52 V, as described in the following figure.

Figure 10. Schematic for operation at bus voltages higher than 52 V



R_{TC_ON} and R_{TC_OFF} resistors in series to pull-down transistors of the telecommand circuitry are sized to guarantee that pins never go to - 32 V under GND, the substrate reference of the device. D_{TC_ON} and D_{TC_OFF} diodes are connected in series to pull-down transistors.

Telemetry pins (TM and STATUS) are connected to BUS GND through the external HV P-CH transistors (Tr_{STATUS}, Tr_{TM}) used in cascade configuration, with gate connected to GND. D_{STATUS}, D_{TM} diodes and R_{TM2} and $R_{STATUS2}$ resistors are also connected.

V_D pin is clamped (for example through a Zener diode among V_{CC}, V_D and D_{VCC_VD}) in order to avoid this pin to go to -32 V under GND when the device is in off-state or in case of a short-circuit.

D_{FW} diode is connected between supply bus and ground.

8 Layout guidelines

The STFC01 simultaneously handles fast switching and medium voltage, which implies specific attention to the layout.

The first priority when components are placed is the power section (current path from input, through current sense resistor and high-side switch, toward output), minimizing the length of each connection and loop at the maximum.

Besides, the path of the gate driver signal (driving ON/OFF the high-side switch) has to present the lowest resistance. A power resistor might be required in series to this path to protect the integrated gate driver.

To minimize noise and voltage spikes (EMI and losses), power connections have to be a part of a power plane and implemented using wide and thick conductor traces. The loop has to be minimized. The inductance effect, leading to ringing of tracks can be minimized by making tracks as short as possible. The number of vias must be minimized to reduce the related parasitic effect.

A capacitor on V_{CC}, as well as the capacitors connected to the digital pins, should be placed as closer as possible to IC to reduce the possible loop and parasitic inductance.

Small signal components and connections to critical nodes (TC_ON/OFF, ISNS+ and ISNS) of the application are also important. In fact, the symmetry of the path may impact the sampled value.

Finally, for reliability reasons, more than one resistor should be used (series connected) between the device and the main bus ground whose total value is obtained by application design considerations.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 11. SO-20 drawings

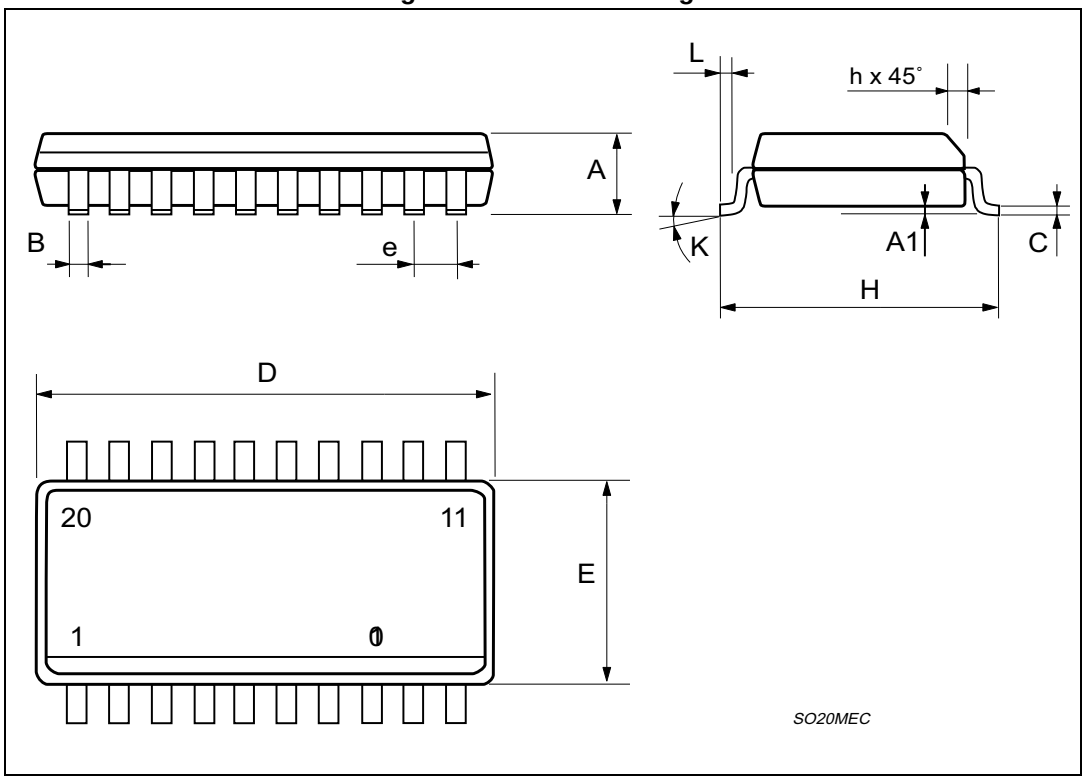


Table 10. SO-20 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.1		0.3
B	0.33		0.51
C	0.23		0.32
D	12.6		13
E	7.4		7.6
e		1.27	
H	10		10.65
h	0.25		0.75
I	0.4		1.27

10 Ordering information

Table 11. Ordering information

Order code	Package	Marking
STFC01DR	SO-20	STFC01D

11 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Aug-2014	1	Initial release.