## **Power MOSFET**

## 60 V, 65 m $\Omega$ , 12 A, Dual N-Ch Logic Level

#### **Features**

- Small Footprint (5x6 mm) for Compact Designs
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- 175°C Operating Temperature
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	60	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>ΨJ-mb</sub>		T <sub>mb</sub> = 25°C	I <sub>D</sub>	12	Α
(Notes 1, 2, 3, 4)	Steady State	T <sub>mb</sub> = 100°C		8.8	
Power Dissipation R <sub>ΨJ-mb</sub> (Notes 1, 2, 3)		T <sub>mb</sub> = 25°C	$P_{D}$	23.4	W
		T <sub>mb</sub> = 100°C		11.7	
Continuous Drain Cur-		T <sub>A</sub> = 25°C	I <sub>D</sub>	4.5	Α
rent R <sub>0JA</sub> (Notes 1, 3 & 4)	Steady	T <sub>A</sub> = 100°C		3.2	
Power Dissipation R <sub>0</sub> JA (Notes 1 & 3)	State	T <sub>A</sub> = 25°C	$P_{D}$	3.0	W
		T <sub>A</sub> = 100°C		1.5	
Pulsed Drain Current	$T_A = 25^{\circ}C$ , $t_p = 10 \mu s$		I <sub>DM</sub>	62	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Source Current (Body Diode)			I <sub>S</sub>	22	Α
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, $I_{L(pk)}$ = 19.5 A, L = 0.1 mH, $R_G$ = 25 $\Omega$ )			E <sub>AS</sub>	19	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) - Steady State (Notes 2, 3)	R <sub>ΨJ−mb</sub>	6.4	
Junction-to-Ambient - Steady State (Note 3)		50	°C/W
Junction-to-Ambient - Steady State (min footprint)	$R_{ hetaJA}$	161	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

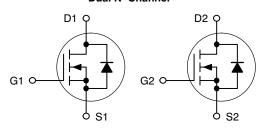


### ON Semiconductor®

### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
60 V	65 mΩ @ 10 V	12 A
	79 mΩ @ 4.5 V	12.4

#### **Dual N-Channel**





CASE 506BT

### **MARKING DIAGRAM**

D1 D1 S1 0 D1 G1 5489NL D1 S2 AYWZZ D2 G2 D2 D2

5489NL = Specific Device Code A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>			
NVMFD5489NLT1G	DFN8 (Pb-Free)	1500/ Tape & Reel			
NVMFD5489NLT3G	DFN8 (Pb-Free)	5000/ Tape & Reel			
NVMFD5489NLWFT1G	DFN8 (Pb-Free)	1500/ Tape & Reel			
NVMFD5489NLWFT3G	DFN8 (Pb-Free)	5000/ Tape & Reel			

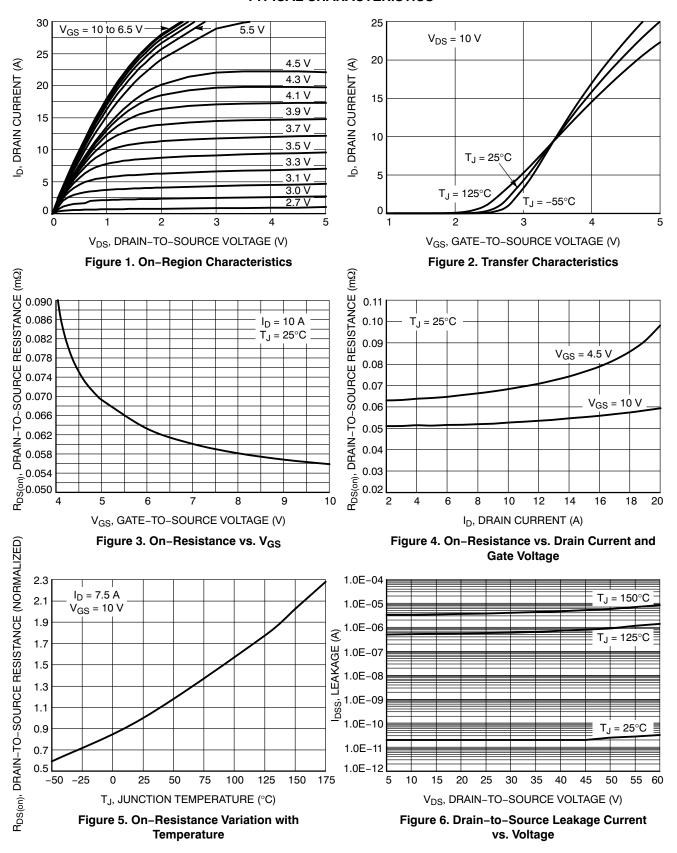
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

### **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condit	tion	Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	Reference to 25°C I <sub>D</sub> = 250 μA			67		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	$T_{J} = 25^{\circ}C$ $T_{J} = 125^{\circ}C$			1.0	μА
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub>				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =	250 μΑ	1.5		2.5	T v
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	Reference to 25°C $I_{D} = 250 \mu\text{A}$			4.86		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A			52	65	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub>	= 7.5 A		66	79	1
CHARGES AND CAPACITANCES	•		•				
Input Capacitance	C <sub>iss</sub>			330		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V			80		
Reverse Transfer Capacitance	C <sub>rss</sub>				39		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 6 A			12.4		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				0.31		
Gate-to-Source Charge	Q <sub>GS</sub>				1.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			4.74		1	
SWITCHING CHARACTERISTICS (N	ote 6)				•		
Turn-On Delay Time	t <sub>d(on)</sub>				7		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub>	= 48 V.		11		1
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 6 A, R_G =$	2.5 Ω		31		1
Fall Time	t <sub>f</sub>				21		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.83	1.2	V
G		I <sub>S</sub> = 10 A	T <sub>J</sub> = 125°C		0.71		1
Reverse Recovery Time	t <sub>RR</sub>		-1		24.2		ns
Charge Time	t <sub>a</sub>	$V_{GS} = 0 \text{ V}, d_{IS}/d_t = 100 \text{ A}/\mu\text{s}, \\ I_S = 10 \text{ A}$			20.2		1
Discharge Time	t <sub>b</sub>				4.0		1
Reverse Recovery Charge	Q <sub>RR</sub>				26.5		nC
PACKAGE PARASITIC VALUES	•		·		•		•
Source Inductance	L <sub>S</sub>	T <sub>A</sub> = 25°C			0.93		nH
Drain Inductance	L <sub>D</sub>				0.005		1
Gate Inductance	L <sub>G</sub>				1.84		1
Gate Resistance	R <sub>G</sub>				12		Ω

<sup>5.</sup> Pulse Test: pulse width = 300  $\mu$ s, duty cycle  $\leq$  2%. 6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



#### **TYPICAL CHARACTERISTICS**

V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

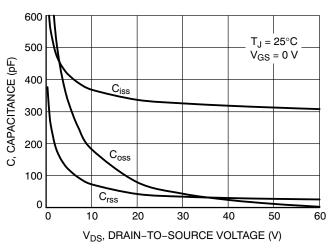


Figure 7. Capacitance Variation

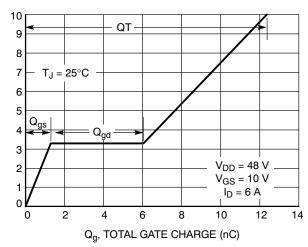


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

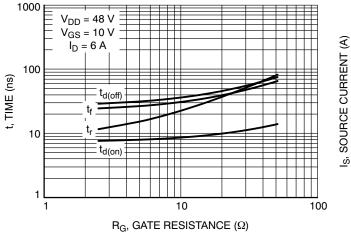


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

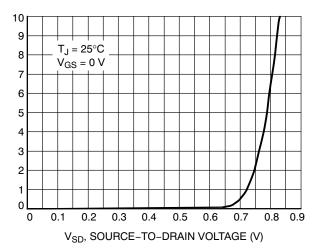


Figure 10. Diode Forward Voltage vs. Current

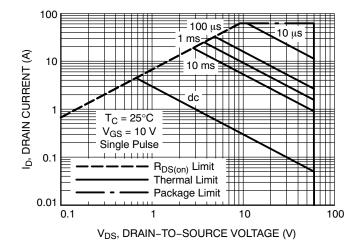


Figure 11. Maximum Rated Forward Biased Safe Operating Area

### **TYPICAL CHARACTERISTICS**

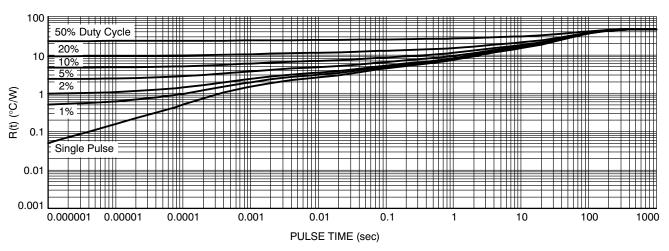
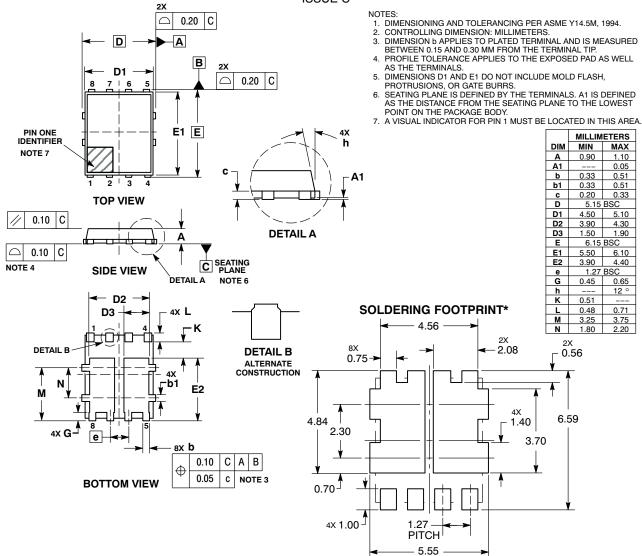


Figure 12. Thermal Response

#### PACKAGE DIMENSIONS

#### DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT ISSUE C



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIMENSION: MILLIMETERS

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