

# MN86072

## Image Processing LSI

### ■ Overview

The MN86072 enhances image quality by applying various imaging processing techniques to the analog signal from an image sensor. It reproduces halftone images with 64-gradation using two-dimensional MTF correction and a user-programmable gamma curve.

### ■ Features

- Image processing that yields top image quality
  - White and black shading correction using overall pixel correction
  - Error dispersion processing that reproduces halftone images with 64-gradation  
User-programmable gamma curve
  - Multivalued smoothing for diagonal lines to eliminate unsightly "jaggies," artifacts resulting from enlargement or line density conversion
  - Enlargement/reduction (line density conversion) with a user-specified scaling factor without introducing moire patterns
- High-speed processing of only 1 ms per line for an A3 page at 400 dpi with an image processing frequency of 6 MHz
- Built-in analog processing circuits: offset correction circuit, gain correction circuit, and analog-to-digital converter
- Drive signal generator for CCDs, CISs, and other
- Memory interfaces that cover a wide variety of applications
  - Standard G3 operation (L mode) (200 dpi, 3 ms/line)
 

B4 readout: 64-Kbit SRAM	× 1
A3 readout: 256-Kbit pseudo-SRAM	× 1
  - High-speed G3 operation (M mode) (200 dpi, 1 ms/line)
 

B4 and A3 readout: 64-Kbit SRAM	× 2
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  - High-resolution G3 operation (M mode) (400 dpi, 2 ms/line)
 

B4 readout: 64-Kbit SRAM	× 2
A3 readout: 256-Kbit SRAM	× 2
+SRAM (16-Kbit)	× 2
or	
256-Kbit SRAM	× 2
  - Ultra-high-speed G4 (H mode) (400 dpi, 1 ms/line)
 

B4 and A3 readout: 64-Kbit SRAM	× 4
+ 5K × 8-bit FIFO	× 1

### ■ Applications

- Facsimile equipment

### ■ Brief Specifications

- Image processing speed:
  - 0.1 to 6 million pixels per second
- Pixels per line:
  - max. 16,384 pixels in the primary scanning direction
- Offset correction:
  - negative feedback preamplifier
    - The chip controls the feedback voltage using A/D conversion data from black pixel sections
    - Built-in circuits: Feedback voltage control circuit + source follower circuit × 2 (Support for channel-separated CCDs included)
- Gain control:
  - Analog control using an external operational amplifier and the built-in field effect transistor (FET)
    - An external resistor determines the control range. (The standard range is from +6 dB to -12 dB.)
    - Built-in circuits: Gain control circuit + FET × 2 (Support for channel-separated CCDs included)
- A/D converter:
  - Half flash converter
    - Number of bits: 8
    - Conversion speed: 0.1 to 6 MHz
    - Input range: min. 3 V<sub>p-p</sub>
    - Input channels: Support for odd/even separation
- White shading correction:
  - Overall pixel correction
    - Distortion correction level: max. 75% (or max. 50%) of A/D converter's input range
- Black shading correction:
  - Overall pixel correction
    - Distortion correction level: 25% of A/D converter's input range
- MTF correction:
  - Laplacian transforms (processing for text images)
    - Reference to five pixels, max. coefficient of -1.875
    - Support for edge direction-specific processing and processing from preceding history
- Halftone processing:
  - Error dispersion processing: Reproduction of 64-gradation using 6-bit processing
  - Dither pattern: Mesh (4 × 4 or 8 × 8 pixels)
    - Bayer (4 × 4 pixels)
- Gamma correction:
  - User-definable by loading a conversion curve
    - Conversion levels: 7 bits to 6
- Binary coded:
  - Fixed slice
    - Slice level: User-specified 5-bit value
- Enlargement/reduction (line density conversion):
  - Decimation with image clock or line enable
    - Scaling factor in primary scanning direction: 0.78% to 200% (in 0.78% increments)
    - Scaling factor in subscanning direction: 0.39% to 200% (in 0.39% increments)
- Enlargement/reduction (line density conversion) correction:
  - Multivalued smoothing (for enlargement in primary direction or line density enhancement)
  - Black pixel preservation (for reduction in primary or subscanning direction or line density reduction)
  - OR processing (for line density conversion in subscanning direction from 7.7 line/mm to 3.85)
- Sensor interfaces:
  - CCD sensor
    - Supports both channel-composite and channel-separated CCDs.
    - Generates the following drive signals using user settings: FSG (SH), FCK1, FCK2 (ø1 and ø2), FR1, FR2 (RS1 and RS2)
  - Contacting bipolar image sensor
    - Generates SCLK and ST signals.

- CdS sensor
  - Generates SCLK and STPL signals.
- Memory interfaces:
  - L mode (max. 1 MHz)
    - : 256-Kbit pseudo-SRAM × 1
    - or
    - 256-Kbit SRAM × 1
    - or, if enlargement and black shading are disabled and the lines are not more than 2048 pixels long, 64-Kbit SRAM × 1
  - M mode(max.3MHz)
    - : 64-Kbit SRAM × 2
    - or, if there is enlargement or black shading
    - 64-Kbit SRAM × 3
  - H mode (max. 6 MHz)
    - : 64-Kbit SRAM × 4
    - + 5K × 8-bit FIFO × 1
  - Shading memory function (Common in L, M, and H modes)"
    - : Support for fixed ROM shading
    - : Support for automatic data transfers between shading memory and EEROM
    - : Shading memory accessible from microprocessor for read/write operations
- Image bus interface:
  - Parallel mode (DMA slave operation)
    - : 8-bit mode
    - : 16-bit mode (requires external circuitry)
  - Serial mode with request ( $\overline{VREQ}$ ) input and enable ( $\overline{VSEN}$ ), clock ( $\overline{VSCK}$ ), and data ( $\overline{VSDA}$ ) outputs
- Scanning modes:
  - Free Scan
  - Cycle scan (normal drive)
  - Cycle scan (trapezoidal drive)
  - Trigger scan
- System interface:
  - Interface to 8-bit microprocessors (Choice of Intel or Motorola formats)
- Video data register readout function:
  - Image data after A/D conversion or shading correction
    - : Maximum value for ABC interval
    - : Minimum value for offset correction interval
    - : Data at user's choice of position
- Image data I/O function:
  - Image data output after shading correction (8 bits)
  - Image data output after multivalued smoothing (7 bits)
  - Image data input sent from external A/D converter (8 bits)
- Output ports:
  - 16 pins (memory interface for L mode)
  - 3 pins (memory interface for M mode)
- Power supply:
  - Digital circuits  $DV_{DD}$ : 5.0V
  - Analog circuits  $AV_{DD}$ : 5.0V
  - A/D converter reference voltages  $V_{REFH}$ : 5.0 to 3.0 V
  - $V_{REFL}$ : 0.0 to 2.0 V

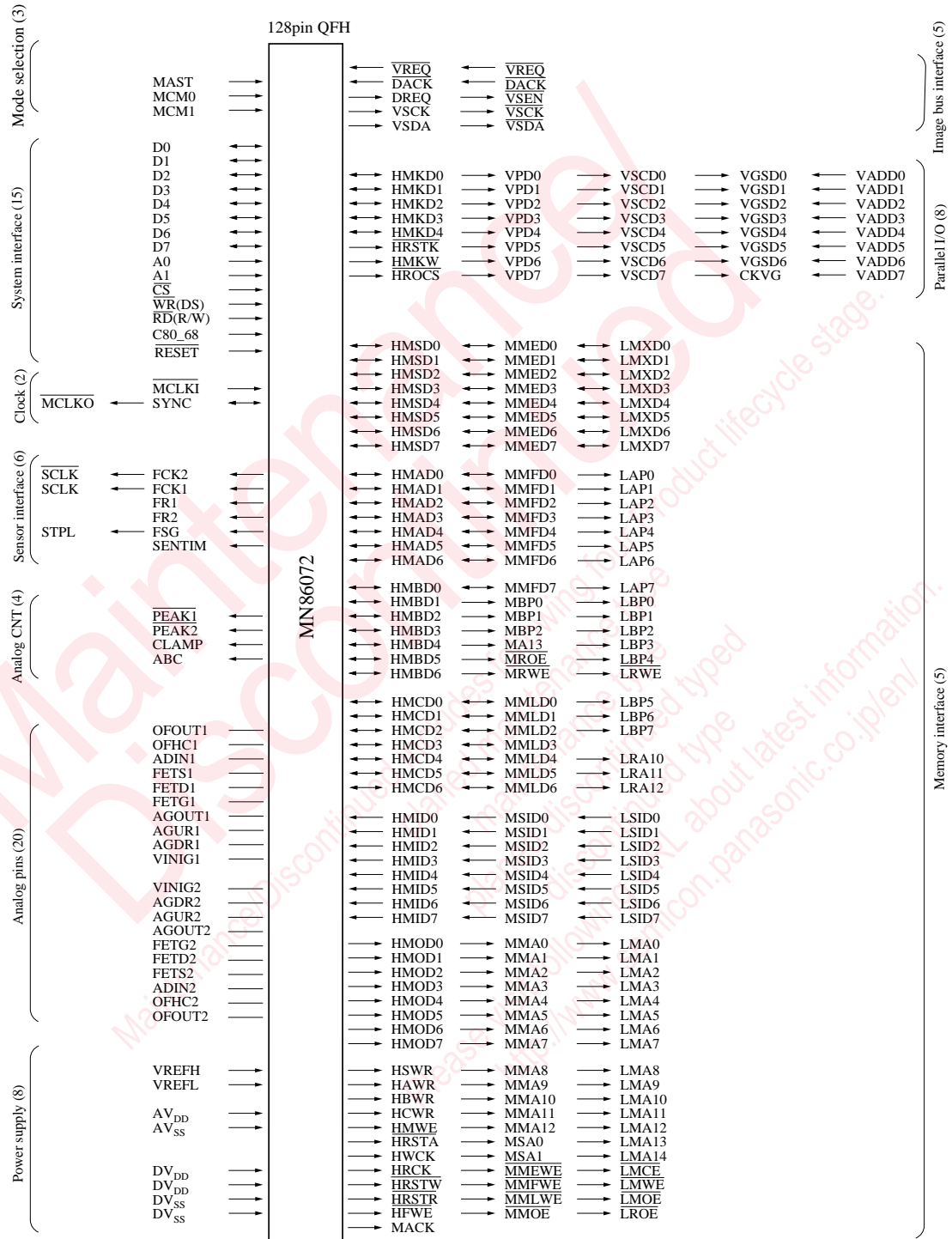
Pin Assignment

LMA8	MMA8	HSWR	97	96	HAWR	MMA9	LMA9
LROE	MMOE	HFWE	98	95	HM0D0	MMA0	LMA0
LMOE	MMLWE	HRSTR	99	94	HM0D1	MMA1	LMA1
LMWE	MMFWE	HRSTW	100	93	HM0D2	MMA2	LMA2
LMCE	MMEWE	HRCK	101	92	HM0D3	MMA3	LMA3
LMA12	MMA12	HMWE	102	91	HM0D4	MMA4	LMA4
LMA11	MMA11	HCWR	103	90	HM0D5	MMA5	LMA5
LMA10	MMA10	HBWR	104	89	HM0D6	MMA6	LMA6
LMA14	MSA1	HWCK	105	88	HM0D7	MMA7	LMA7
LSID7	MSID7	HMID7	106	87	MAST		
LSID6	MSID6	HMID6	107	86	MCM0		
LSID5	MSID5	HMID5	108	85	MCM1		
LSID4	MSID4	HMID4	109	84	FSG	STPL	
LSID3	MSID3	HMID3	110	83	FCK1	SCLK	
LSID2	MSID2	HMID2	111	82	FCK2	SCLK	
LSID1	MSID1	HMID1	112	81	FR1		
LSID0	MSID0	HMID0	113	80	FR2		
LRA12	MMLD6	HMCD6	114	79	SENTIM		
LRA11	MMLD5	HMCD5	115	78	SYNC		
LRA10	MMLD4	HMCD4	116	77	MCLKI	MCLKO	
	MMLD3	HMCD3	117	76	D0		
	MMLD2	HMCD2	118	75	D1		
LBP7	MMLD1	HMCD1	119	74	D2		
LBP6	MMLD0	HMCD0	120	73	D3		
LAP6	MMFD6	HMAD6	121	72	D4		
LAP5	MMFD5	HMAD5	122	71	D5		
LAP4	MMFD4	HMAD4	123	70	D6		
LAP3	MMFD3	HMAD3	124	69	D7		
LAP2	MMFD2	HMAD2	125	68	A0		
LAP1	MMFD1	HMAD1	126	67	A1		
LAP0	MMFD0	HMAD0	127	66	C80_08		
		DV <sub>DD</sub>	128	65	DV <sub>SS</sub>		
				64			DV <sub>DD</sub>
				63			CS
				62			RD
				61			WR
				60			RESET
				59			VPD0
				58			VPD1
				57			VPD2
				56			VPD3
				55			VPD4
				54			VPD5
				53			VPD6
				52			VPD7
				51			VSDA
				50			VSCA
				49			VSCB
				48			DACK
				47			VREQ
				46			ABC
				45			CLAMP
				44			PEAK1
				43			PEAK2
				42			VINIG1
				41			AGDR1
				40			AGUR1
				39			AGOUT1
				38			FETG1
				37			FETS1
				36			FETD1
				35			VREFL
				34			VREFH
				33			AV <sub>SS</sub>
				1			DV <sub>SS</sub>
				2			HRSTA
				3			MACK
				4			HMBD6
				5			HMBD5
				6			HMBD4
				7			HMBD3
				8			HMBD2
				9			HMBD1
				10			MMFD7
				11			MMFD0
				12			MMSD7
				13			MMSD6
				14			MMSD5
				15			MMSD4
				16			MMSD3
				17			MMSD2
				18			MMSD1
				19			MMSD0
				20			OFOUT1
				21			OFHC1
				22			OFOUT2
				23			OFHC2
				24			VINIG2
				25			AGDR2
				26			AGUR2
				27			AGOUT2
				28			FETG2
				29			FETS2
				30			FETD2
				31			AV <sub>DD</sub>
				32			ADIN1

(TOP VIEW)

QFH128-P-1818

Pin Function Chart



■ Pin Descriptions

1. Mode Selection Pins

Pin No.	Symbol	I/O	Function Description
87	MAST	O	<p>Clock synchronization selection</p> <p>H: Master mode. The chip synchronizes operation with its internal SYNC signal and feeds this signal to the SYNC pin.</p> <p>L: Slave mode. The chip synchronizes operation with the external SYNC signal from the SYNC pin.</p>
86	MCM0	I	<p>Memory interface mode selection</p> <p>These inputs select the mode for the memory interface pins, which determine the multiplier applied to master clock frequency (from the MCLKI pin).</p>
85	MCM1	I	

MAST	MCM1	MCM0	Memory Interface Mode	Clock Mode
L	L	L	L mode	Slave $f_{CKVD} \times 16$
L	L	H	M mode	Slave $f_{CKVD} \times 8$
L	H	L	H mode	Slave $f_{CKVD} \times 2$
L	H	H	T mode	Slave $f_{CKVD} \times 2$
H	L	L	L mode	Master $f_{CKVD} \times 16$
H	L	H	M mode	Master $f_{CKVD} \times 8$
H	H	L	H mode	Master $f_{CKVD} \times 2$
H	H	H	DCTEST	—

L mode (Low-speed mode)

256-Kbit pseudo-SRAM  $\times 1$  or 256-Kbit SRAM  $\times 1$

Recommended image signal frequency ( $f_{CKVD}$ ): max. 1 MHz

Master clock frequency ( $f_{MCLKI}$ ):  $f_{CKVD} \times 16$

M mode (Medium-speed mode)

64-Kbit SRAM  $\times 3$

If enlargement and black shading are disabled

64-Kbit SRAM  $\times 2$

Recommended image signal frequency ( $f_{CKVD}$ ): max. 3 MHz

Master clock frequency ( $f_{MCLKI}$ ):  $f_{CKVD} \times 8$

H mode (High-speed mode)

64-Kbit SRAM  $\times 4 + 5K \times 8$ -bit FIFO  $\times 1$

Recommended image signal frequency ( $f_{CKVD}$ ): max. 6 MHz

Master clock frequency ( $f_{MCLKI}$ ):  $f_{CKVD} \times 2$

■ Pin Descriptions (continued)

1. Mode Selection Pins (continued)

Pin No.	Symbol	I/O	Function Description												
			<p>T mode (Test data input mode)</p> <p>This mode is for testing internal functions.</p> <p>Master clock frequency (<math>f_{MCLKI}</math>): <math>f_{CKVD} \times 2</math></p> <p>DCTEST mode</p> <p>This mode configures the output and I/O pins for DC testing.</p> <table border="1" data-bbox="696 636 1338 787"> <thead> <tr> <th>HMID0</th> <th>HMID1</th> <th>DC Test Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>—</td> <td>Output high-impedance test</td> </tr> <tr> <td>1</td> <td>0</td> <td>"L" level output test</td> </tr> <tr> <td>1</td> <td>1</td> <td>"H" level output test</td> </tr> </tbody> </table>	HMID0	HMID1	DC Test Function	0	—	Output high-impedance test	1	0	"L" level output test	1	1	"H" level output test
HMID0	HMID1	DC Test Function													
0	—	Output high-impedance test													
1	0	"L" level output test													
1	1	"H" level output test													

2. System Interface Pins

Pin No.	Symbol	I/O	Function Description
76 to 69	D0 to D7	I/O	Microprocessor data I/O bus
68, 67	A0, A1	I	Microprocessor address input
63	$\overline{CS}$	I	Microprocessor chip select input
61	$\overline{WR}(DS)$	I	Microprocessor data write input (Set C80_68 pin at "H" level) Microprocessor data strobe input (Set C80_68 pin at "L" level)
62	$\overline{RD}(R/W)$	I	Microprocessor data read input (Set C80_68 pin at "H" level) Microprocessor data read/write input (Set C80_68 pin at "L" level)
66	C80_68	I	Microprocessor selection input L: Motorola H: Intel
60	$\overline{RESET}$	I	System reset input

■ Pin Descriptions (continued)

3. Clock Pins

Pin No.	Symbol	I/O	Function Description									
77	$\overline{\text{MCLKI}}$	I	<p>Master clock input</p> <p>Clock frequency:                      Image signal frequency <math>\times 2</math> (H mode memory interface)                      Image signal frequency <math>\times 8</math> (M mode memory interface)                      Image signal frequency <math>\times 16</math> (L mode memory interface)</p> <p>Clock duty: 50%</p>									
78	$\overline{\text{SYNC}}$	I/O	<p>Clock synchronization signal I/O</p> <p>Start timing pulse for individual lines</p> <table border="1"> <thead> <tr> <th>MAST</th> <th>SYSL (TIM2 REG)</th> <th>Remarks</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>—</td> <td>SYNC input</td> </tr> <tr> <td>H</td> <td>1</td> <td>SYNC output</td> </tr> </tbody> </table>	MAST	SYSL (TIM2 REG)	Remarks	L	—	SYNC input	H	1	SYNC output
	MAST	SYSL (TIM2 REG)	Remarks									
L	—	SYNC input										
H	1	SYNC output										
$\overline{\text{MCLKO}}$	O	<p>Internal master clock output.</p> <p>This pin provides the internal master clock, the signal from the <math>\overline{\text{MCLKI}}</math> pin.</p> <table border="1"> <thead> <tr> <th>MAST</th> <th>SYSL (TIM2 REG)</th> <th>Remarks</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>0</td> <td>MCLK output</td> </tr> </tbody> </table>	MAST	SYSL (TIM2 REG)	Remarks	H	0	MCLK output				
MAST	SYSL (TIM2 REG)	Remarks										
H	0	MCLK output										



■ Pin Descriptions (continued)

4. Sensor Interface Pins

Pin No.	Symbol	I/O	Function Description															
83	FCK1	O	CCD: 1 (TIM 1 REG) Reduced CCD sensor. $\phi 1$ clock: CKVD/2.															
	SCLK	O	CCD: 0 (TIM 1 REG) CdS or bipolar image sensor. SCLK clock: $\overline{\text{CKVD}}$															
82	FCK2	O	CCD: 1 (TIM 1 REG) Reduced CCD sensor. $\phi 2$ clock: CKVD/2.															
	$\overline{\text{SCLK}}$	O	CCD: 0 (TIM 1 REG) CdS or bipolar image sensor. SCLK clock: CKVD															
84	FSG	O	CCD: 1, CONTA: — (TIM 1 REG) Reduced CCD sensor. $\phi \text{SG}$															
	ST	O	CCD: 0, CONTA: 0 (TIM 1 REG) Bipolar image sensor. ST = Start puls															
	STPL	O	CCD: 0, CONTA: 0 (TIM 1 REG) CdS sensor. STPL = Start pulse															
81	FR1	O	FRM2: 0 Reduced CCD sensor. $\phi \text{R1}$ clock (parallel mode) FRM2: 1 Reduced CCD sensor. $\phi \text{R}$ clock (serial mode)															
80	FR2	O	FRM2: 0 Reduced CCD sensor. $\phi \text{R2}$ clock (parallel mode) FRM2: 1 Reduced CCD sensor. $\phi \text{SP}$ clock (serial mode)															
79	SENTIM	O	Sensor timing output pin <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>STM1 (TIM2 REG)</th> <th>STM0 (TIM2 REG)</th> <th>SETIM output signal</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Offset enable</td> </tr> <tr> <td>0</td> <td>1</td> <td>ABC enable</td> </tr> <tr> <td>1</td> <td>0</td> <td>User-defined timing (for all lines read)</td> </tr> <tr> <td>1</td> <td>1</td> <td>User-defined timing (for valid lines only)</td> </tr> </tbody> </table>	STM1 (TIM2 REG)	STM0 (TIM2 REG)	SETIM output signal	0	0	Offset enable	0	1	ABC enable	1	0	User-defined timing (for all lines read)	1	1	User-defined timing (for valid lines only)
STM1 (TIM2 REG)	STM0 (TIM2 REG)	SETIM output signal																
0	0	Offset enable																
0	1	ABC enable																
1	0	User-defined timing (for all lines read)																
1	1	User-defined timing (for valid lines only)																

■ Pin Descriptions (continued)

5. Sensor Drive Pins

Pin No.	Symbol	I/O	Function Description
44	$\overline{\text{PEAK1}}$	O	Gain control signal 1 (Overflow 1) "L" level: Reduce gain. "H" level: Increase gain.
43	$\overline{\text{PEAK2}}$	O	Gain control signal 2 (Overflow 2) "L" level: Reduce gain. "H" level: Increase gain.
45	CLAMP	O	Clamp (offset correction) interval signal. "L" level: Hold. "H" level: Sample (offset adjustment operation).
46	ABC	O	ABC effective interval signal. "L" level: Hold gain. "H" level: Adjust gain.

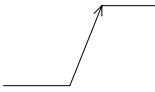
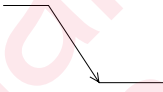
■ Pin Descriptions (continued)

6. Image Bus Interface Pins

Pin No.	Symbol	I/O	Function Description
47	$\overline{\text{VREQ}}$	I	<p>Video request.</p> <p>This pin accepts image data transfer requests from the controlled device.</p> <p>"L" level: Transfer request enable.</p> <p>"H" level: Transfer request disable.</p> <p>In the trigger scan mode, pulling this pin to "L" level forces the sensor start (STPL) pin to "L" level to start sensor readout. After image-processing a line of data, the image data are outputted at the VSDA pin.</p> <p>In the cycle scan mode, pulling this pin to "L" level enables the next readout line. After image-processing a line of data, the image data are outputted at the VSDA pin.</p> <p>In the free scan mode, the chip ignores this pin, sensor readout starts at the interval specified with the timing settings, and the image data are outputted at the VSDA pin after processing each line of data.</p>
49	DREQ	O	<p>Parallel mode (IPARA (IBCNT REGI): 1)</p> <p>Parallel data transfer request.</p> <p>"L" level: Transfer request enable.</p> <p>"H" level: Transfer request disable.</p>
	$\overline{\text{VSEN}}$	O	<p>Serial mode (IPARA (IBCNT REGI): 0)</p> <p>Video enable</p> <p>"L" level: Image data enable.</p> <p>"H" level: Image data disable.</p>
48	$\overline{\text{DACK}}$	I	<p>Parallel data acknowledge.</p> <p>Data transfer acknowledge signal in response to DREQ.</p> <p>"L" level: Data transfer enable.</p> <p>"H" level: Data transfer disable.</p>

■ Pin Descriptions (continued)

6. Image Bus Interface Pins (continued)

Pin No.	Symbol	I/O	Function Description
50	V $\overline{\text{SCK}}$	O	Parallel mode (IPARA (IBCNT REGI): 1) Video serial clock (signal for external circuitry).  Timing for reading VSDA data.
	$\overline{\text{VSDA}}$	O	Serial mode (IPARA (IBCNT REGI): 0) Video serial clock.  Timing for reading VSDA data.
51	VSDA	O	Parallel mode (IPARA (IBCNT REGI): 1) Video serial data. (signal for external circuitry). Binary image data output. "L" level: Black. "H" level: White.
	$\overline{\text{VSDA}}$	O	Serial mode (IPARA (IBCNT REGI): 0) Video serial data. Binary image data output. "L" level: Black. "H" level: White.

■ Pin Descriptions (continued)

7. Parallel I/O Pins

Pin No.	Symbol	I/O	Function Description
52	VADD7	I	PSD2: 0, PSD1: 0, PSD0: — (IBCNT REGI) External A/D converter signal input
	HROCS	O	PSD2: 0, PSD1: 1, PSD0: — (IBCNT REGI) Shading ROM chip select
	VPD7	O/Hi-z	PSD2: 1, PSD1: 0, PSD0: 0 (IBCNT REGI) Binary parallel image output (parallel interface) $\overline{\text{DACK}}$ : L Output. $\overline{\text{DACK}}$ : H High-impedance.
	VSCD7	O	PSD2: 1, PSD1: 0, PSD0: 1 (IBCNT REGI) Output pin for image signal after shading correction
	CKVG	O	PSD2: 1, PSD1: 1, PSD0: 0 (IBCNT REGI) Multivalue image signal synchronization clock output
	SBUS7	O	PSD2: 1, PSD1: 1, PSD0: 1 (IBCNT REGI) Internal DBUS data output
	53	VADD6	I
HKWR		O	PSD2: 0, PSD1: 1, PSD0: — (IBCNT REGI) HMKD write/read output
VPD6		O/Hi-z	PSD2: 1, PSD1: 0, PSD0: 0 (IBCNT REGI) Binary parallel image output (parallel interface) $\overline{\text{DACK}}$ : L Output. $\overline{\text{DACK}}$ : H High-impedance.
VSCD6		O	PSD2: 1, PSD1: 0, PSD0: 1 (IBCNT REGI) Output pin for image signal after shading correction
VGSD6		O	PSD2: 1, PSD1: 1, PSD0: 0 (IBCNT REGI) Multivalue image signal output
SBUS6		O	PSD2: 1, PSD1: 1, PSD0: 1 (IBCNT REGI) Internal DBUS data output
54		VADD5	I
	HRSTK	O	PSD2: 0, PSD1: 1, PSD0: — (IBCNT REGI) External address control clear for black shading
	VPD5	O/Hi-z	PSD2: 1, PSD1: 0, PSD0: 0 (IBCNT REGI) Binary parallel image output (parallel interface) $\overline{\text{DACK}}$ : L Output. $\overline{\text{DACK}}$ : H High-impedance.
	VSCD5	O	PSD2: 1, PSD1: 0, PSD0: 1 (IBCNT REGI) Output pin for image signal after shading correction

■ Pin Descriptions (continued)

7. Parallel I/O Pins (continued)

Pin No.	Symbol	I/O	Function Description
54	VGSD5	O	PSD2: 1, PSD1: 1, PSD0: 0 (IBCNT REG1) Multivalue image signal output
	SBUS5	O	PSD2: 1, PSD1: 1, PSD0: 1 (IBCNT REG1) Internal DBUS data output
55 to 59	VADD4 VADD0	I	PSD2: 0, PSD1: 0, PSD0: — (IBCNT REG1) External A/D converter output
	HMKD4 to HMKD0	I/O	PSD2: 0, PSD1: 1, PSD0: — (IBCNT REG1) Black shading correction data I/O. HKWR: L Input. HKWR: H High-impedance.
	VPD4 to VPD0	O/Hi-z	PSD2: 1, PSD1: 0, PSD0: 0 (IBCNT REG1) Binary parallel image signal output (parallel interface) $\overline{\text{DACK}}$ : L Output. $\overline{\text{DACK}}$ : H High-impedance.
	VSCD4 to VSCD0	O	PSD2: 1, PSD1: 0, PSD0: 1 (IBCNT REG1) Shading correction data I/O.
	VGSD4 to VGSD0	O	PSD2: 1, PSD1: 1, PSD0: 0 (IBCNT REG1) Multivalue image signal output
	SBUS4 to SBUS0	O	PSD2: 1, PSD1: 1, PSD0: 1 (IBCNT REG1) Internal DBUS data output

\*1 VPD0 to 7  
1: Black      Data direction: MSB first  
0: White

\*2 VPD0 to 7  
X'FF' to X'00': "White" to "Black"

\*3 VGSD 0 to 6  
X'7F' to X'00': "White" to "Black"

\*4 VADD0 to 7  
X'FF' to X'00': "White" to "Black"

■ Pin Descriptions (continued)

8. Memory interface pins

Function is selected by the memory control register (MECR) and mode pins of MCMO (Pin No. 86) and of MCM1 (Pin No. 85).

Mode	Mode pins		MECR		Image processing functions			Notes
	MCM1	MCM0	RSH	MAG	Shading		Enlarge-ment	
					White Correc-tion	Black Correc-tion		
L	L	L	0	0	●	×	×	Image signal frequency: Max. 625kHz to 1MHz  Memory selection bit, STK. 0: SRAM or PSRAM 1: PSRAM  EXSCD *1 0: Internal SCD processing. 1: External SCD input.
			0	1	●	●	●	
			1	0	Fixed in ROM	×	×	
			1	1	Fixed in ROM	●	●	
M	L	H	0	–	●	●	●	Image signal frequency: Max. 3 MHz EXSCD *1 0: Internal SCD processing. 1: External SCD input.  STK:– Disabling black correction and enlargement reduces memory requirements to two SRAMs.
			1	1	Fixed in ROM	●	●	
H	H	L	–	–	● Fixed in ROM	●	●	Image signal frequency: Max. 6 MHz EXSCD *1 0: Internal SCD processing. 1: External SCD input. STK:–

Note\*1: SCD is the data after shading correction.

■ Pin Descriptions (continued)

8.1 L Mode

Pin No.	Symbol	I/O	Function Description
18 to 11	LMXD0 to LMXD7	I/O	RAM data I/O bus. I/O data bus for white shading data, black shading data, error dispersion processing error data, and 2-line image data."
95 to 88 97 96 104 103 102 2 105	LMA0 to LMA7 LMA8 LMA9 LMA10 LMA11 LMA12 LMA13 LMA14	O	RAM address
99	$\overline{\text{LMOE}}$	O	RAM OE control
100	$\overline{\text{LMWE}}$	O	RAM WE control
101	$\overline{\text{LMCE}}$	O	Pseudo-SRAM chip select control
103 to 106	LSID0 to LSID7	I	White shading ROM data input. Input for data after external shading correction.
98	$\overline{\text{LROE}}$	O	White shading ROM OE control.
4	$\overline{\text{LRWE}}$	O	EEROM WE control
116 to 114	LRA10 to LRA12	O	Upper address of EEROM (The lower bits use LMA0–LMA9.)
127 to 121 10	LAP0 to LAP6 LAP7	O	Output port A (8 bits)
9 to 5 120 119 118	LBP0 to LBP4 LBP5 LBP6 LBP7	O	Output port B (8 bits)



■ Pin Descriptions (continued)

8.2 M Mode

Pin No.	Symbol	I/O	Function Description
18 to 11	MMED0 to MMED7	I/O	RAM data I/O. White shading data and error dispersion processing error data.
127 to 121 10	MMFD0 to MMFD6 MMFD7	I/O	RAM data I/O. Black shading data and error dispersion processing error data (for use in enlargement).
120 to 114	MMLD0 to MMLD6	I/O	RAM data I/O. 2-line image data.
113 to 106	MSID0 to MSID7	I	White shading ROM data input, or input for data after external shading correction.
95 to 88 97 96 104 to 102 6	MMA0 to MMA7 MMA8 MMA9 MMA10 to MMA12 MMA13	O	RAM address
2 105	MSA0 MSA1	O	Upper address of RAM
101 100 99	$\overline{\text{MMEWE}}$ $\overline{\text{MMFWE}}$ $\overline{\text{MMLWE}}$	O	RAM WE control
98	$\overline{\text{MMOE}}$	O	RAM OE control
5	$\overline{\text{MROE}}$	O	White shading ROM and EEROM OE control
4	$\overline{\text{MRWE}}$	O	EEROM WE control
9 to 7	MBP0 to MBP2	O	Output port B (3 bits)

■ Pin Descriptions (continued)

8.3 H Mode

Pin No.	Symbol	I/O	Function Description
18 to 11	HMSD0 to HMSD7	I/O	RAM data I/O. White shading data.
127 to 121	MMAD0 to MMAD6	I/O	RAM data I/O. One-line image data.
10 to 4	MMBD0 to MMBD6	I/O	RAM data I/O. One-line image data.
120 to 114	MMCD0 to MMCD6	I/O	RAM data I/O. One-line image data.
113 to 106	HMID0 to HMID7	I	FIFO data input. Error dispersion processing error data.
95 to 88	HMOD0 to HMOD7	O	FIFO data input. Error dispersion processing error data.
97 96 104 103	HMSWR HMAWR HMBWR HMCWR	O	RAM OE control
102	HMWE	O	RAM WE control (needs NAND gate)
105	HWCK	O	FIFO WCK
101	HRCK	O	FIFO RCK
100	$\overline{\text{HRSTW}}$	O	FIFO RSTW
99	$\overline{\text{HRSTR}}$	O	FIFO RSTR
98	$\overline{\text{HFWE}}$	O	FIFO WE
3	MACK	O	RAM address counter clock
2	$\overline{\text{HRSTA}}$	O	RAM address counter clear

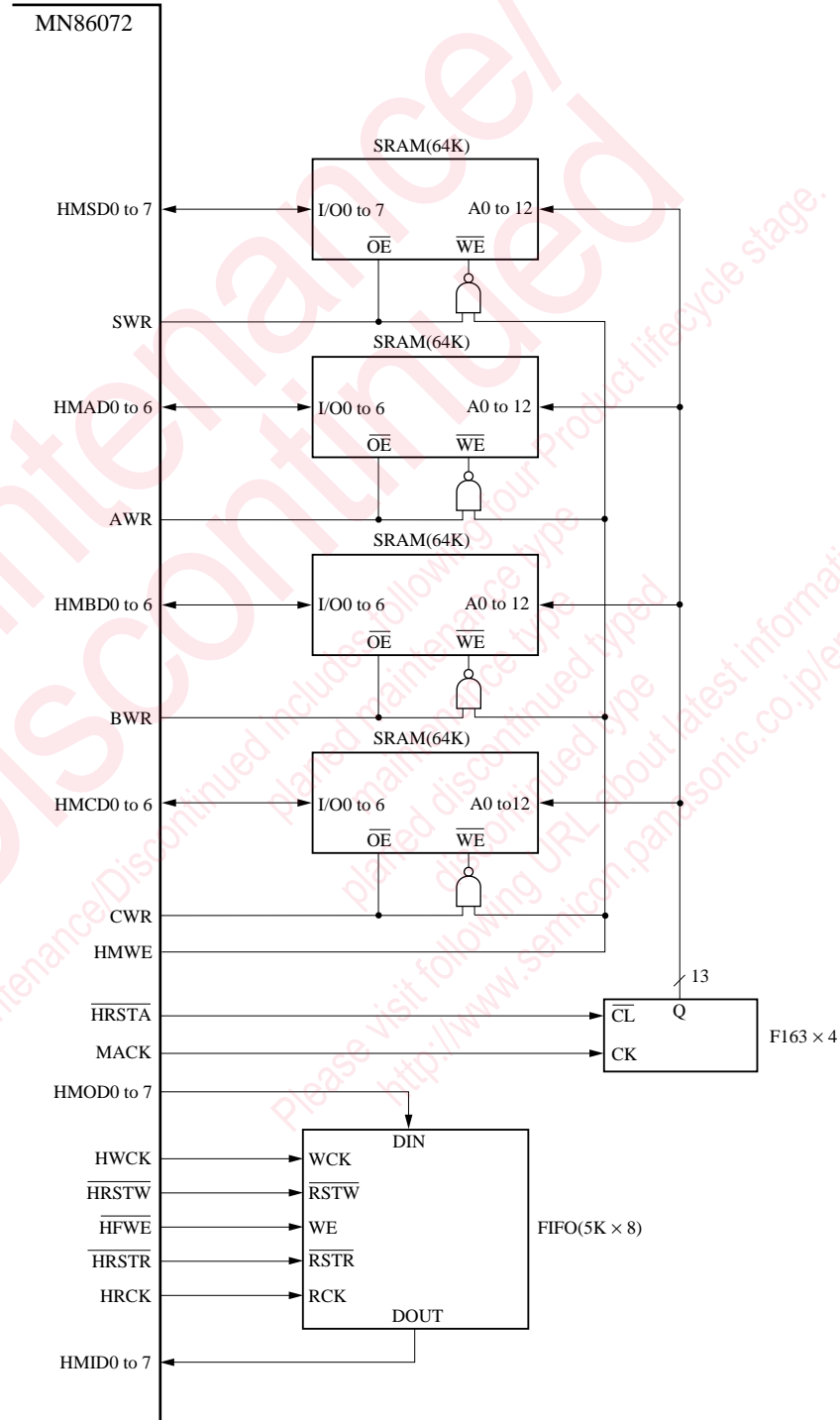
■ Application Circuit Example (1)

H Mode

White correction (without SMA mode) with no black correction

Memory configuration: 64-Kbit SRAM × 4

5K × 8-bit FIFO × 1



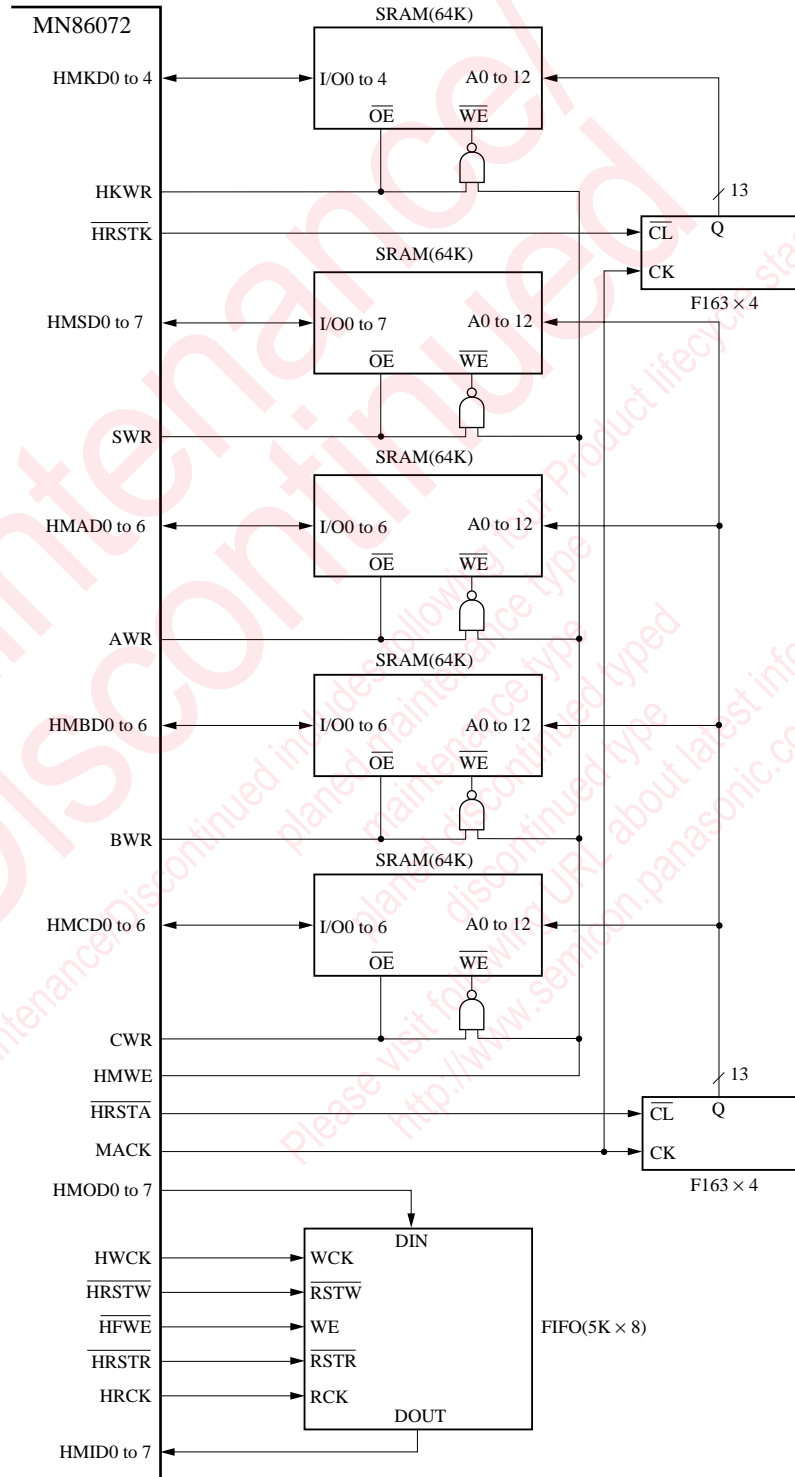
■ Application Circuit Example (2)

H Mode

White correction (without SMA mode) with black correction

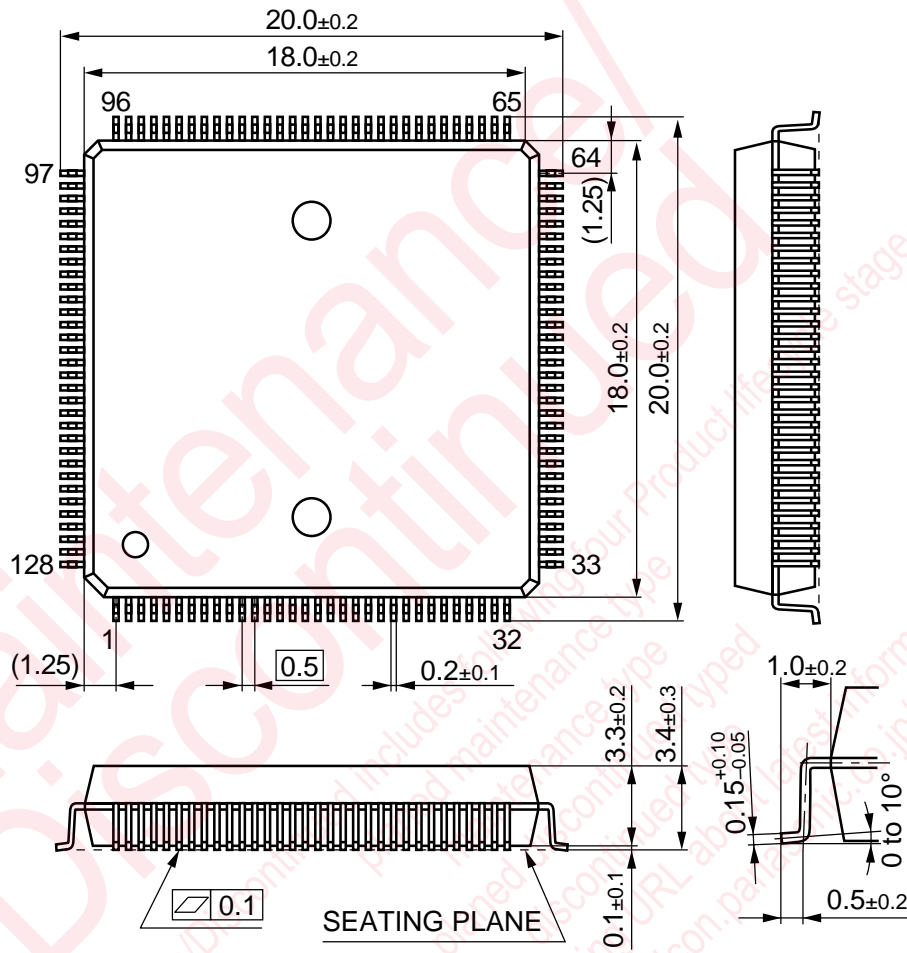
Memory configuration: 64-Kbit SRAM × 4

5K × 8-bit FIFO × 1



■ Package Dimensions (Unit: mm)

QFH128-P-1818



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