

HM514260, HM514260L Series

262,144-word × 16-bit Dynamic Random Access Memory

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM514260 are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM514260 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514260 offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM514260 to be packaged in standard 400-mil 40-pin plastic SOJ, standard 475-mil 40-pin plastic ZIP, and 400-mil 40-pin plastic TSOP.

Features

- Single 5 V (± 10%)
- High speed
 - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
 - Active mode: 935 mW/825 mW/715 mW (max)
 - Standby mode: 11 mW (max)
1.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
128 ms (L-version)
- 2 $\overline{\text{CAS}}$ byte control
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- Battery back up operation (L-version)

Ordering Information

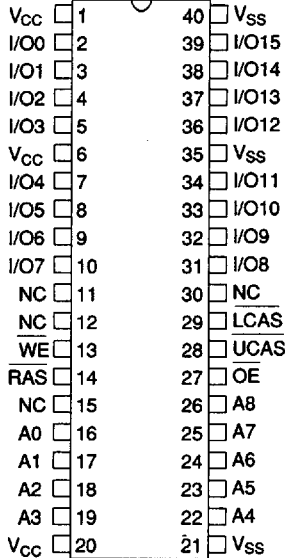
Type No.	Access time	Package
HM514260JP-7	70 ns	400-mil 40-pin plastic SOJ (CP-40D)
HM514260JP-8	80 ns	
HM514260JP-10	100 ns	
HM514260ZP-7	70 ns	475-mil 40-pin plastic ZIP (ZP-40)
HM514260ZP-8	80 ns	
HM514260ZP-10	100 ns	
HM514260TT-7	70 ns	400-mil 40-pin plastic TSOP (TTP-40DB)
HM514260TT-8	80 ns	
HM514260TT-10	100 ns	
HM514260LJP-7	70 ns	400-mil 40-pin plastic SOJ (CP-40D)
HM514260LJP-8	80 ns	
HM514260LJP-10	100 ns	
HM514260LZP-7	70 ns	475-mil 40-pin plastic ZIP (ZP-40)
HM514260LZP-8	80 ns	
HM514260LZP-10	100 ns	
HM514260LTT-7	70 ns	400-mil 40-pin plastic TSOP (TTP-40DB)
HM514260LTT-8	80 ns	
HM514260LTT-10	100 ns	

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Pin Arrangement

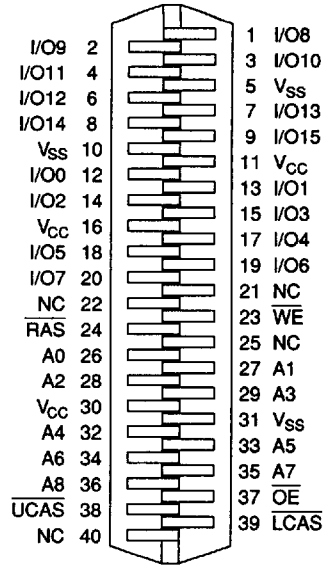
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HM514260JP/LJP Series



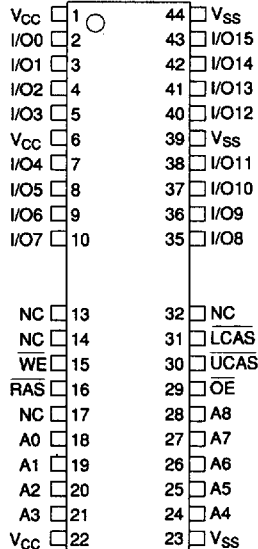
(Top View)

HM514260ZP/LZP Series



(Bottom View)

HM514260TT/LTT Series



(Top View)

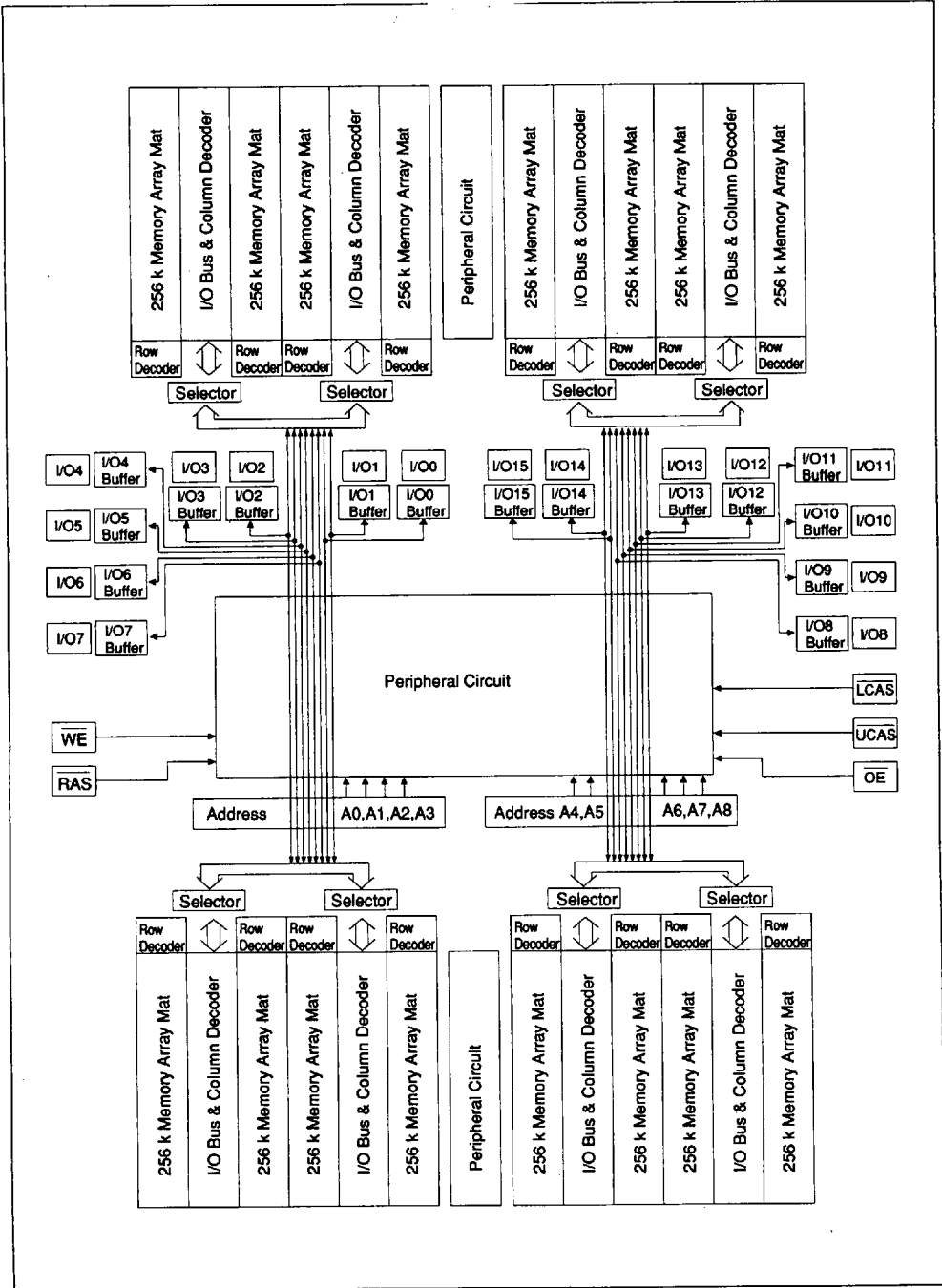
Pin Description

Pin name	Function
A0 – A8	Address input – Row address A0 – A8 – Column address A0 – A8 – Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/write enable
OE	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

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Block Diagram

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HM514260, HM514260L Series**Truth Table****HITACHI/ LOGIC/ARRAYS/MEM**

Inputs					I/O		Operation
RAS	LCAS	UCAS	WE	OE	I/O0 - I/O7	I/O8 - I/O15	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

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Recommended DC Operating Conditions (Ta = 0 to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.5	5.0	5.5	V	1
Input high voltage	V _{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin) V _{IL}	-1.0	—	0.8	V	1
	(Others) V _{IL}	-2.0	—	0.8	V	1

- Notes: 1. All voltage referenced to V_{SS}
 2. The supply voltage with all V_{CC} pins must be on the same level.
 The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

HM514260-7 HM514260-8 HM514260-10

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I _{CC1}	—	170	—	150	—	130	mA	RAS cycling LCAS or UCAS cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, LCAS, UCAS = V _{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, LCAS, UCAS ≥ V _{CC} - 0.2 V Dout = High-Z	
Standby current (L-version)		—	200	—	200	—	200	μA	CMOS interface RAS, LCAS, UCAS ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	150	—	130	—	110	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} LCAS or UCAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	150	—	130	—	110	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	130	—	120	—	110	mA	t _{PC} = min	1, 3

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DC Characteristics (Ta = 0 to 70°C, VCC = 5 V ± 10%, VSS = 0 V) (cont)

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Battery back up current (Standby with CBR refresh) (L-version)	I _{CC10}	—	300	—	300	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: t _{RC} = 125 μs t _{RAS} ≤ 1 μs, CAS = V _{IL} WE = V _{IH}	4
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes:
1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while RAS = V_{IL}.
 3. Address can be changed once or less while LCAS and UCAS = V_{IH}.
 4. V_{IH} ≥ V_{CC} - 0.2 V, V_{IL} ≤ 0.2 V

Capacitance (Ta = 25°C, VCC = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	5	pF	1
Input capacitance (Clocks)	C _{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C _{I/O}	—	10	pF	1, 2

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. LCAS and UCAS = V_{IH} to disable Dout

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AC Characteristics (Ta = 0 to 70°C, VCC = 5 V ± 10%, VSS = 0 V) *1,*14,*15,*17,*18

Test Conditions

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- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + CL (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	130	—	150	—	180	—	ns	
RAS precharge time	t _{RP}	50	—	60	—	70	—	ns	
RAS pulse width	t _{RAS}	70	10000	80	10000	100	10000	ns	
CAS pulse width	t _{CAS}	20	10000	20	10000	25	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	15	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	19
Column address hold time	t _{CAH}	15	—	15	—	20	—	ns	19
RAS to CAS delay time	t _{RCD}	20	50	20	60	25	75	ns	.8
RAS to column address delay time	t _{RAD}	15	35	15	40	20	55	ns	9
RAS hold time	t _{RSH}	20	—	20	—	25	—	ns	
CAS hold time	t _{CSH}	70	—	80	—	100	—	ns	
CAS to RAS precharge time	t _{CRP}	15	—	15	—	15	—	ns	20
OE to Din delay time	t _{ODD}	20	—	20	—	25	—	ns	
OE delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	
CAS setup time from Din	t _{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	7
Refresh period	t _{REF}	—	8	—	8	—	8	ms	
Refresh period (L-version)	t _{REF}	—	128	—	128	—	128	ms	

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Read Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from RAS	t _{RAC}	—	70	—	80	—	100	ns	2, 3
Access time from CAS	t _{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access time from address	t _{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from OE	t _{OAC}	—	20	—	20	—	25	ns	
Read command setup time	t _{RCS}	0	—	0	—	0	—	ns	19
Read command hold time to CAS	t _{RCH}	0	—	0	—	0	—	ns	16, 19
Read command hold time to RAS	t _{RRH}	0	—	0	—	0	—	ns	16
Column address to RAS lead time	t _{RAL}	35	—	40	—	55	—	ns	
Output buffer turn-off time	t _{OFF1}	0	15	0	15	0	20	ns	6
Output buffer turn-off to OE	t _{OFF2}	0	15	0	15	0	20	ns	6
CAS to Din delay time	t _{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	10, 19
Write command hold time	t _{WCH}	15	—	15	—	20	—	ns	20
Write command pulse width	t _{WP}	10	—	10	—	20	—	ns	
Write command to RAS lead time	t _{RWL}	20	—	20	—	25	—	ns	
Write command to CAS lead time	t _{CWL}	20	—	20	—	25	—	ns	21
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	11, 19
Data-in hold time	t _{DH}	15	—	15	—	20	—	ns	11, 19
CAS to OE delay time	t _{COD}	—	0	—	0	—	0	ns	23

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Read-Modify-Write Cycle

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Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	180	—	200	—	245	—	ns	
RAS to WE delay time	t _{RWD}	95	—	105	—	135	—	ns	10
CAS to WE delay time	t _{CWD}	45	—	45	—	60	—	ns	10
Column address to WE delay time	t _{AWD}	60	—	65	—	80	—	ns	10, 13
OE hold time from WE	t _{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

HM514260-7 HM514260-8 HM514260-10

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
CAS setup time (CAS-before-RAS refresh cycle)	t _{CSR}	10	—	10	—	10	—	ns	19
CAS hold time (CAS-before-RAS refresh cycle)	t _{CHR}	10	—	10	—	10	—	ns	20
RAS precharge to CAS hold time	t _{RPC}	10	—	10	—	10	—	ns	19
CAS precharge time in normal mode	t _{CPN}	10	—	10	—	10	—	ns	22

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Fast Page Mode Cycle

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HM514260-7 HM514260-8 HM514260-10

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	50	—	55	—	60	—	ns	
Fast page mode \overline{CAS} precharge time	t_{CP}	15	—	15	—	15	—	ns	22
Fast page mode \overline{RAS} pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from \overline{CAS} precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13, 20
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast page mode read-modify-write cycle \overline{CAS} precharge to \overline{WE} delay time	t_{CPW}	65	—	70	—	85	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	110	—	ns	

Counter Test Cycle

HM514260-7 HM514260-8 HM514260-10

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
\overline{CAS} precharge time in counter test cycle	t_{CPT}	50	—	50	—	50	—	ns	22

- Notes:
- AC measurements assume $t_T = 5$ ns.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 - $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .

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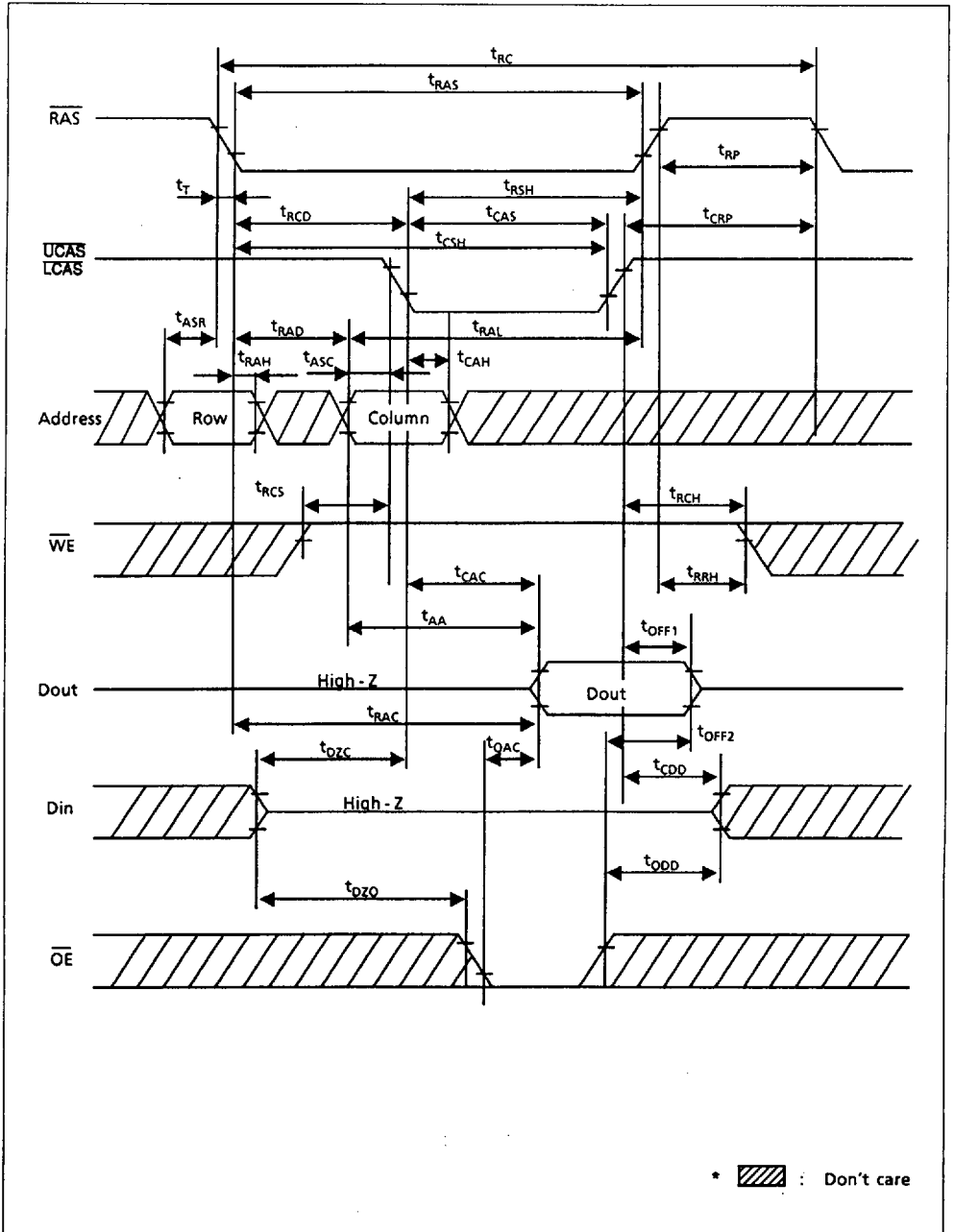
10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be straggled within the same write/read cycles.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. t_{ASC} , t_{CAH} , t_{RCS} , t_{RCH} , t_{WCS} , t_{WCH} , t_{DS} , t_{DH} , t_{CSR} , and t_{PPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
20. t_{CRP} , t_{CHR} , t_{ACP} , and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
21. t_{CWL} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
22. t_{CPN} , t_{CP} , and t_{CPT} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
23. Do not enable Dout buffer when using delayed write timing.

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Timing Waveforms

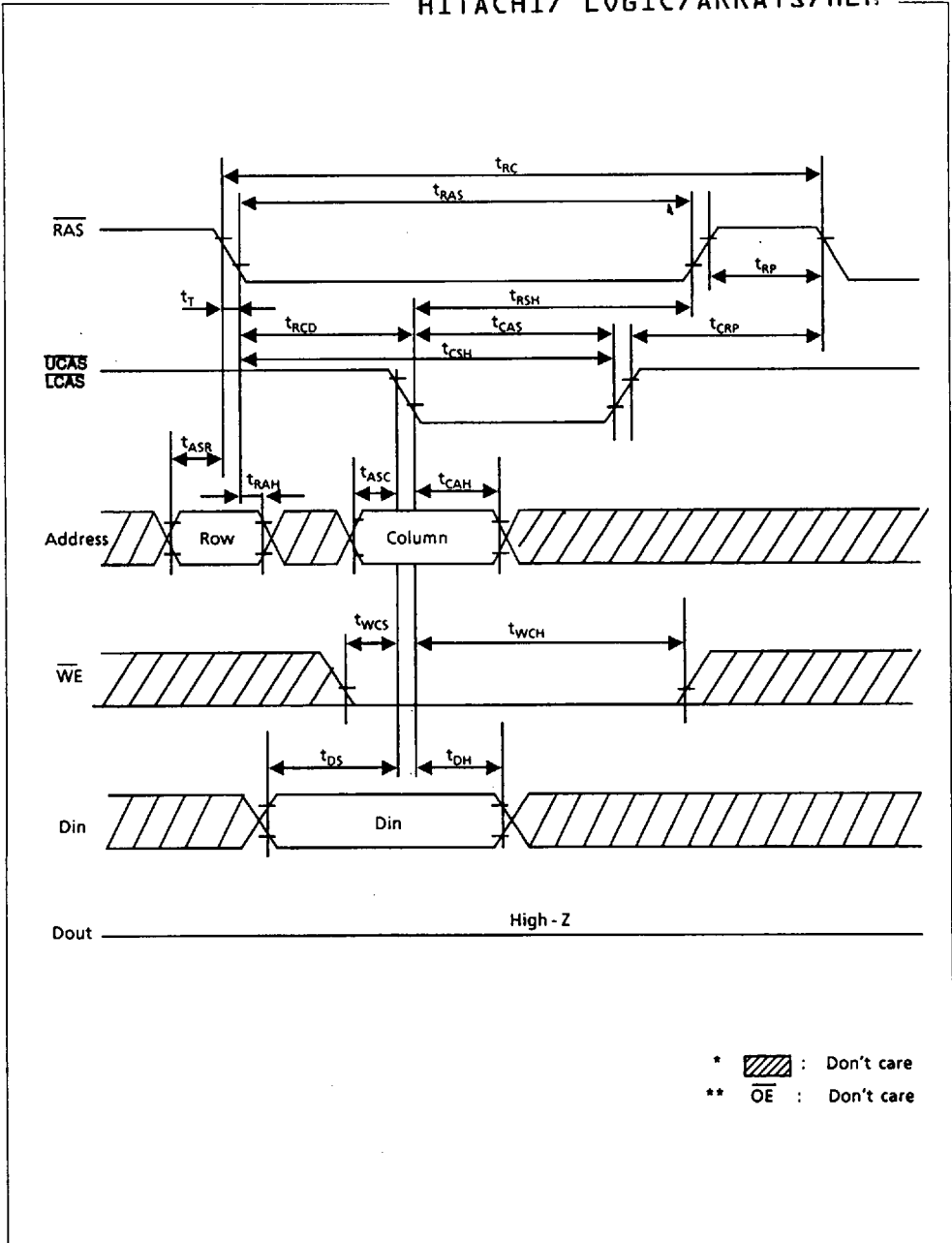
Read Cycle



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Early Write Cycle

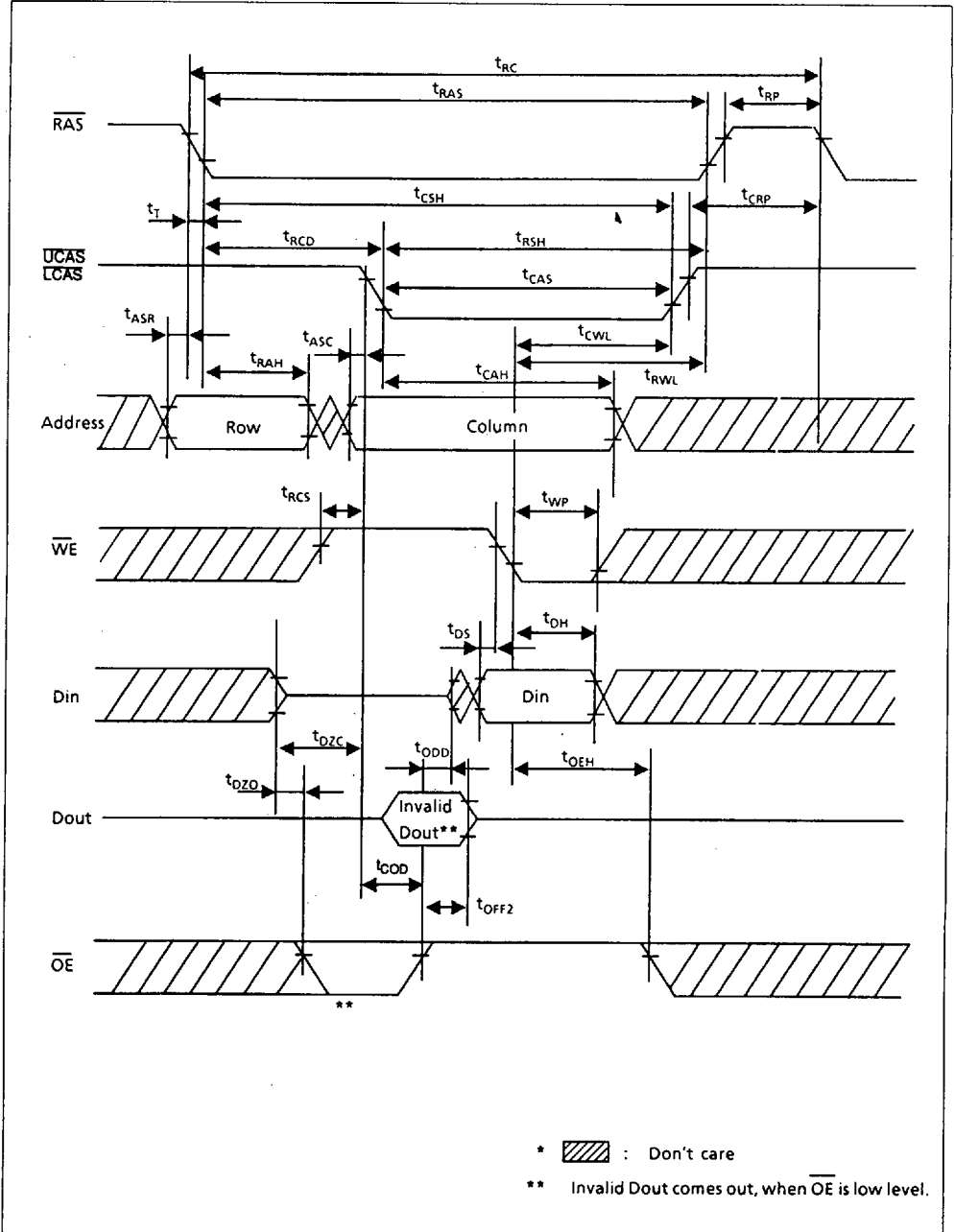
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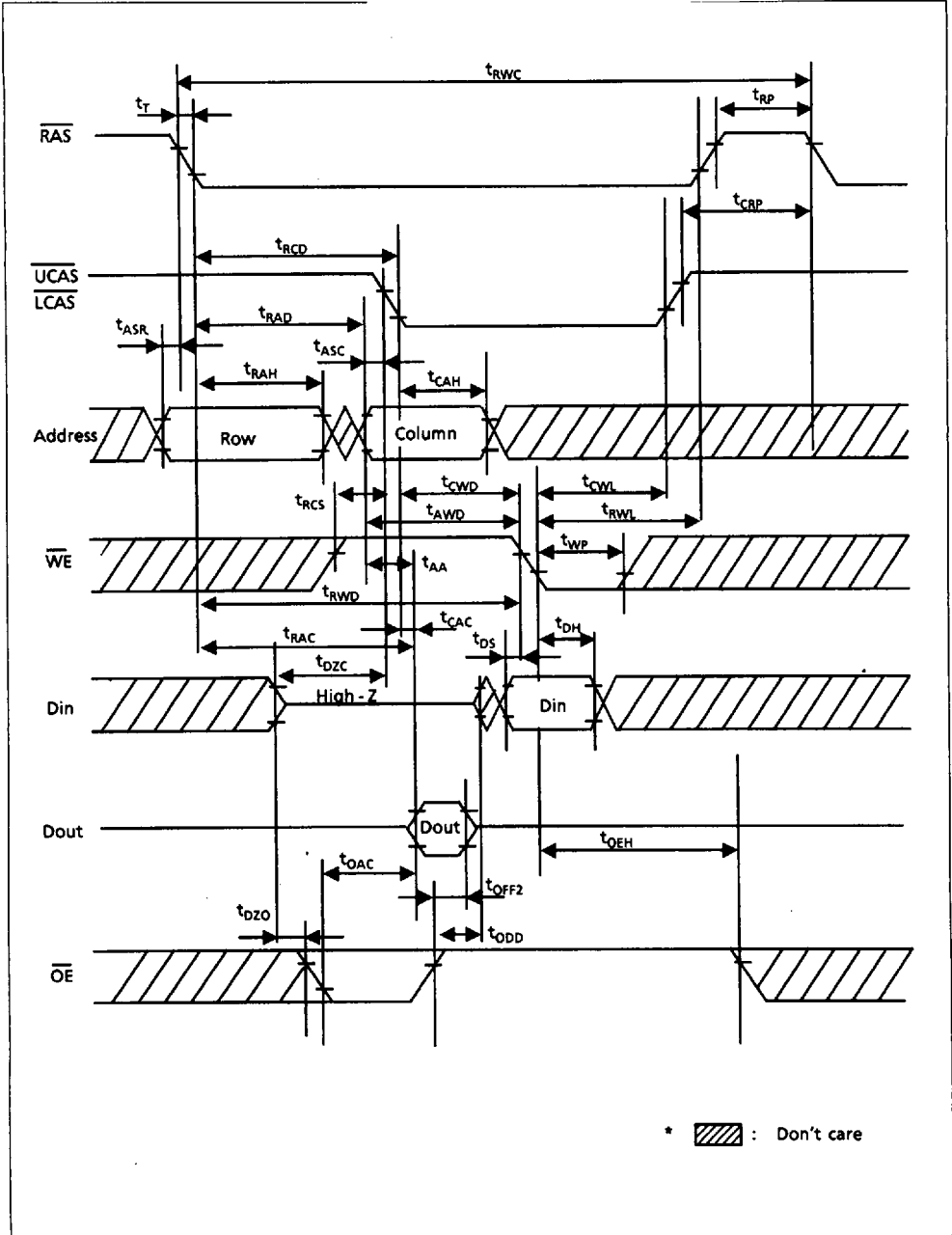
Delayed Write Cycle



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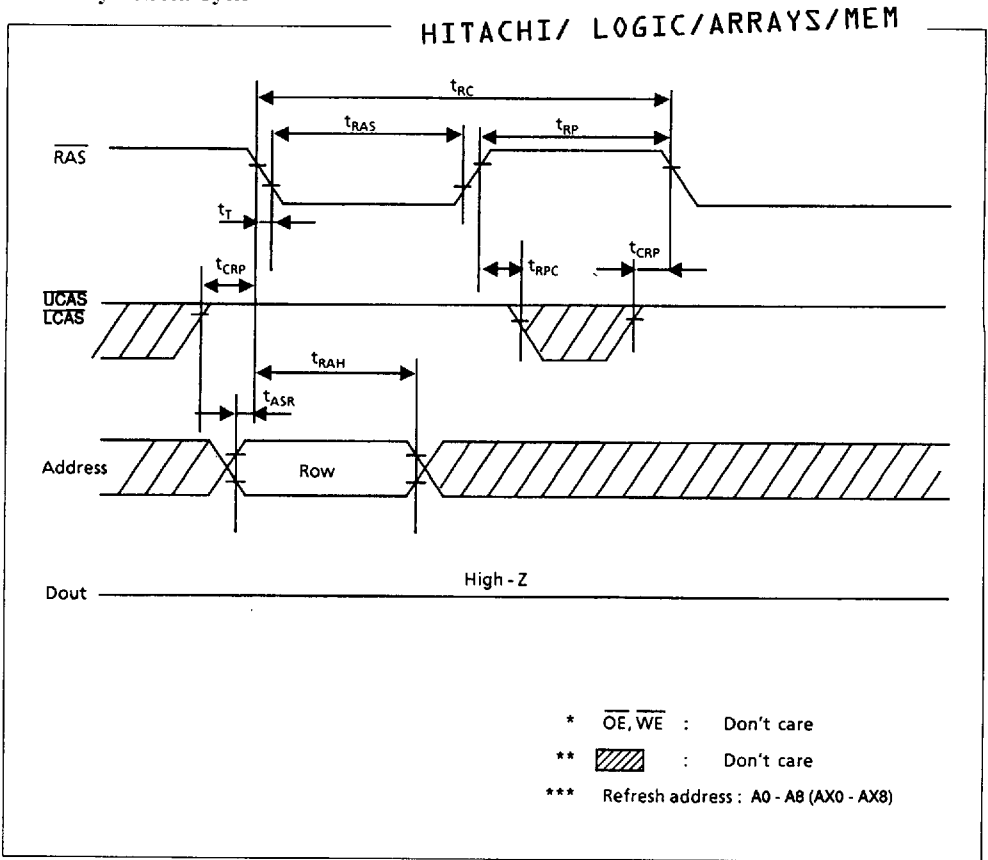
Read-Modify-Write Cycle

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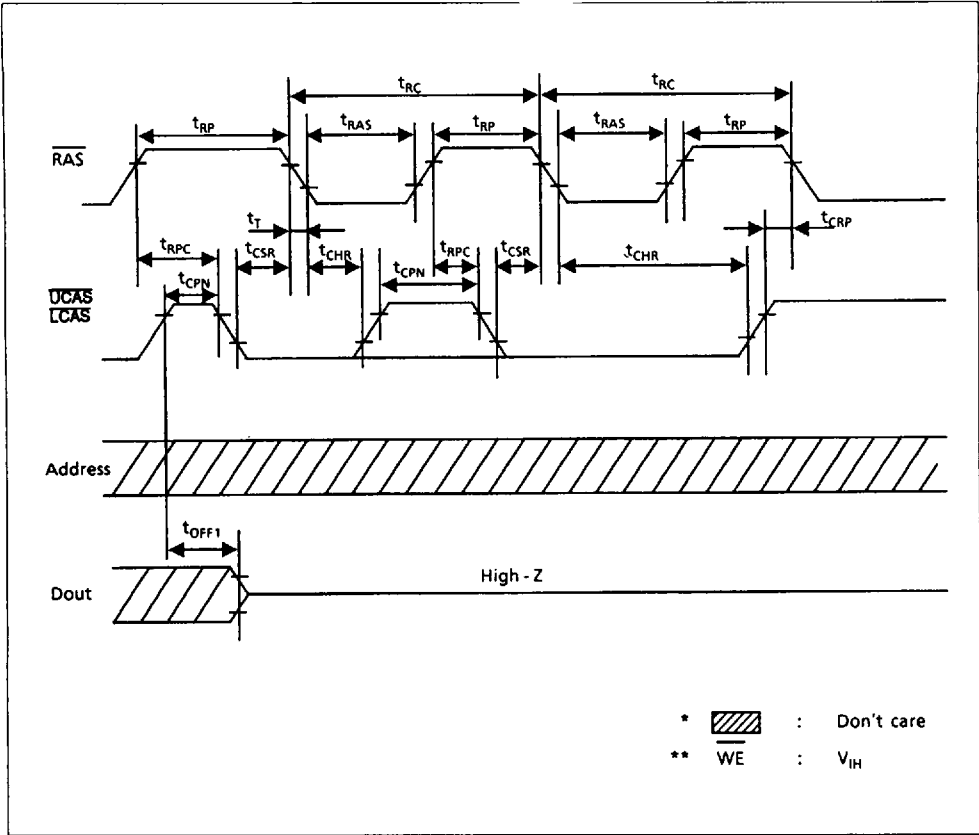
RAS-Only Refresh Cycle



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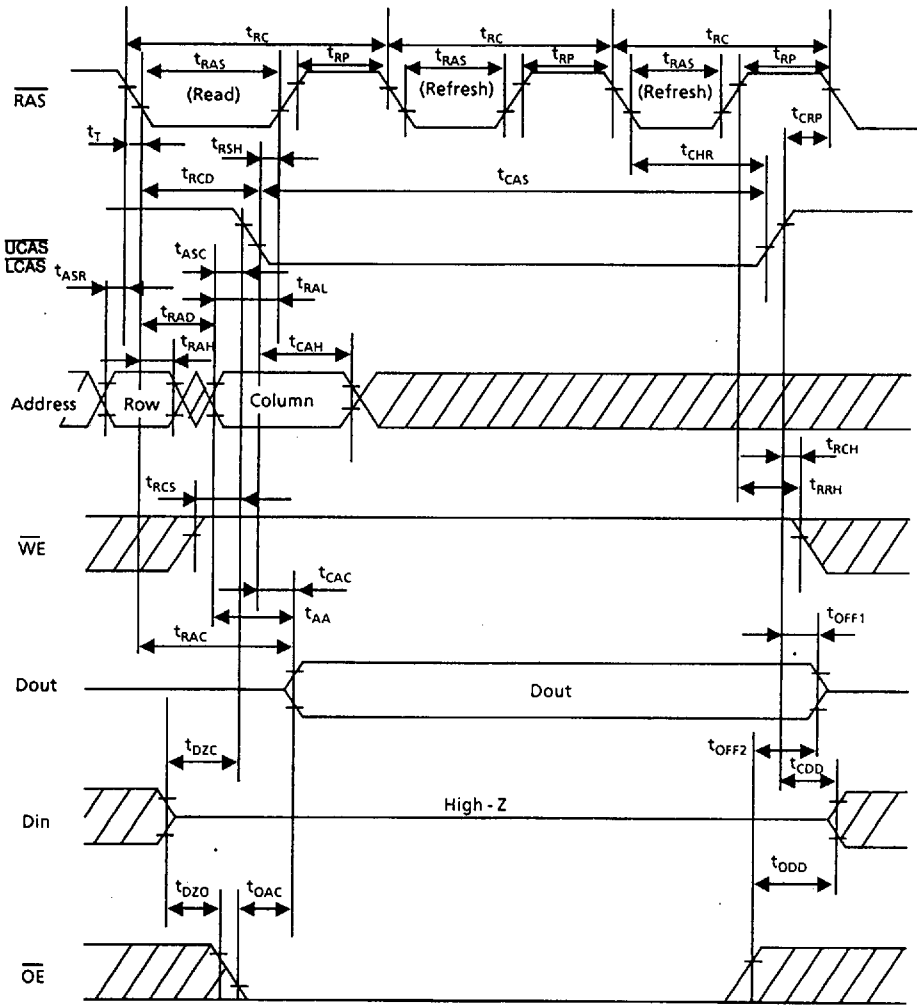
CAS-Before-RAS Refresh Cycle




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Hidden Refresh Cycle

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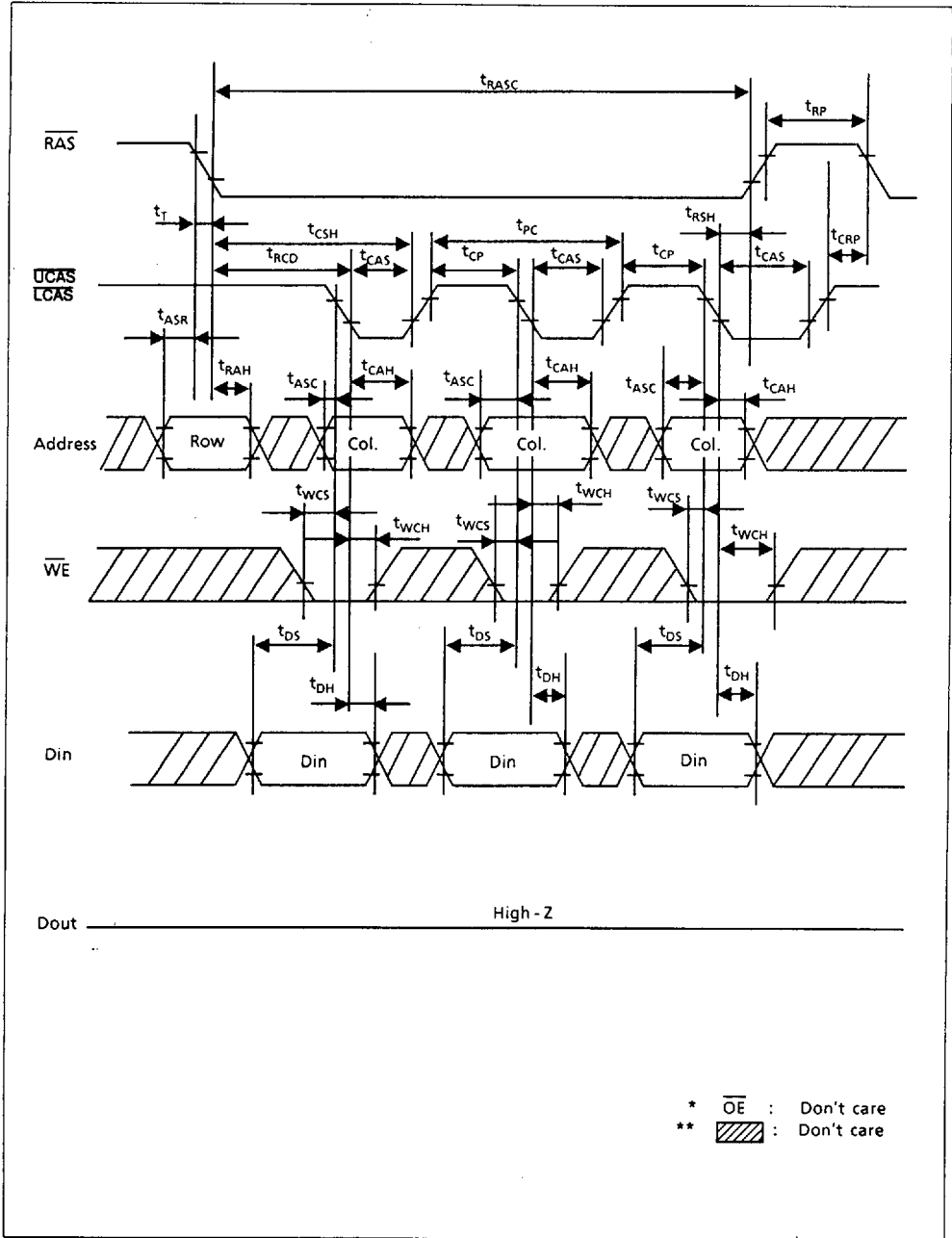


*  : Don't care

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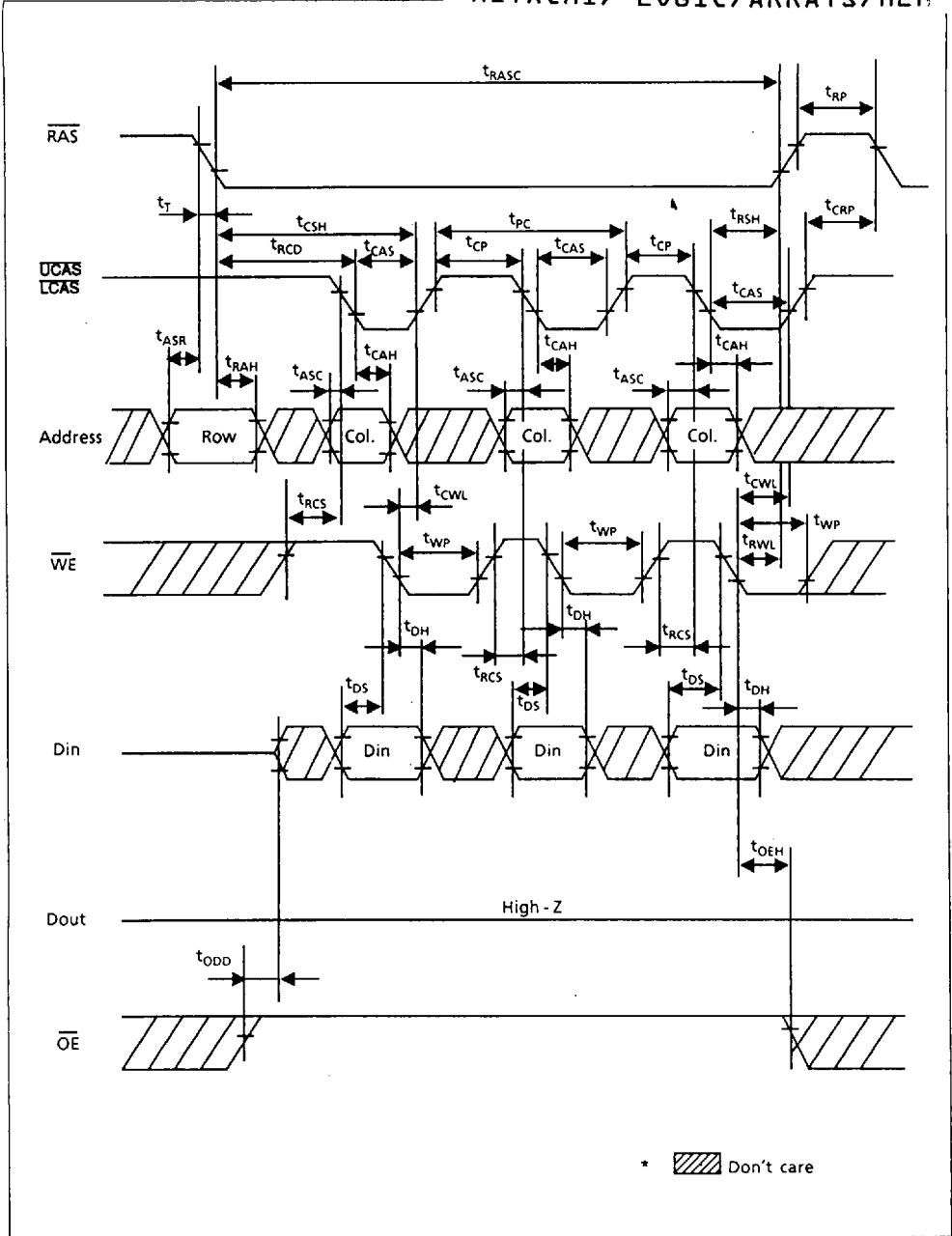
Fast Page Mode Early Write Cycle



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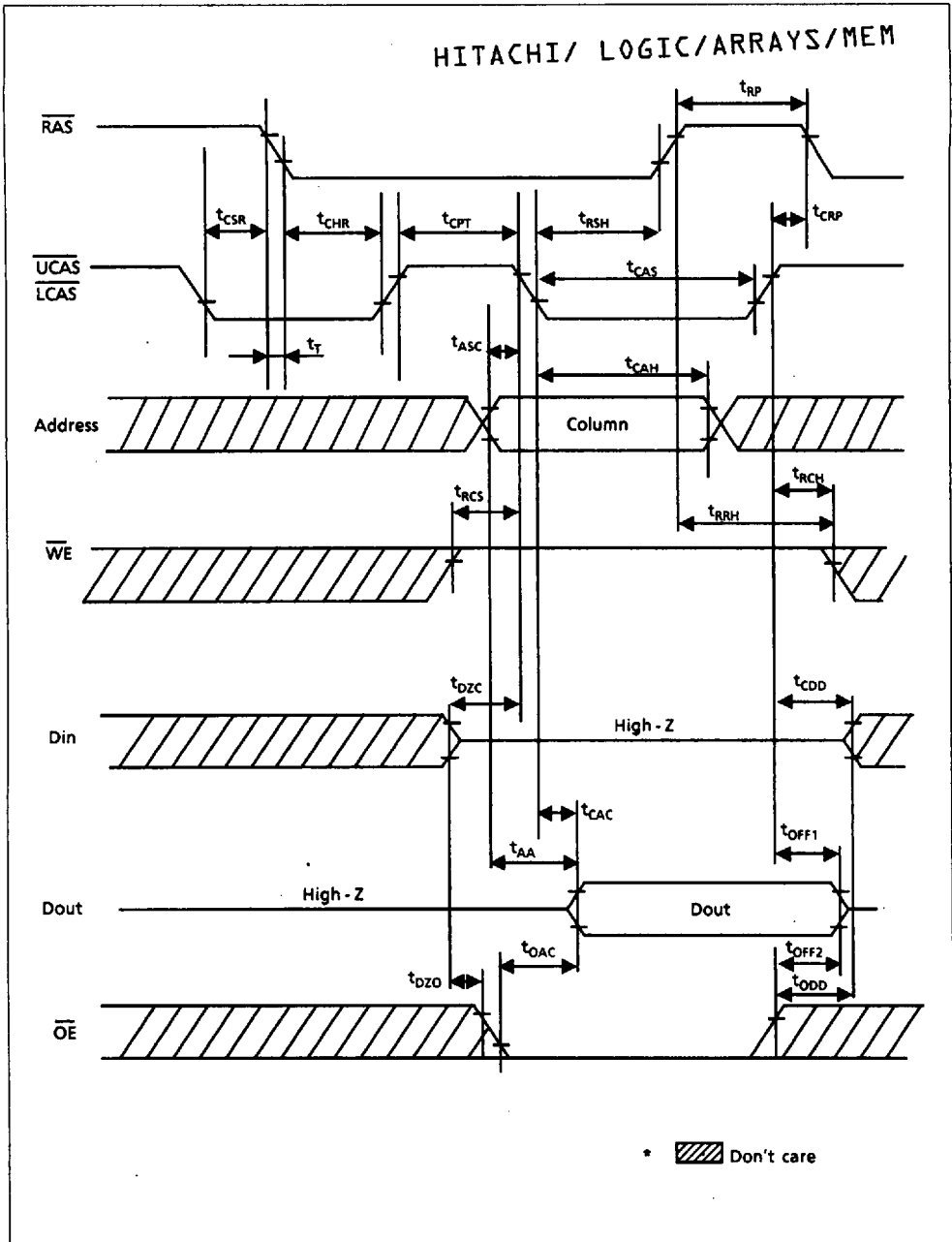
Fast Page Mode Delayed Write Cycle

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CAS-Before-RAS Refresh Counter Check Cycle (Read)



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CAS-Before-RAS Refresh Counter Check Cycle (Write)

