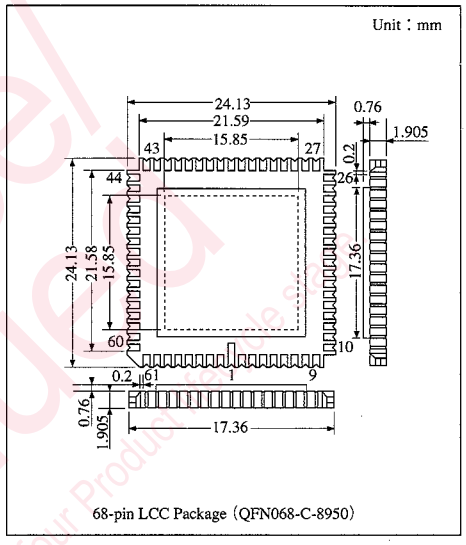
AN8135

High Speed Low Power Consumption Bipolar 10-Bit A/D Convertor

■ Overview

The AN8135 is a 10-bit A/D Convertor for measurement which employs the high frequency bipolar process to realize the low power consumption.

It can operate with single power supply of −5.2V and maximum conversion rate of 100 MSPS, realizing the low error rate.



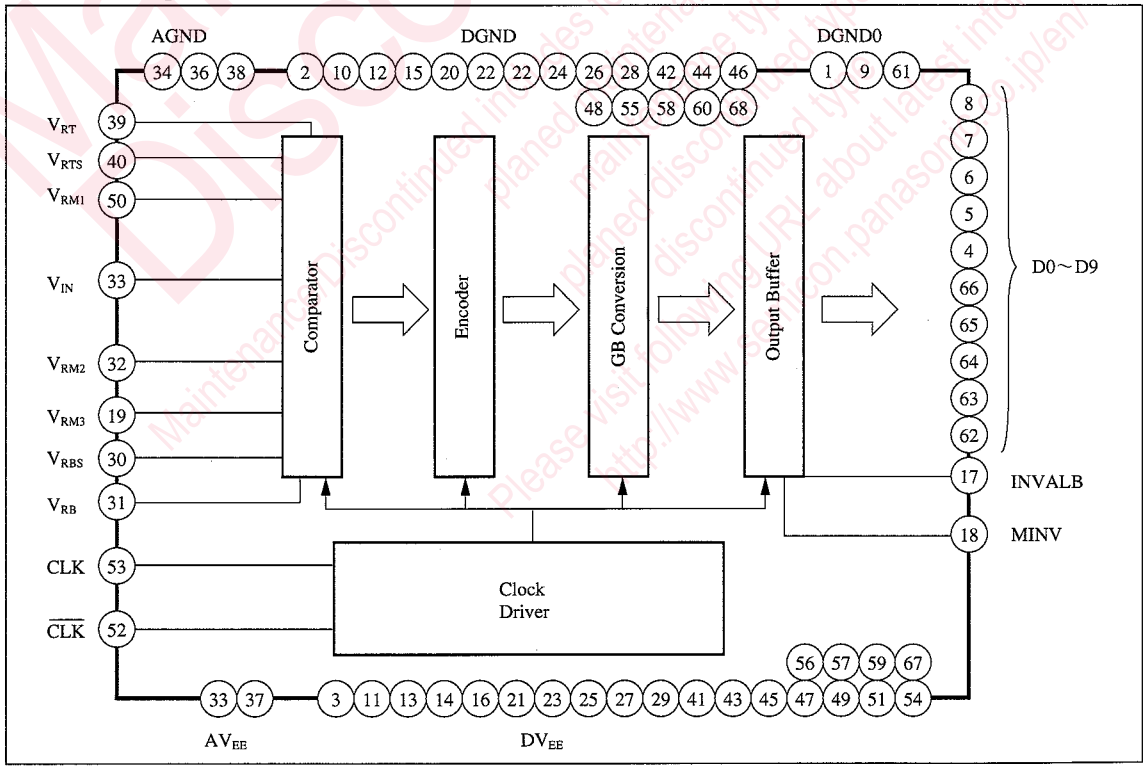
■ Features

- 10-bit resolution
- Super high speed : maximum conversion rate of 100MSPS (min.)
- Low power consumption : 1.8W (typ.)
- Low input capacitance : 10pF
- Input/Output form : ECL level

■ Application Field

- Measuring equipment such as digital oscilloscope
- Image processing

■ Block Diagram



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■ Absolute Maximum Rating (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}	−6.0 to +0.5	V
Analogue input voltage	V_{IN}	V_{EE} to +0.5	V
Digital input voltage	$V_{CLK}/\overline{V_{CLK}}$	V_{EE} to +0.5	V
Digital output current	I_{D0} to I_{D9}	−20	mA
Reference resistive voltage	I_{RT}/I_{RB}	+20/−20	mA
Reference input voltage	V_{RB}/V_{RT}	V_{EE} to +0.5	V
Power dissipation	P_D	1582.2*	mW
Operating ambient temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−55 to +150	℃

* Under Ta=70℃ (With no air and heat emitter)

■ Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	min	typ	max	Unit
Negative supply voltage	V_{EE}	−5.4	−5.2	−5.0	V
Reference voltage	V_{RTS}	—	0	—	V
	V_{RBS}	—	−2.0	—	V
Analogue input voltage	V_{IN}	V_{RBS}	—	V_{RTS}	V
Digital input voltage	V_{IH}	—	−0.9	—	V
	V_{IL}	—	−1.7	—	V
Clock input pulse width *	t_H	—	5	—	ns

* f_{CLK}=100MHz

■ Electrical Characteristics (V_{EE}=5V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	I_{EE}		−400	−350	—	mA
Reference current	I_{RT}	V_{RTS}=0V	—	8	14	mA
	I_{RB}	V_{RBS}=−2.0V	−14	−8	—	mA
Input bias current	I_{IN}	V_{IN}=−1.0V	—	220	350	μA
Clock input current	I_{IH}	V_{CLK}=−1.105V	—	—	20	μA
Digital output voltage	V_{OH}	R_L=100Ω TO V_T=−2.0V	−1.1	—	—	V
	V_{OL}		—	—	−1.6	V
Linearity error	E_L	$V_{RTS}-V_{RBS}$=2.0V	—	—	±2.0	LSB
Differential linearity error	E_D	$V_{RTS}-V_{RBS}$=2.0V	—	—	±0.6	LSB
Maximum coversion rate	F_{CMAX}		100	—	—	MHz
Input dynamic range			—	2	—	V_{P-P}
Equivalent input impedence *1	R_{IN}	V_{IN}=−1V	—	300	—	kΩ
Input capacitance *1	C_{IN}	V_{IN}=−1V	—	10	—	pF
Error rate *1		f_{CLK}=100MHz, f_{IN}=50MHz 12LSB以上	—	—	10^{-12}	tps
Quantization noise *2	SINAD	f_{CLK}=100MHz, f_{IN}=50MHz	50	54	—	dB
		f_{CLK}=100MHz, f_{IN}=50MHz	42	45	—	dB
Input band *1	BW_F	−3dB, V_{IN}=2.0V_{PP}	—	100	—	MHz
Clock duty *1	DTY	f_{CLK}=100MHz	30	50	60	%
Digital output delay *1	τ_d		(6.8)	7	(7.2)	ns

*1 Design reference value but not guaranteed one
*2 Total harmonics distortion included

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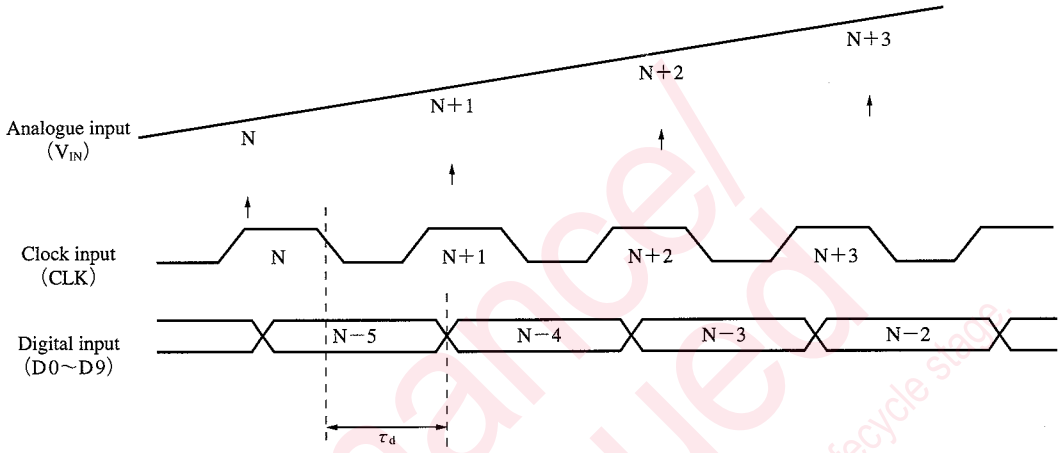
■ Timing Chart



■ Output Code

Step	Input signal	Digital output			
		MINV=L		MINV=H	
		INVALB=L	INVALB=H	INVALB=L	INVALB=H
	2.000VFS 1.9531mV STEP	M L 9876543210	M L 9876543210	M L 9876543210	M L 9876543210
000	−0.0000000	0000000000	1111111111	1000000000	0111111111
001	−0.0019531	0000000001	1111111110	1000000001	0111111110
.	.	.	.	.	.
.	.	.	.	.	.
511	−0.9980469	0111111111	1000000000	1111111111	0000000000
512	−1.0000000	1000000000	0111111111	0000000000	1111111111
.	.	.	.	.	.
.	.	.	.	.	.
1022	−1.9980489	1111111110	0000000001	0111111110	1000000001
1023	−2.0000000	1111111111	0000000000	0111111111	1000000000

Note) The digital output is reversed in half clock after shift from MINV to INVALB.

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A/D and D/A Converters

■ Pin Descriptions

Pin No.	Symbol	Pin name	Standard waveform	Voltage level	Description
35	V_{IN}	Analogue input		−2~0V	It is an input pin of analogue for A/D conversion circuit.
34, 36 38	AGND	Analogue ground		0V	Connect the AGND and DGND with the possible lowest impedance at one point as near as the chip.
33,37	AV_{EE}	Analogue negative power supply pin		−5.2V	It is a power supply pin for analogue circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and AGND.
3, 11 13, 14 16, 21 23, 25 27, 29 41, 43 45, 47 19, 51 54, 56 57, 59 67	DV_{EE}	Digital negative power supply pin		−5.2V	It is a power supply pin for digital circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to this pin between this pin and DGND.
39 40 50 32 19 31 30	V_{RT} V_{RTS} V_{RM1} V_{RM2} V_{RM3} V_{RB} V_{RBS}	Reference voltage high level, Monitor pin for VRT, Reference voltage middle point level, Reference voltage middle point level, Reference voltage middle point level, Reference voltage low level, Minitor pin for VRB		0.03V 0V −0.5V −1.0V −1.5V −2.03V −2.0V	It is used to set the reference voltage for comparator. Normally, V_{RT} is given 0V and V_{RB} is given −2V. Connect tantalum capacitor of several μF and ceramic of 0.1 μF in parallel between each pin and analogue ground. V_{RM1-3} are provided for linearity compensation, which give middle point potential between V_{RTS} and V_{RBS}. However, they are normally opened. V_{RTS} and V_{RBS} are sense pins of V_{RT} and V_{RB} respectively.
2, 10 12, 15 20, 22 24, 26 28, 42 44, 46 48, 55 58, 60 68	DGND	Digital ground		0V	Connect AGND and DGND with the possible lowest impedance at one point as near as possible to the chip.
1, 9, 61	DGND0	Digital ground for output		0V	It is a ground pin for digital output.
53 52	$\overline{CLK}$ CLK	Clock input	Refer to timing chart.	ECL	It is a clock for sampling. For their timing, refer to the timing chart.
8 7 6 5 4 66 65 64 63 62	D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_9	Digital output (LSB) Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output Digital output (MSB)	Refer to timing chart.	ECL	It is an output pin of TTL Level.
18 17	MINV INVALB	MSB reverse pin, Total bit reverse pin		ECL	Setting the MINV pin to "H" level reverses the data output D9. Setting the INVALB pin "H" level reverses the data outputs (D0-D9). The outputs are reversed synchronously with clock.

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