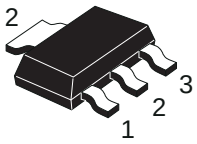
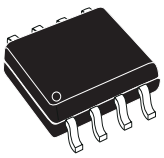
VNL5090N3-E
VNL5090S5-E

OMNIFET III
fully protected low-side driver

Datasheet - production data



SOT-223



SO-8

Features

Type	V_{clamp}	$R_{DS(on)}$	I_D
VNL5090N3-E	41 V	90 mΩ	13 A
VNL5090S5-E			

- Automotive qualified
- Drain current: 13 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output (Root part number 2 only)
- Specially intended for 2 x R10W or 4 x R5W automotive signal lamps

Description

The VNL5090N3-E and VNL5090S5-E are monolithic devices made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit.

Output current limitation protects the devices in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention.Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Table 1. Devices summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	VNL5090N3-E	VNL5090N3TR-E
SO-8	VNL5090S5-E	VNL5090S5TR-E

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1 Block diagrams and pins configurations

Figure 1. VNL5090N3-E block diagram

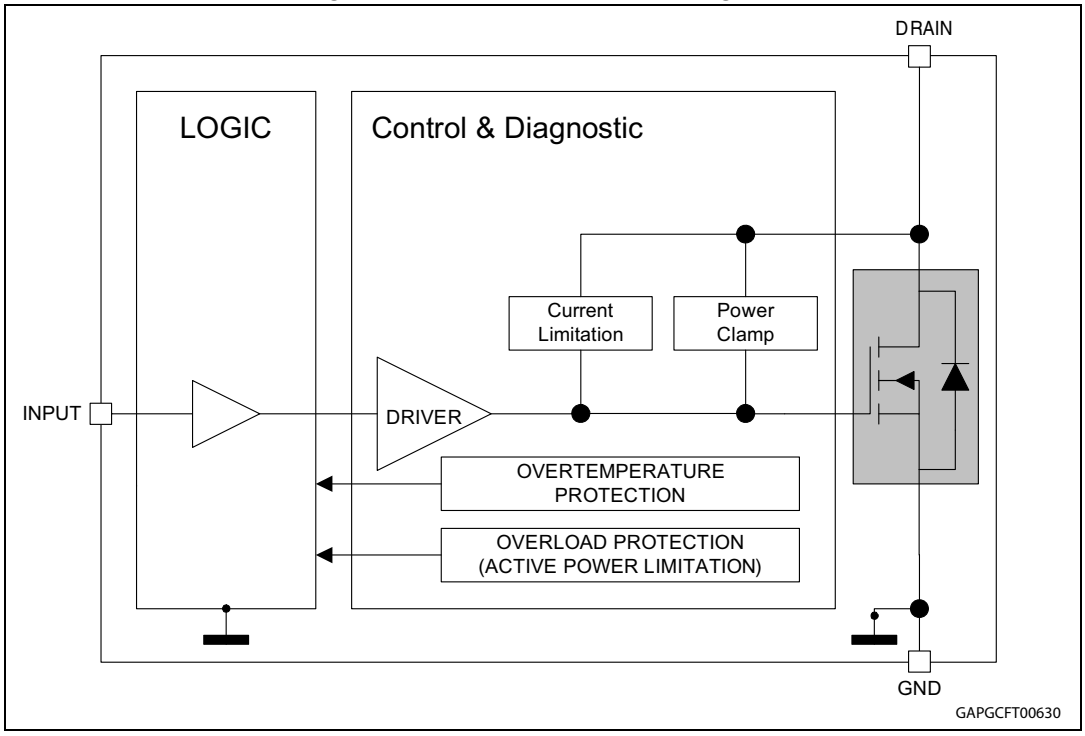


Figure 2. VNL5090S5-E block diagram

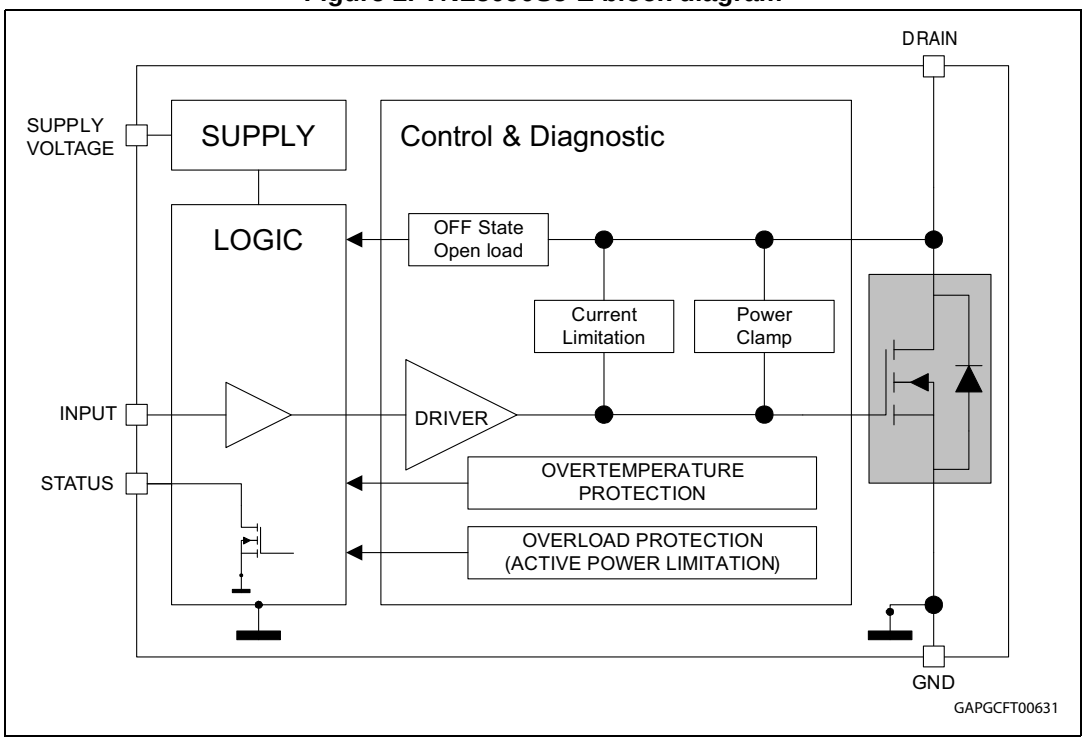


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible; It controls output switch state(1)
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5 V)
STATUS	Open drain digital diagnostic pin(2)

1. Internally connected to V_{supply} in the VNL5090N3-E
2. Valid for VNL5090S5-E only.

Figure 3. VNL5090N3-E current and voltage conventions

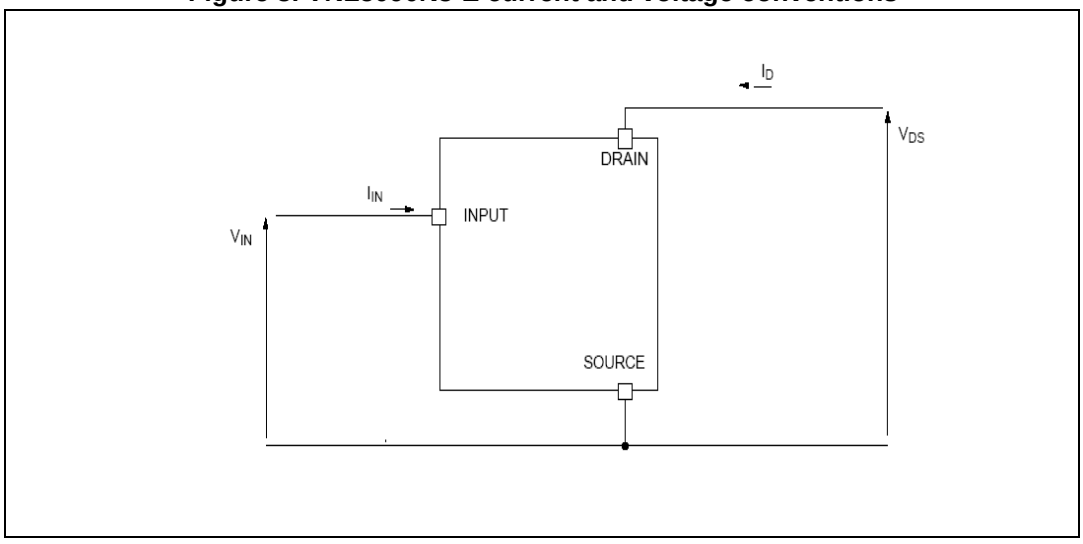


Figure 4. VNL5090S5-E current and voltage conventions

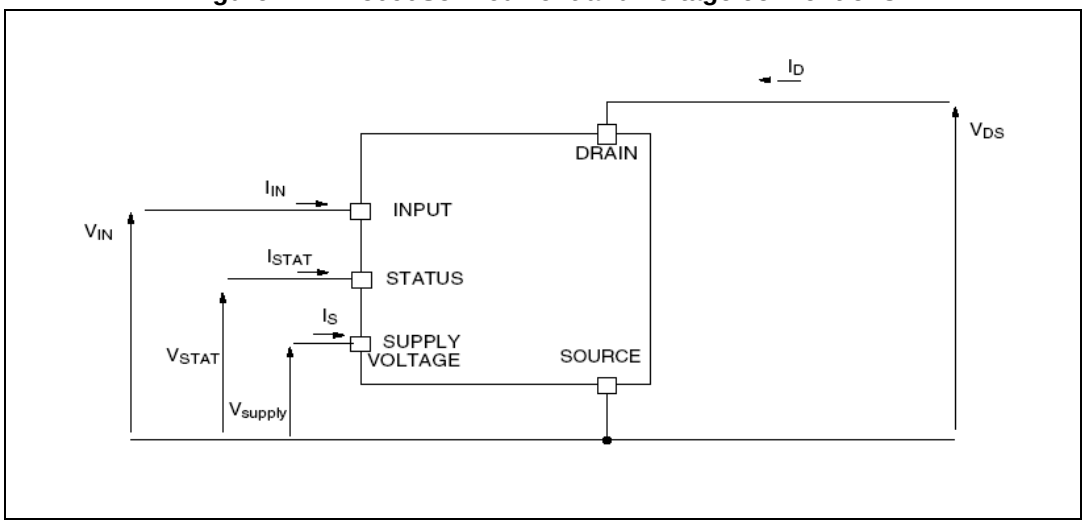
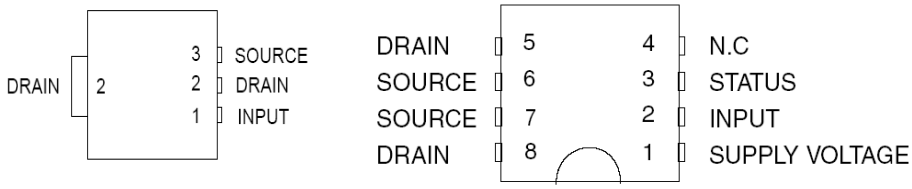


Figure 5. Configuration diagrams (top view)



SOT-223 **SO-8**

Table 3. Suggested connections for unused and N.C. pins

Connection / pin	Status	N.C.	Input
Floating	X(1)	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage (V_{IN} = 0 V)	Internally clamped		V
I_D	DC drain current	Internally limited		A
$-I_D$	Reverse DC drain current	12.5		A
I_S	DC supply current	—	-1 to 10	mA
I_{IN}	DC input current	-1 to 10		mA
I_{STAT}	DC status current	—	-1 to 10	mA
V_{ESD1}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF) – DRAIN – SUPPLY, INPUT, STATUS	 5000 4000		 V V
V_{ESD2}	Electrostatic discharge on output pin only (R = 330 Ω, C = 150 pF)	2000		V
T_j	Junction operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C
E_{AS}	Single pulse avalanche energy (L = 1.1 mH, T_j = 150°C, R_L = 0, I_{OUT} = I_{limL})	50		mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value		Unit
		SOT-223	SO-8	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	147(1)	102	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins

2.3 Electrical characteristics

Values specified in this section are for V_{supply} = V_{IN} = 4.5 V to 5.5 V, -40°C < T_j < 150°C, unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{supply}	Operating supply voltage		3.5	5	5.5	V
R_{ON}	ON-state resistance	I_D = 1.6 A; T_j = 25°C; V_{supply} = V_{IN} = 5 V			90	mΩ
		I_D = 1.6 A; T_j = 150°C; V_{supply} = V_{IN} = 5 V			180	
		I_D = 1.6 A; T_j = 150°C; V_{supply} = V_{IN} = 4.5 V(1)			190	
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 1.6 A	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
I_{DSS}	OFF-state output current	V_{IN} = 0 V; V_{DS} = 13 V; T_j = 25°C	0		3	µA
		V_{IN} = 0 V; V_{DS} = 13 V; T_j = 125°C	0		5	

1. Valid only for VNL5090N3-E.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	I_D = 1.6 A; V_{IN} = 0 V	—	0.8	—	V

Table 8. Input section(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	ON-state: V_{supply} = V_{IN} = 5 V; V_{DS} = 0 V		30	65	µA
V_{ICL}	Input clamp voltage	I_S = 1 mA	5.5		7	V
		I_S = -1 mA		-0.7		
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	1		3.5	V

1. Valid for VNL5090N3-E option (input and supply pins connected together)

Table 9. Status pin(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, V_{STAT} = 5 V			10	µA

Table 9. Status pin(1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{STAT}	Status pin input capacitance	Normal operation, V_{STAT} = 5 V			100	pF
V_{STCL}	Status clamp voltage	I_{STAT} = 1 mA	5.5		7	V
		I_{STAT} = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 10. Logic input(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.13			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 11. Openload detection(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Openload OFF-state voltage detection threshold	V_{IN} = 0 V	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in openload condition	I_{OUT} = 0 A	45	425	1100	µs

1. Valid for VNL5090S5-E option

Table 12. Supply section(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	OFF-state; T_j = 25°C; V_{IN} = V_{DRAIN} = 0 V;		10	25	µA
		ON-state; V_{IN} = 5 V; V_{DS} = 0 V		25	65	
V_{SCL}	Supply clamp voltage	I_{SCL} = 1 mA	5.5		7	V
		I_{SCL} = -1 mA		-0.7		

1. Valid for VNL5090S5-E option

Table 13. Switching characteristics(1)

Symbol	Parameter	Test conditions	SOT-223(2)			SO-8			Unit
			Min.	Typ.	Max	Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on delay time	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	8	—	—	8	—	µs
$t_{d(OFF)}$	Turn-off delay time	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	3.4	—	—	18	—	µs
t_r	Rise time	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	10	—	—	10	—	µs
t_f	Fall time	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	2.7	—	—	10	—	µs
W_{ON}	Switching energy losses at turn-on	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	57	—	—	57	—	µJ
W_{OFF}	Switching energy losses at turn-off	R_L = 8.2 Ω, V_{CC} = 13 V(3)	—	14	—	—	55	—	µJ

1. See *Figure 7: VNL5090N3-E application schematic* and *Figure 8: VNL5090S5-E application schematic*
2. 3.5 V ≤ V_{supply} = V_{IN} ≤ 5.5 V
3. See *Figure 6: Switching characteristics*

Table 14. Protection and diagnostics

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{DS} = 13 V; V_{supply} = V_{IN} = 5 V	13	18	25	A
I_{limL}	Short-circuit current during thermal cycling	V_{DS} = 13 V; $T_R < T_j < T_{TSD}$; V_{supply} = V_{IN} = 5 V		8		A
t_{dlimL}	Step response current limit	V_{DS} = 13 V; V_{input} = 5 V		44		µs
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R(2)	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS} (3)	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C

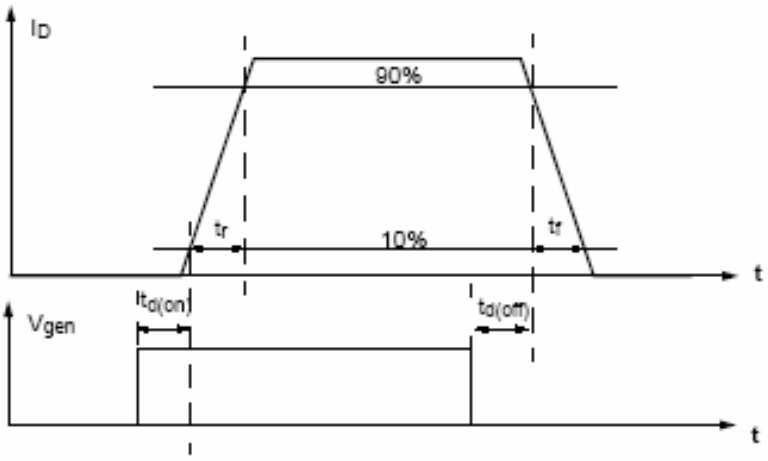
1. V_{supply} = V_{input} in VNL5090N3-E version.
2. Valid for VNL5090S5-E option.

Table 15. Truth table(1)

Conditions	INPUT	DRAIN	STATUS
Normal operation	L H	H L	H H
Current limitation	L H	H X	H H
Overtemperature	L H	H H	H L
Undervoltage	L H	H H	X X
Output voltage < V_{OL}	L H	L L	L H

1. Valid for VNL5090S5-E option

Figure 6. Switching characteristics



3 Application information

Figure 7. VNL5090N3-E application schematic

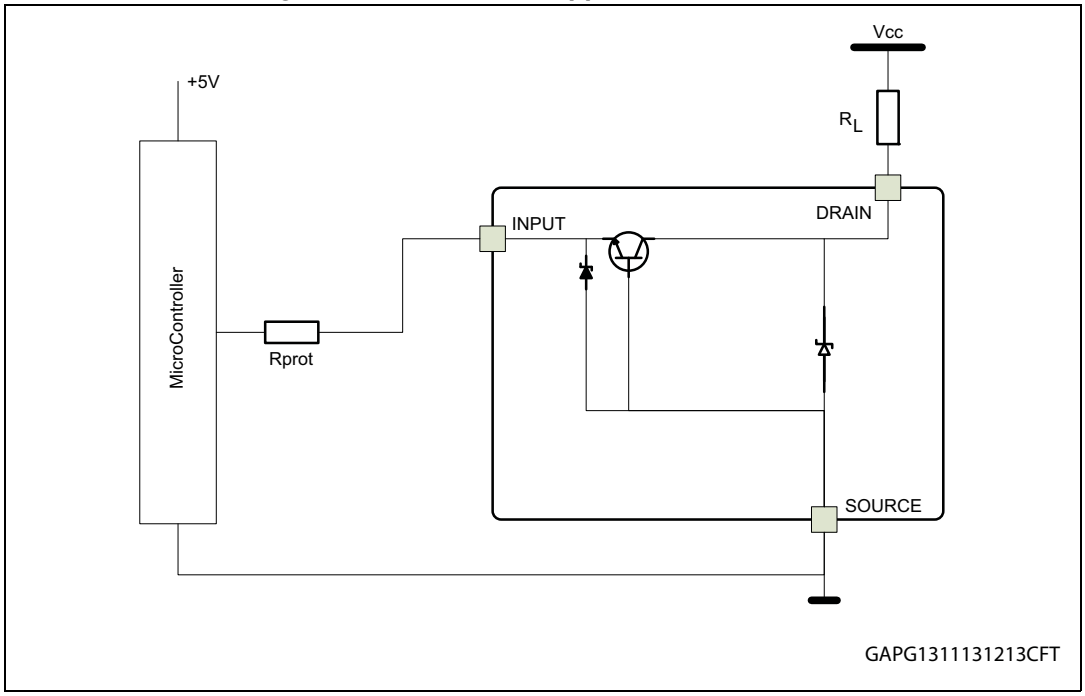
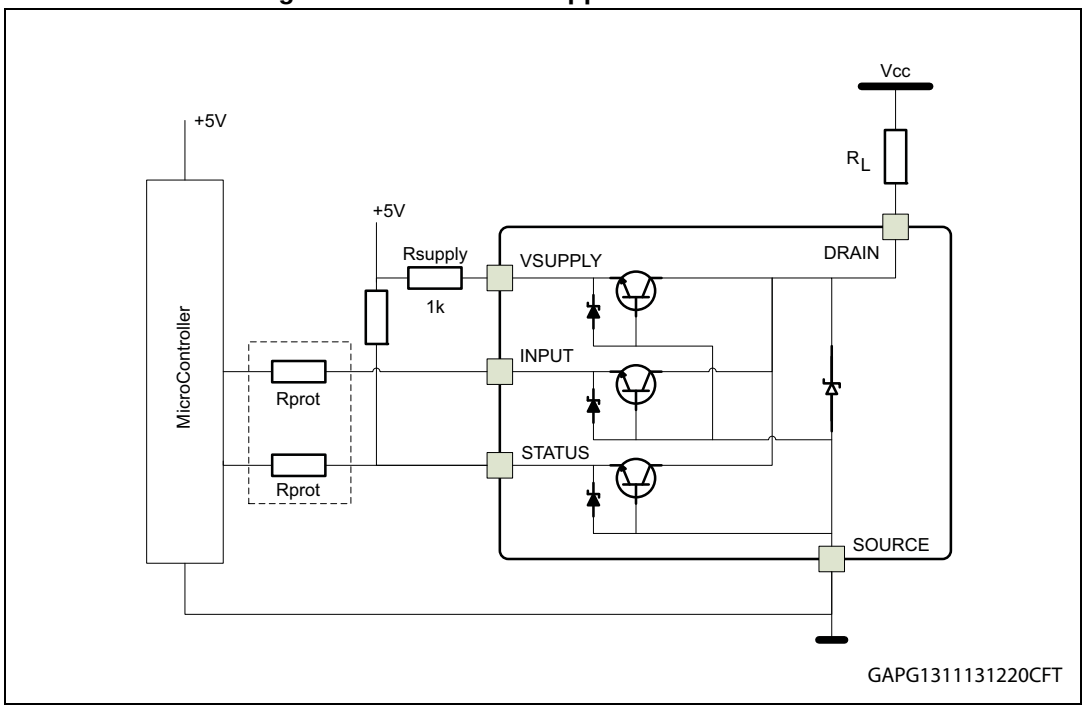


Figure 8. VNL5090S5-E application schematic



3.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up[(a)]. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

Let:

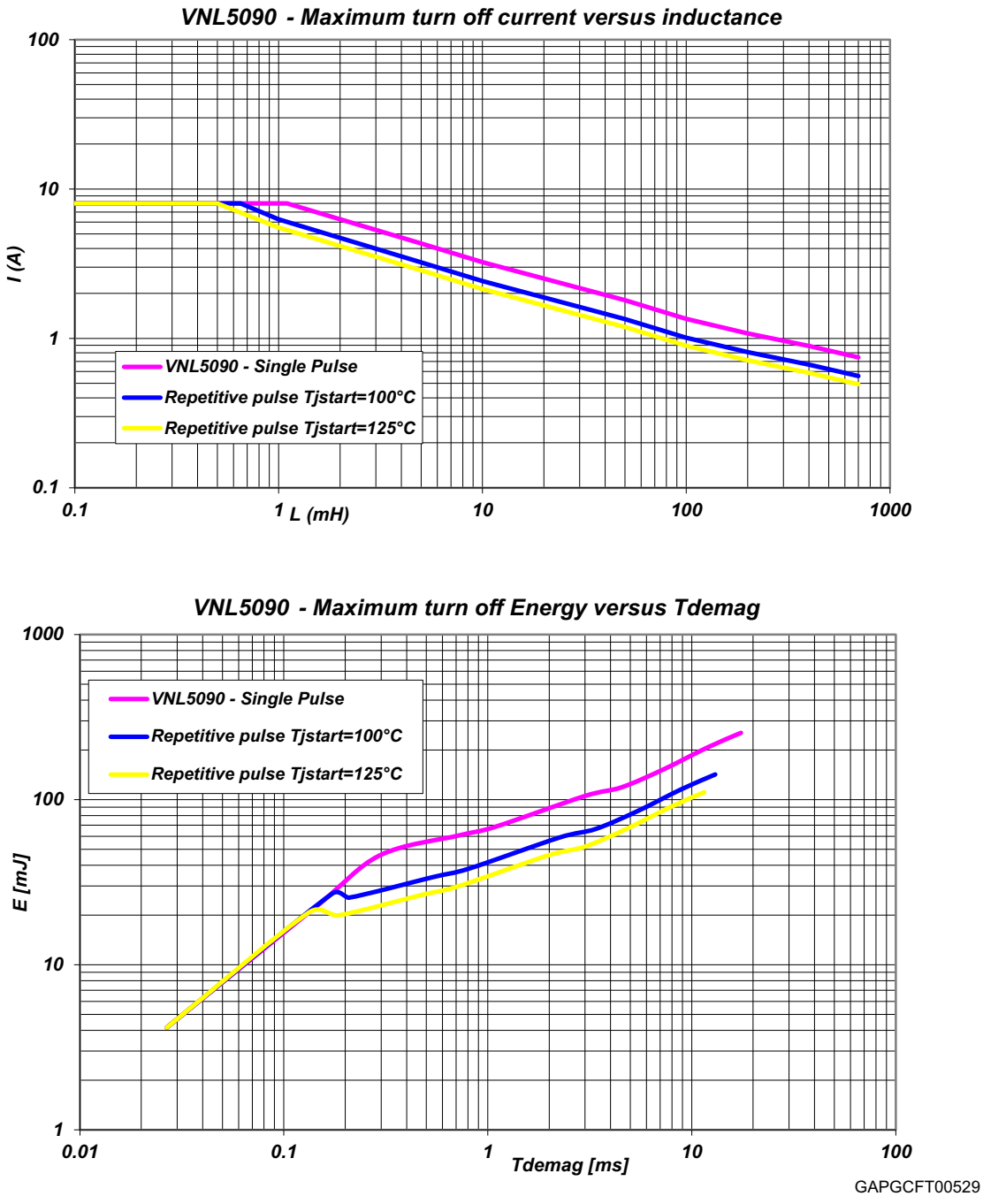
- $I_{latchup} \geq 20$ mA
- $V_{OH\mu C} \geq 4.5$ V
- $35\ \Omega \leq R_{prot} \leq 100\ K\Omega$

Then, the recommended value is $R_{prot} = 1\ K\Omega$

Figure 9 shows the turn-off current drawn during the demagnetization.

a. In case of negative transient on the drain pin.

Figure 9. Maximum demagnetization energy (V_{CC} = 16 V)

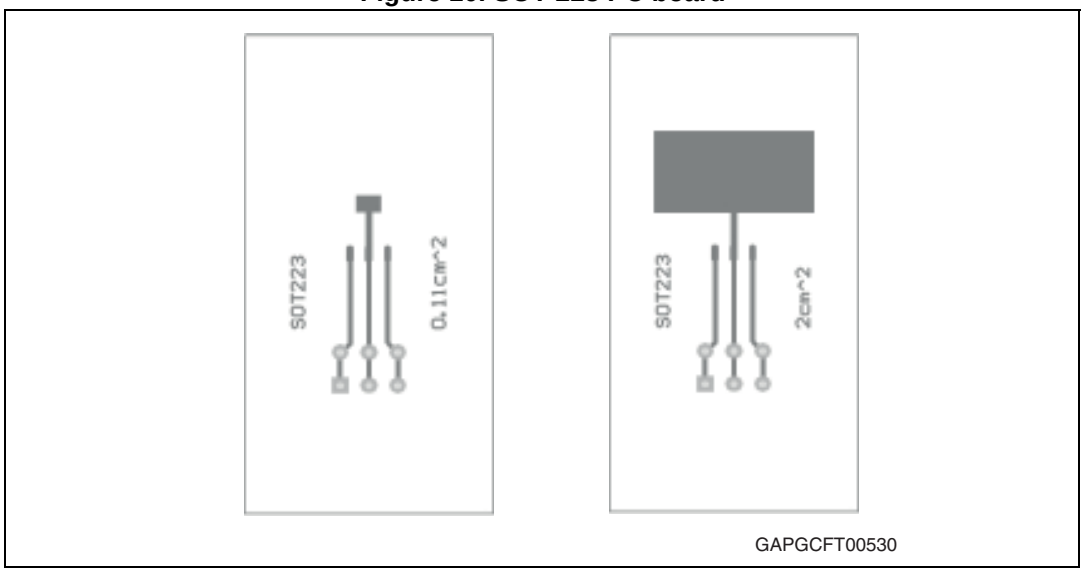


1. The voltage supply is V_{CC} = 13.5 V.

4 Package and PC board thermal data

4.1 SOT-223 thermal data

Figure 10. SOT-223 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 30 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, copper areas: from minimum pad lay-out to 0.8 cm^2).

Figure 11. SOT-223 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

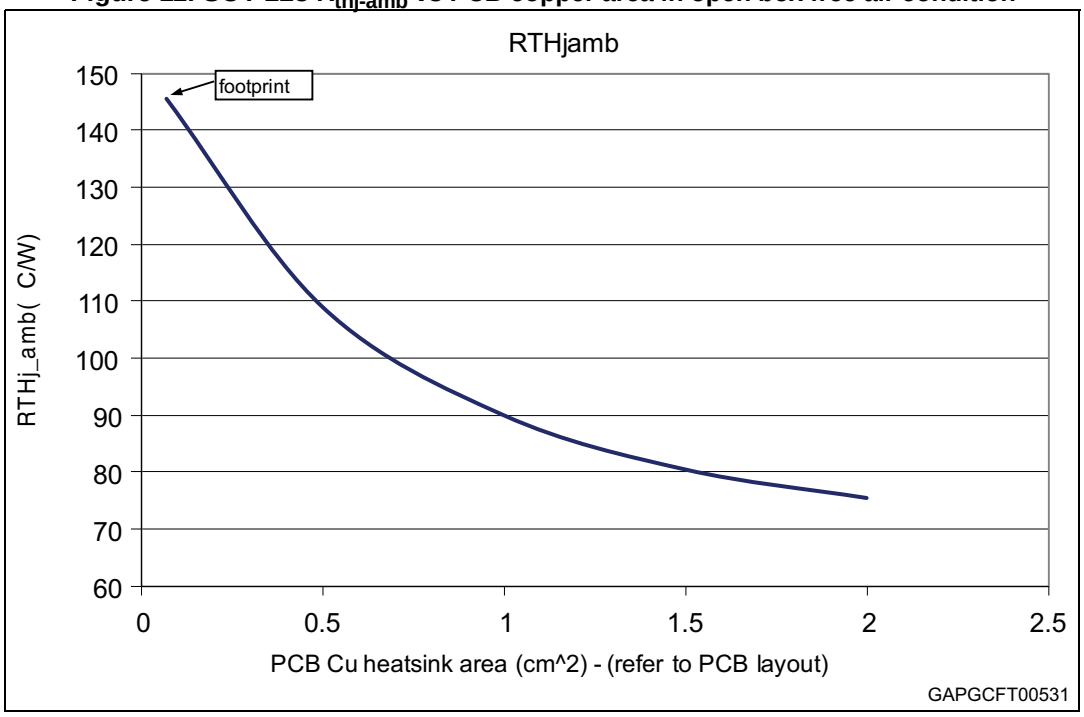
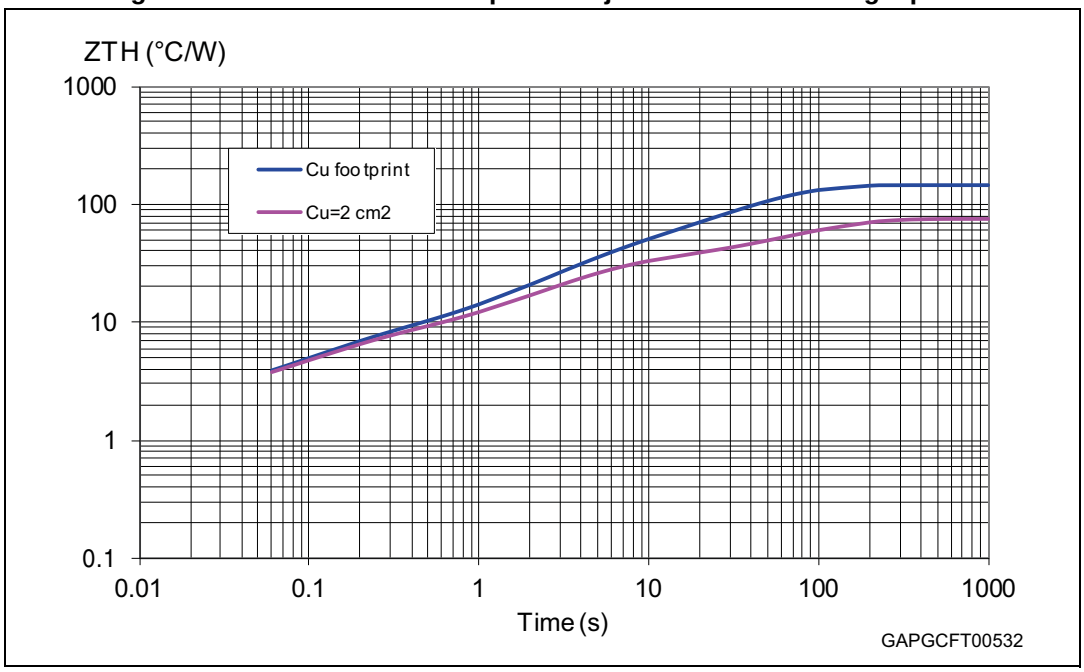


Figure 12. SOT-223 thermal impedance junction ambient single pulse

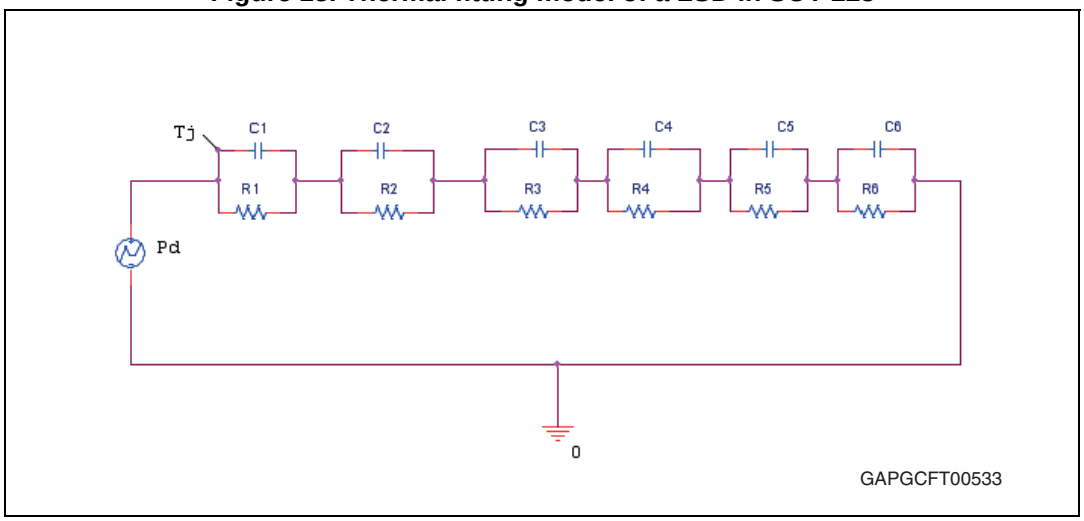


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 13. Thermal fitting model of a LSD in SOT-223



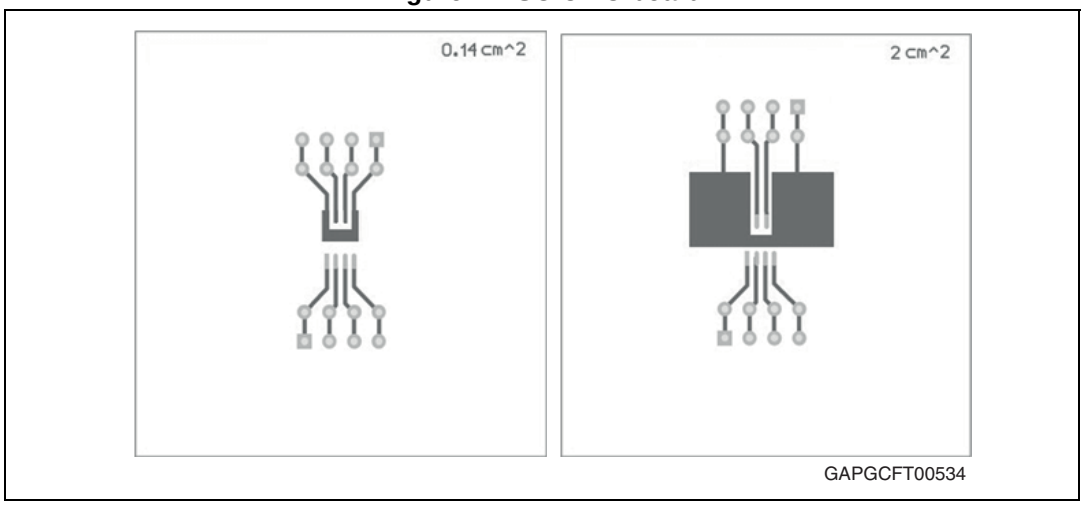
Note: The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SOT-223 thermal parameters

Area/island (cm^2)	Footprint	2
R1 (°C/W)	0.8	
R2 (°C/W)	1	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	115	45
C1 (W.s/°C)	0.00004	
C2 (W.s/°C)	0.0003	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.16	
C5 (W.s/°C)	1000	
C6 (W.s/°C)	0.4	2

4.2 SO-8 thermal data

Figure 14. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm (front and back side), Copper areas: from minimum pad lay-out to 2 cm^2).

Figure 15. SO-8 $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

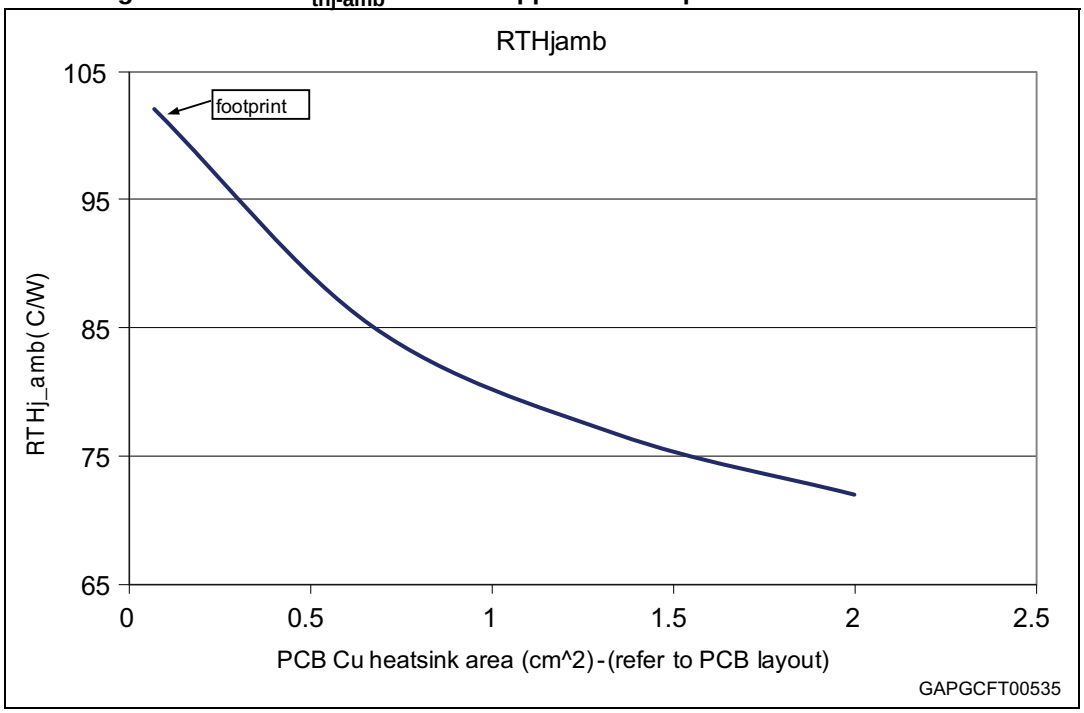
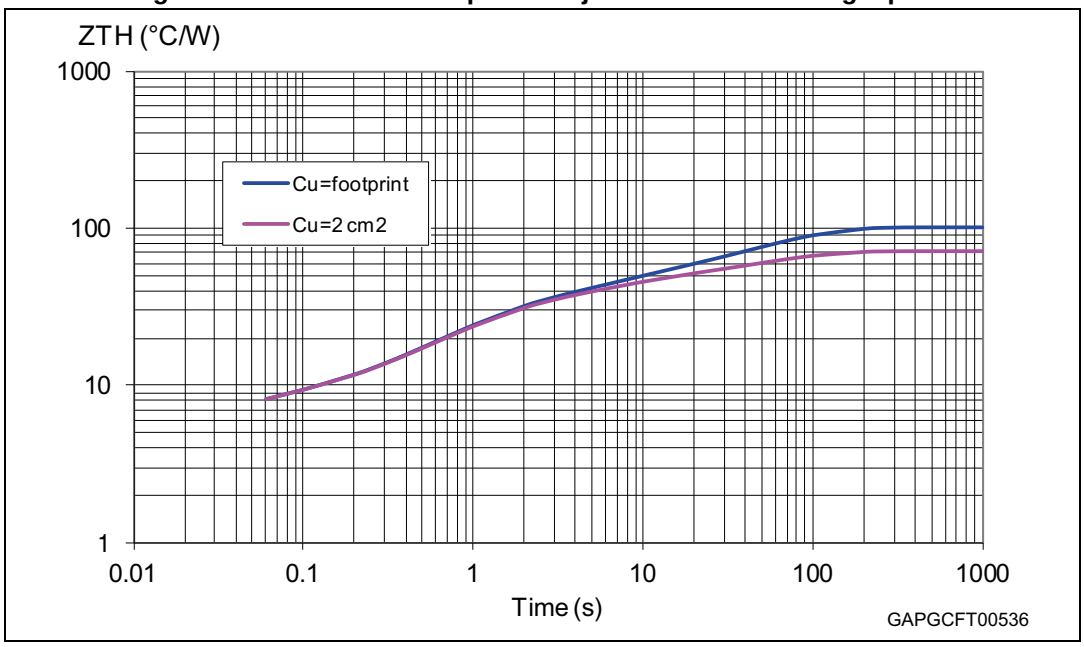


Figure 16. SO-8 thermal impedance junction ambient single pulse

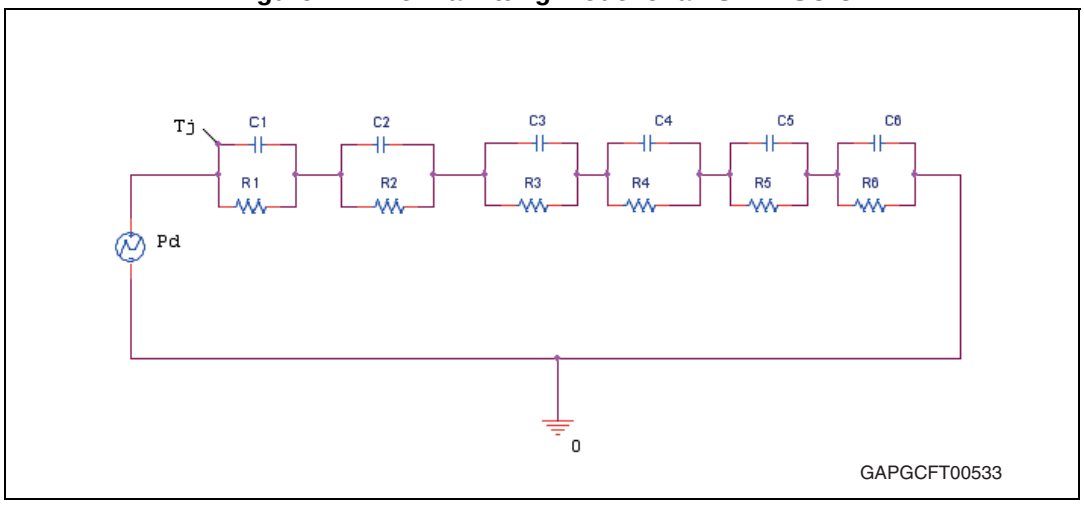


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 17. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. SO-8 thermal parameters

Area/island (cm^2)	Footprint	2
R1 (°C/W)	0.8	
R2 (°C/W)	2.7	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00005	
C2 (W.s/°C)	0.001	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SOT-223 mechanical data

Figure 18. SOT-223 package dimensions

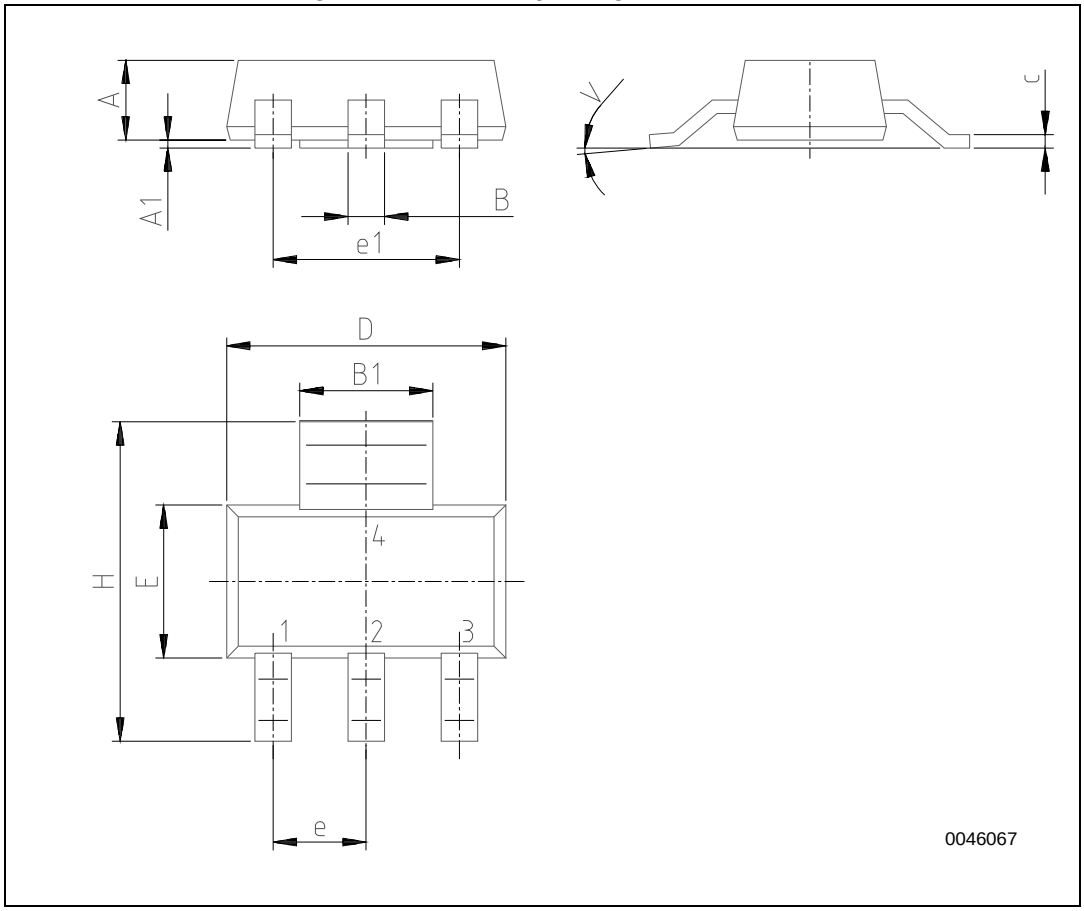


Table 18. SOT-223 mechanical data

DIM.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10 (max)					
A1	0.02		0.1	0.0008		0.004

5.3 SO-8 mechanical data

Figure 19. SO-8 package dimensions

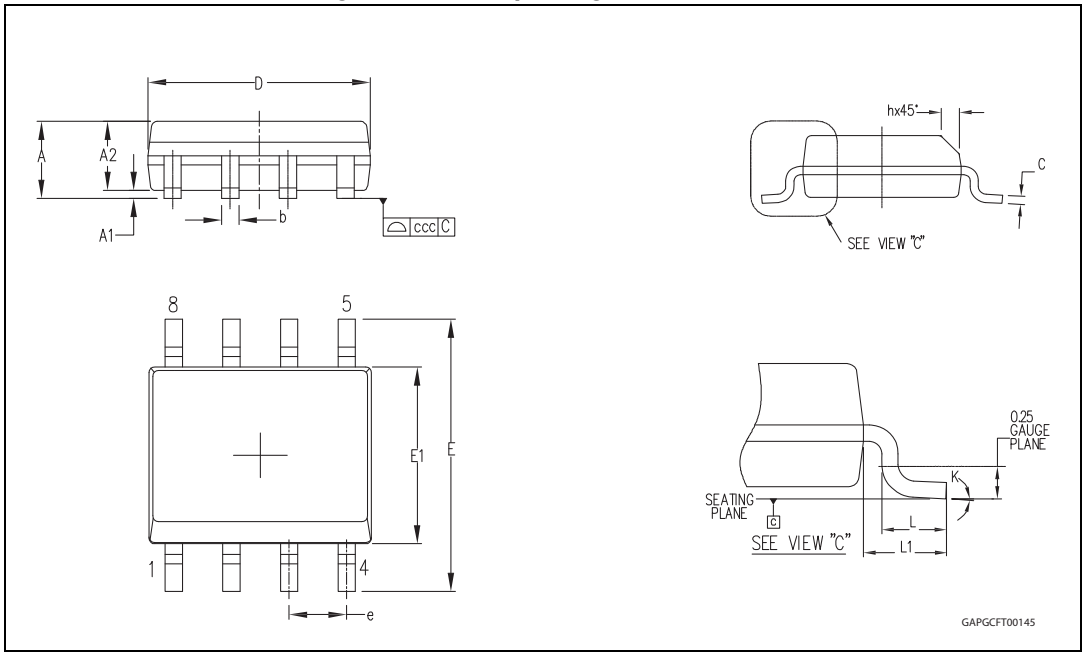


Table 19. SO-8 mechanical data

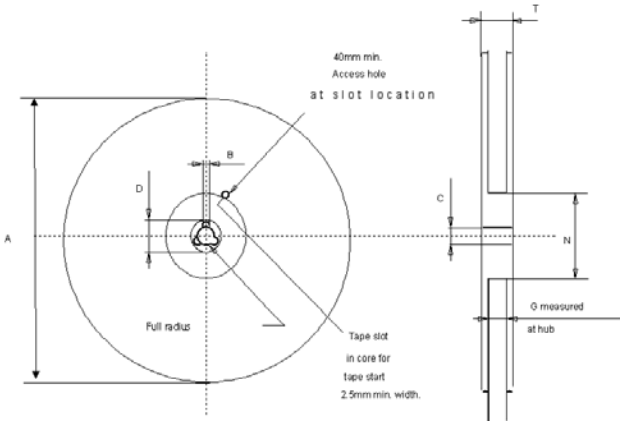
Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.4 SOT-223 packing information

The devices can be packed in tube or tape and reel shipments (see the *Table 1: Devices summary on page 1*).

Figure 20. SOT-223 tape and reel shipment (suffix “TR”)



Reel dimensions

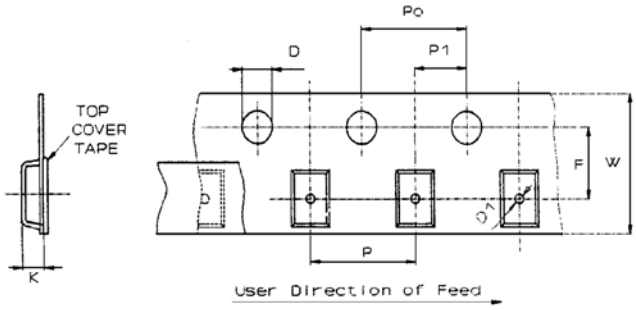
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

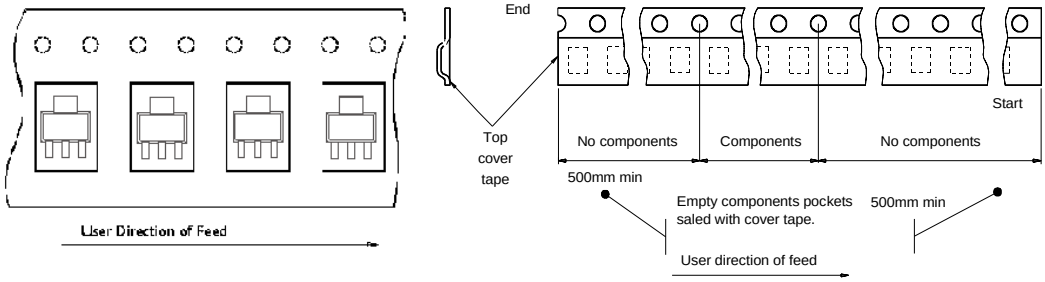
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

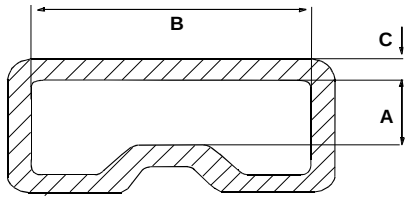
All dimensions are in mm.





5.5 SO-8 packing information

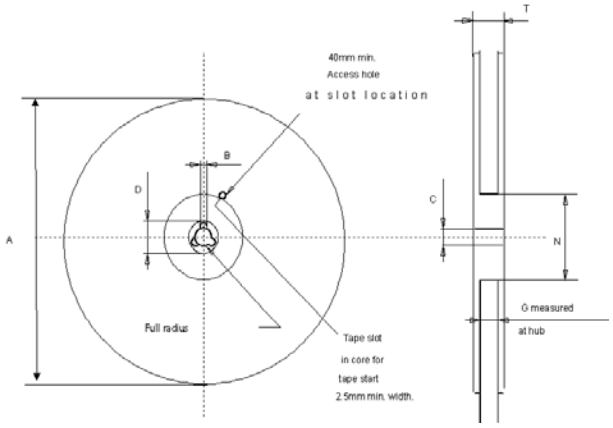
Figure 21. SO-8 tube shipment (no suffix)



Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 22. SO-8 tape and reel shipment (suffix "TR")



Reel dimensions

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

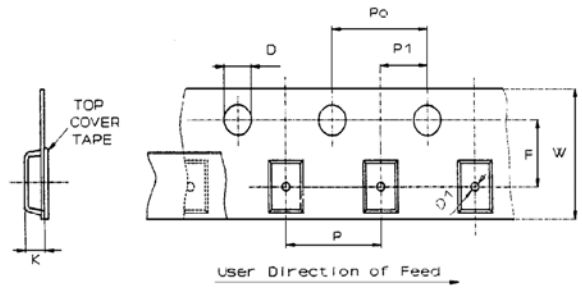
All dimensions are in mm.

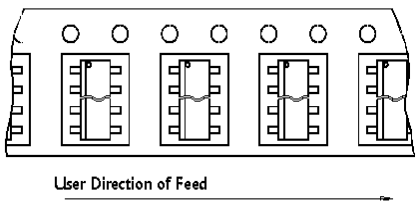
Tape dimensions

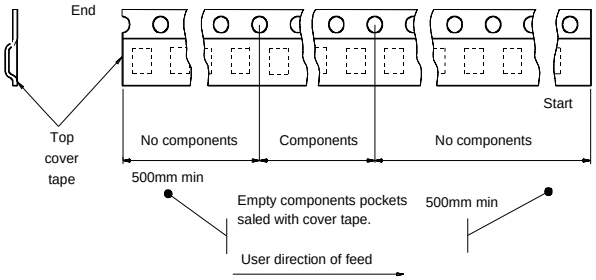
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (+ 0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	5.5
Compartment depth	**K (max)**	4.5
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 20. Document revision history

Date	Revision	Changes
15-Dec-2011	1	Initial release.
20-Jan-2012	2	*Table 4: Absolute maximum ratings*: – $-I_D$: updated value
18-Apr-2012	3	Updated *Features* list
10-Aug-2012	4	Updated *Table 13: Switching characteristics*
18-Sep-2013	5	Updated disclaimer.
13-Nov-2013	6	Updated *Features* list *Table 8: Input section*: – I_{ISS}: updated maximum value *Table 12: Supply section*: – I_{IS}: updated maximum value Updated *Figure 7: VNL5090N3-E application schematic* and *Figure 8: VNL5090S5-E application schematic* Updated *Section 3.1: MCU I/O protection*

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