SCG4503 Synchronous Clock Generator

PLL

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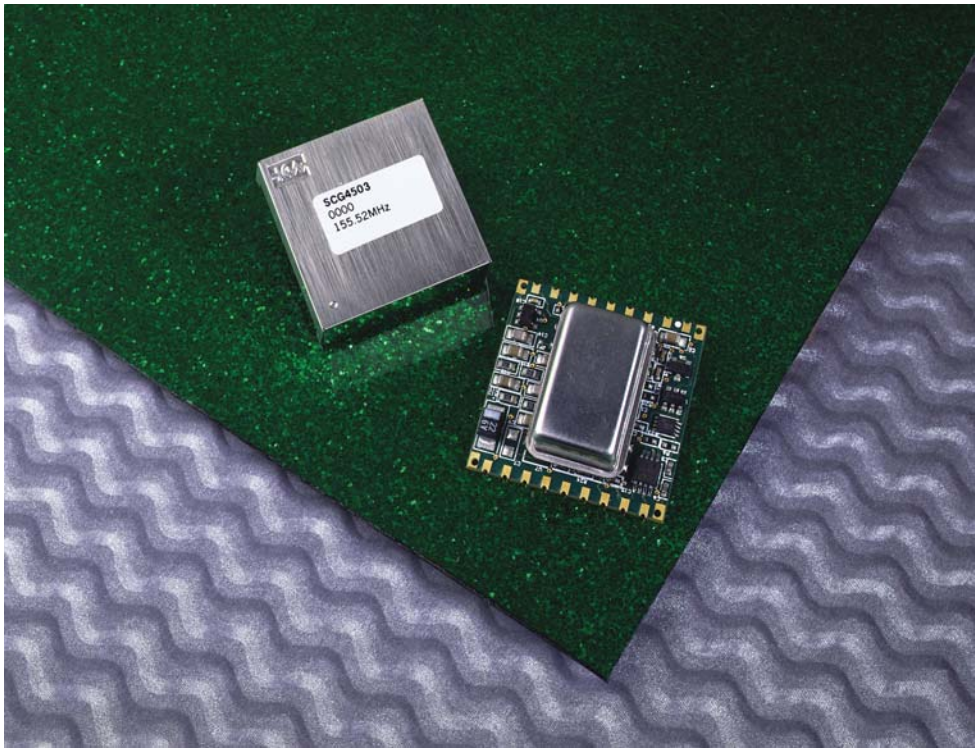

Features

- 27 - 64 Hz Jitter Bandwidth
- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- LVPECL Outputs with Disable Function
- Dual Input References
- LOR & LOL combined alarm output
- Force Free Run Function
- Automatic Free Run operation on loss of both References A & B
- Input Duty Cycle Tolerant
- 3.3V dc Power Supply
- Small Size: 1 Square Inch

Bulletin	**SG082**
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Revision	**00**
Date	**17 JUNE 05**
Issued By	**MBatts**

General Description

The SCG4503 is a mixed-signal phase locked loop generating LVPECL outputs from an intrinsically low jitter, voltage controlled, crystal oscillator. The LVPECL outputs may be disabled.

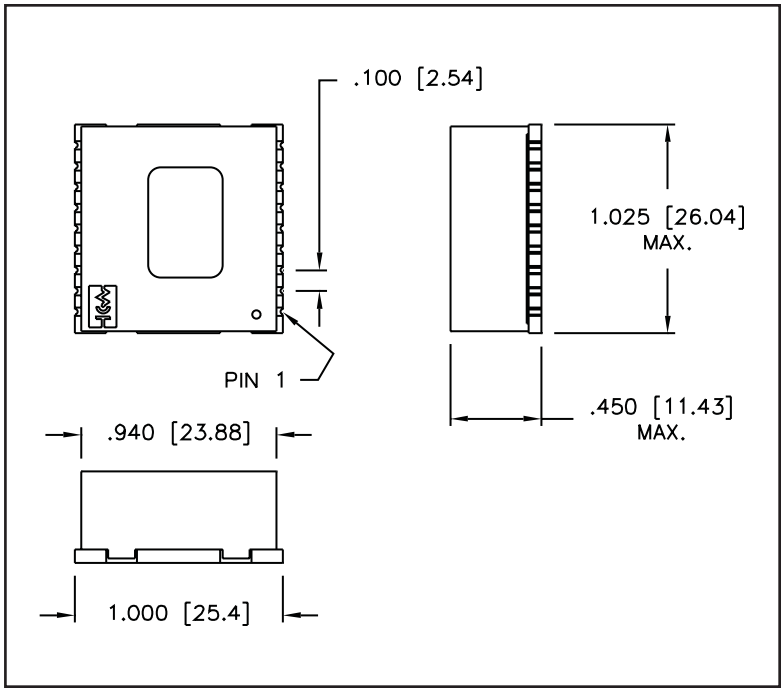
The SCG4503 can lock to one of two external references, which is selectable using the SEL_{AB} input select pin. The unit has a fast acquisition time of about 1.5 seconds and it is tolerant of different reference duty cycles.

The SCG4503 includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 ppm. Additionally the Free Run mode may be entered manually.

The package dimensions are 1" x 1.025" x .45" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloys, 180°C surface mount reflow processes.

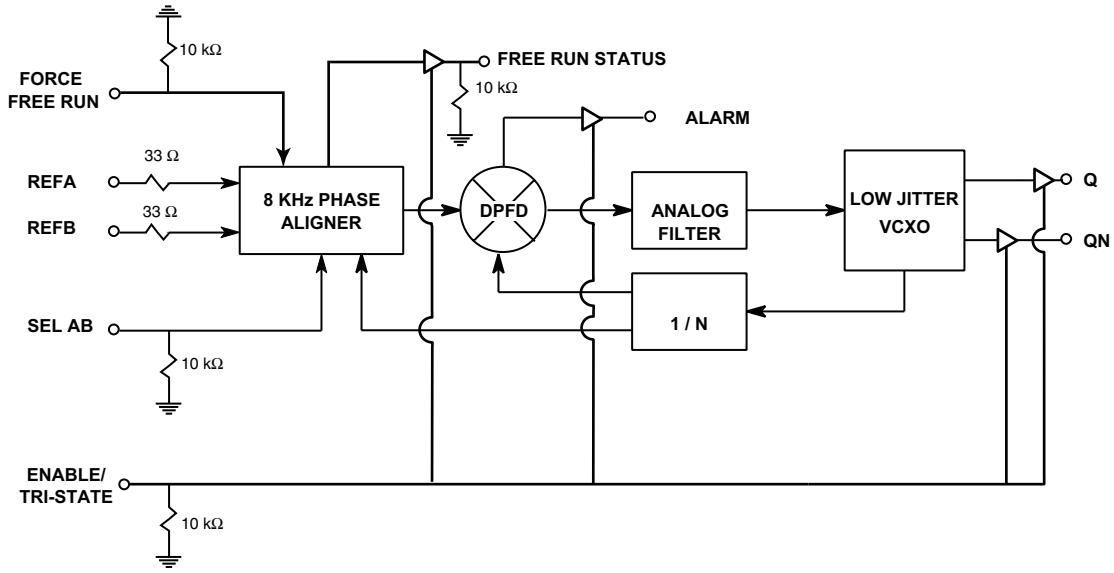
Maximum Dimension Package Outline

Figure 1



Block Diagram

Figure 2



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+100	°C	1.0

Operating Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
R_{IN}	Input Reference Frequency (CMOS)	-	8	-	kHz	
f_{OUT}	Output Frequency (LVPECL)	-	155.52	-	MHz	
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	2.0
I_{cc}	Power Supply Current	-	250	300	mA	5.0
T_o	Temperature Range	0	-	70	°C	
F_{fr}	Free Run Frequency Range	-20	-	20	ppm	
Φ_{gain}	Phase Gain	-	-	0.2	dB@~0.1Hz	
F_{cap}	Capture/pull-in range	-25	-	25	ppm	
F_{bw}	Jitter Filter Bandwidth	27	-	64	Hz	3.0
t_{jtol}	Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	31.25	-	-	µs	8 kHz Ref. units
t_{aq}	Typical Acquisition Time Data					
	Acquisition from a cold power-up:					
	Phase lock within 12ns:		<3		sec.	
	Phase lock settled:		<3		sec.	
	Alarm time:		<1		sec.	
	Acquisition from Free Run:					
	Phase lock within 12ns:		<3		sec.	
	Phase lock settled:		<3		sec.	
	Alarm time:		1		sec.	
	Frequency lock with a 20PPM reference frequency step: Typically 30ms.					
	Phase lock during a switch between equal frequency references: Typically 0.1s, no alarm should be issued					
t_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	4.0
DC	Output Duty Cycle	40	50	60	%	
$MTIE_{sr}$	MTIE at Synchronization Rearrangement		GR-253-CORE.1999 R5-135			5.0,6.0
	Dynamic Offset Range (0°- 70°)	-	-	20	ns	
	Dynamic Offset Range (25°- 70°)	-	-	13	ns	
	Unit to Unit Phase Differential	-	-	100	ns	7.0

Output Jitter Specifications

Table 3

	Jitter BW 10 Hz - 1 MHz		SONET Jitter BW 12 kHz - 20 MHz	
Frequency (MHz)	pS (RMS)	m UI	pS (RMS)	m UI
155.52	20 Typ.	3.110 Typ.	1 Max.	0.156 Max.

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (22 uF, 330 pF)

3.0 3db loop response.

4.0 50-ohm load biased to 1.3 volts.

5.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

6.0 The wider bandwidth of this model may result in a break in the GR-253-CORE, R5-135 Switching Mask for observation times of <50ms

7.0 Under rapidly changing input conditions. (-11ppm to +11ppm)

Input And Output Characteristics

Table 4

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input and Output Characteristics						
V_{ih}	High Level Input Voltage	2.0	-	5.5	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage	-	-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
PECL Output Characteristics						
V_{oh}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{ol}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_l	Output Capacitance	-	-	10	pF	
T_{skew}	Differential Output Skew	-	50	-	ps	

Input Selection / Output Response

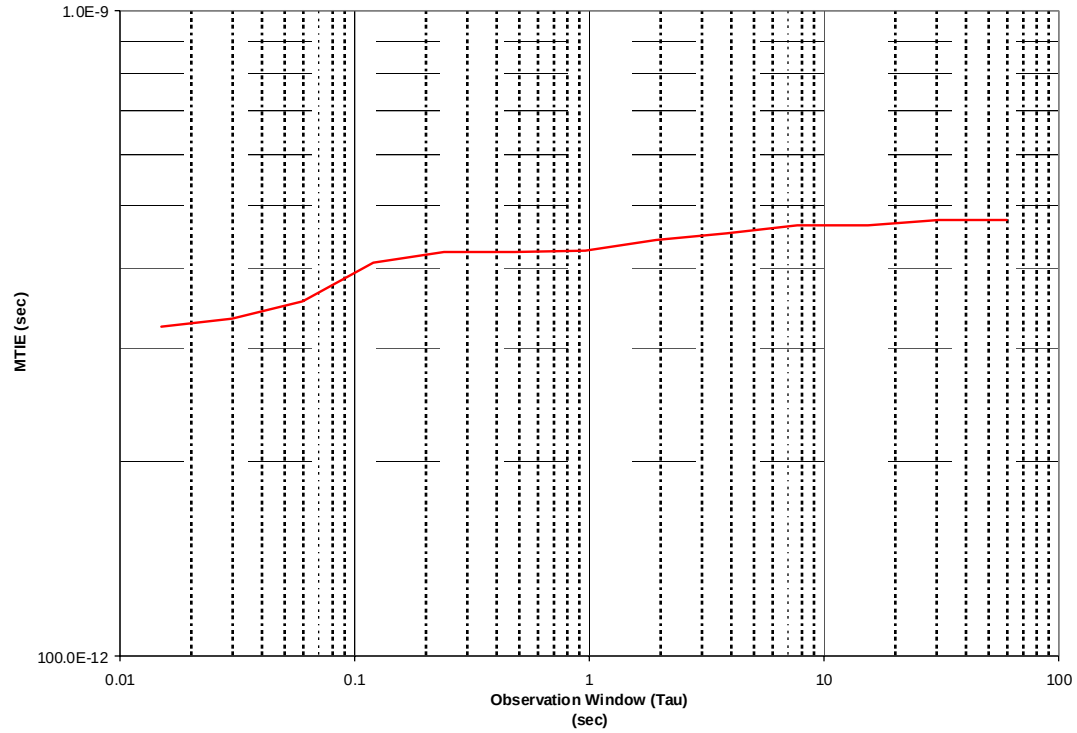
Table 5

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	X	X	X	FR
X	1	X	X	X	X	X	X	0	1	
0	0	X	X	X	1	1	X	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:
A Active
FR Free Run Mode
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

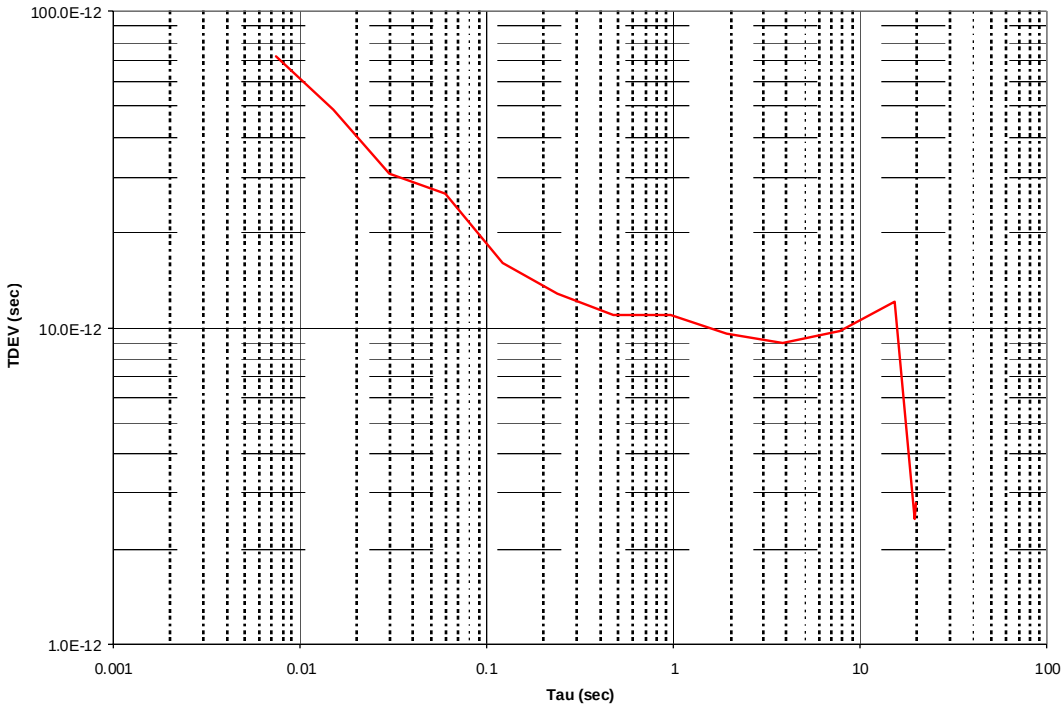
Typical MTIE Measurement

Figure 3



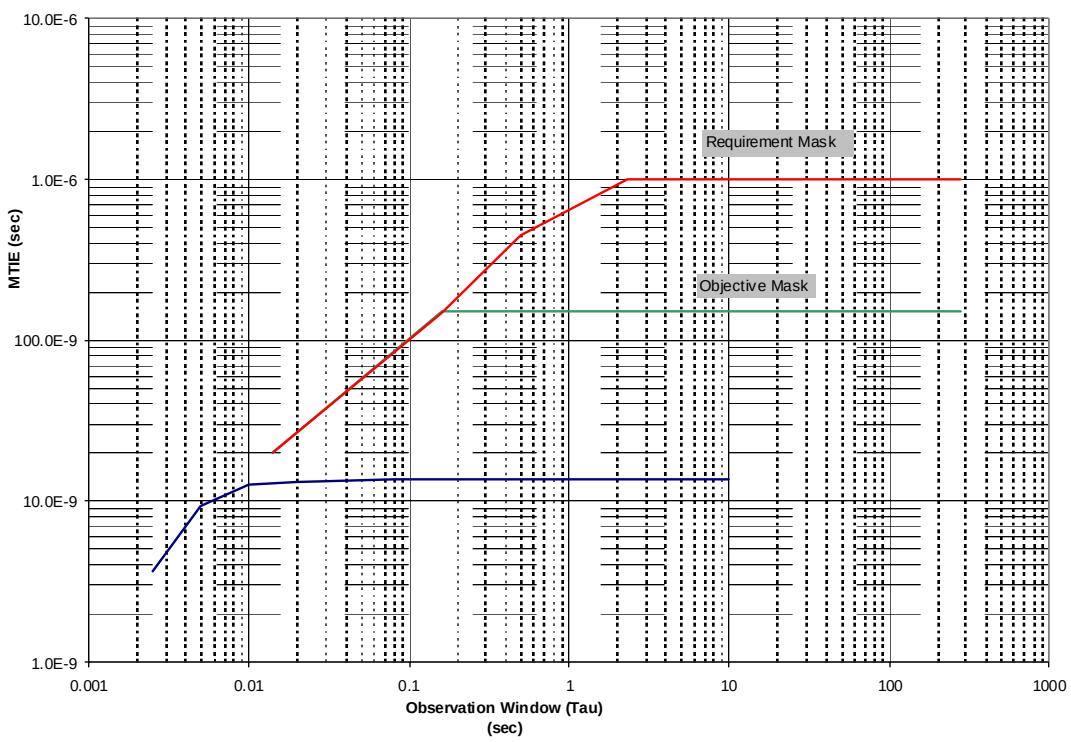
Typical TDEV Measurement

Figure 4



Typical MTIE at Synchronization Rearrangement. Reference B Equal to Inverse of Reference A, No Modulation.

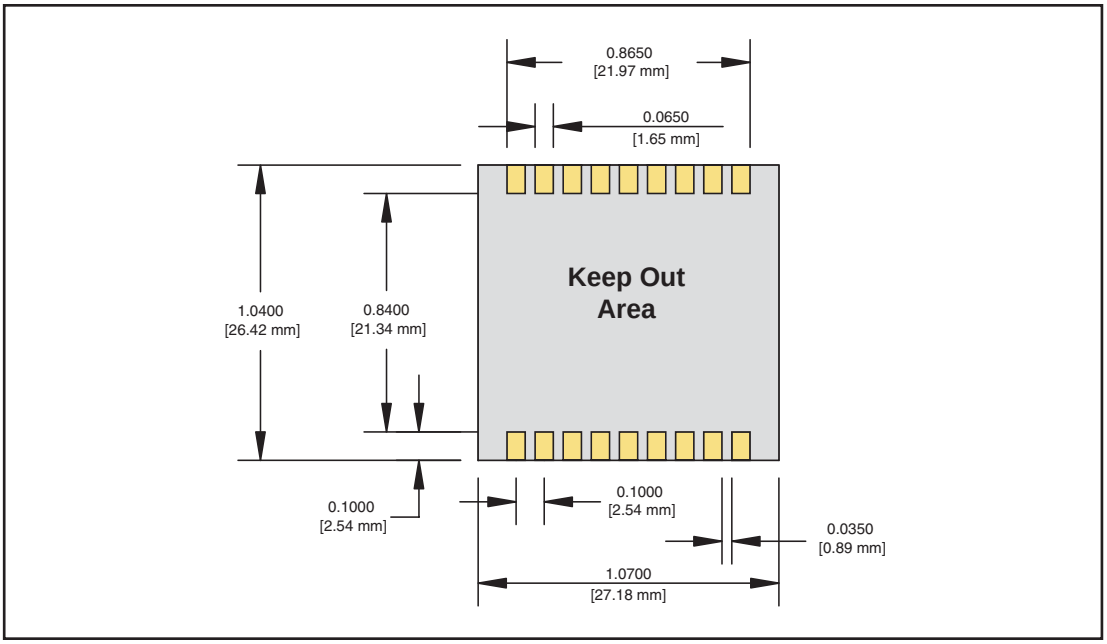
Figure 5



***NOTE:** The wider bandwidth of this model may result in a break in the GR-253-CORE, R5-135 Switching Mask for observation times of <50ms.

Circuit Board Footprint & Keepout Recommendations

Figure 6



Pin Description

Table 6

Pin #	Pin Name	Pin Information	Note
1	ENABLE/TRI-STATE	VCXO Enable. (Enable = 0, Disable = 1 = CMOS Outputs Tri-stated)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	CMOS Reference Frequency Input.	
5	SEL_{AB}	Input Reference Select Pin. (REFA = 0, REFB = 1)	9.0
6	RESET	RESET. (RESET = 1)	9.0
7	REF_B	CMOS Reference Frequency Input.	
8	V_{ee}	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	N/C	No Connection.	8.0
12	ALARM	Loss of Reference / Lock alarm. (Alarm = 1)	
13	FR	Force Free Run. (Phase Lock = 0, Free Run = 1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	LVPECL Complementary Output.	
17	V_{ee}	Ground.	
18	Q	LVPECL Output.	

NOTES
8.0 Do not connect pin
9.0 Input pulled to ground

Ordering Information

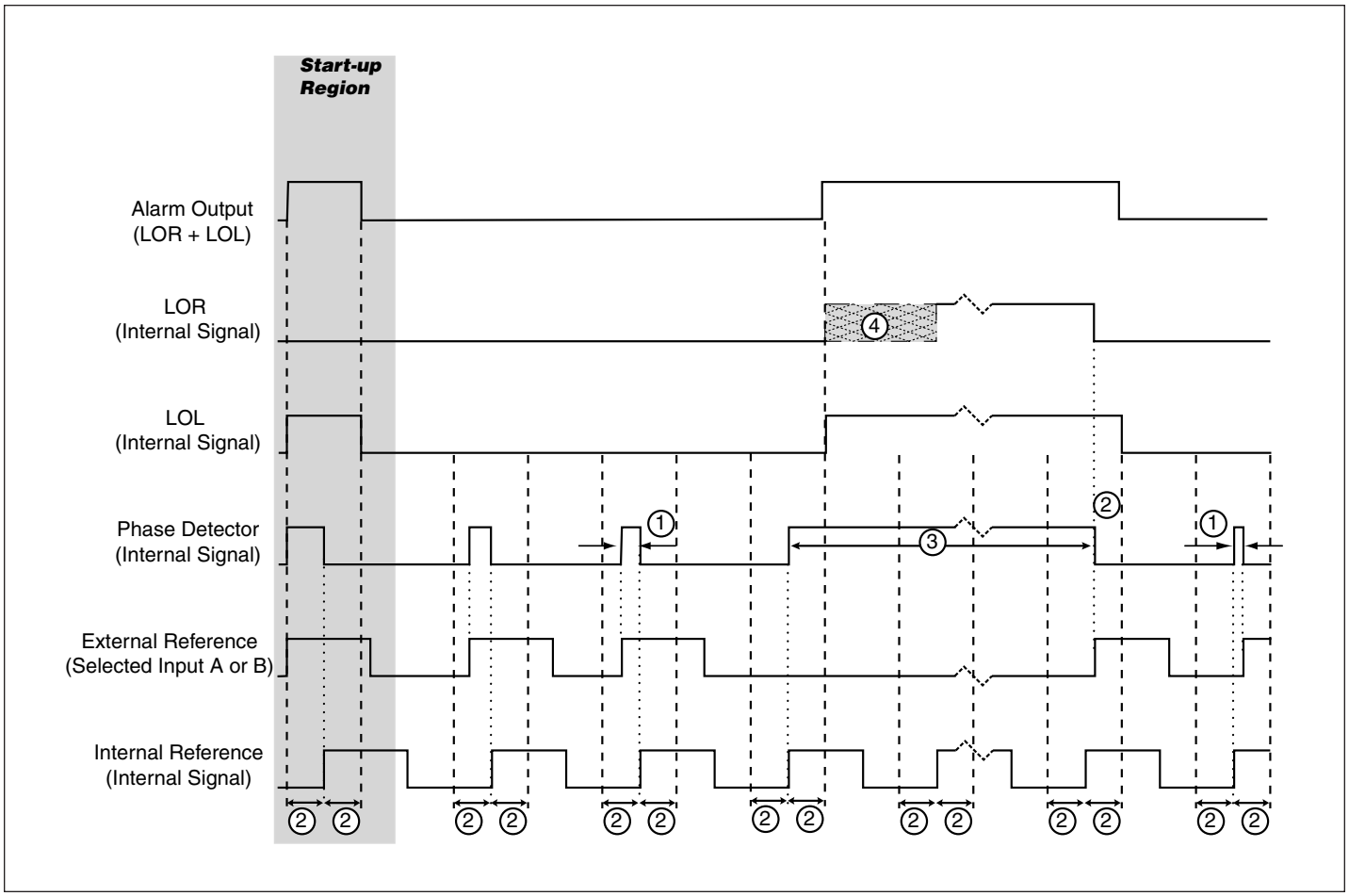
SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (4503)
FFF.FFF equals the Oscillator Output frequency (155.52)
M equals MHZ and is added to all part numbers

Example: To order an SCG4503 with an Oscillator Output of 155.52 MHz,
Order part number SCG4503-155.52M

Loss of Reference Condition Alarm Timing

Figure 7



AlarmTiming Legend

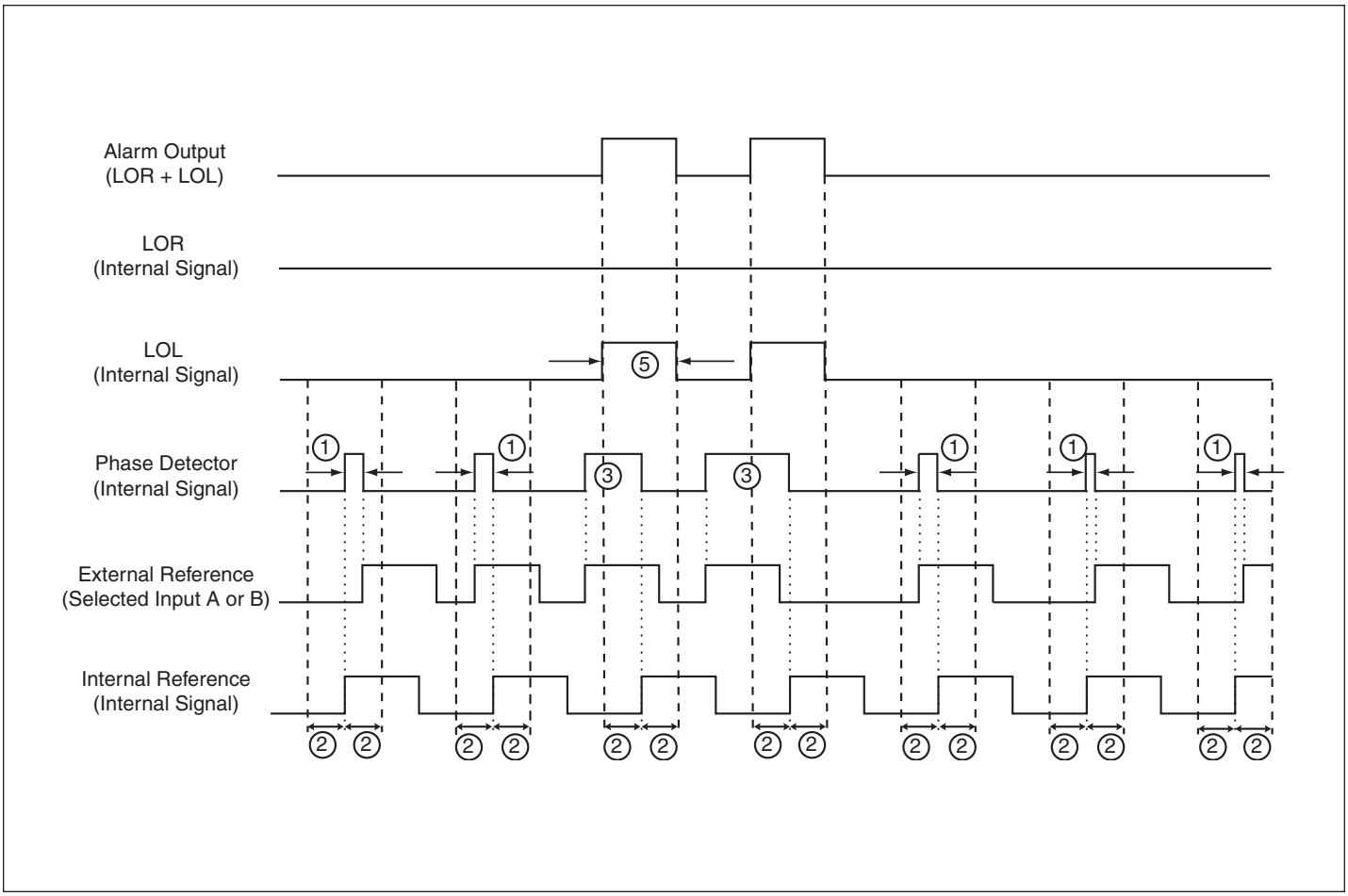
Use for all alarm timing diagrams

Table 7

	8 kHz Reference Input
1	< 31.25 µsec
2	31.25 µsec
3	> 31.25 µsec
4	125 µsec wide range
5	Minimum pulse width = 62.5 µsec
Start-up Region	During Start-up, The LOL Alarm will pulse during the first few seconds of operation

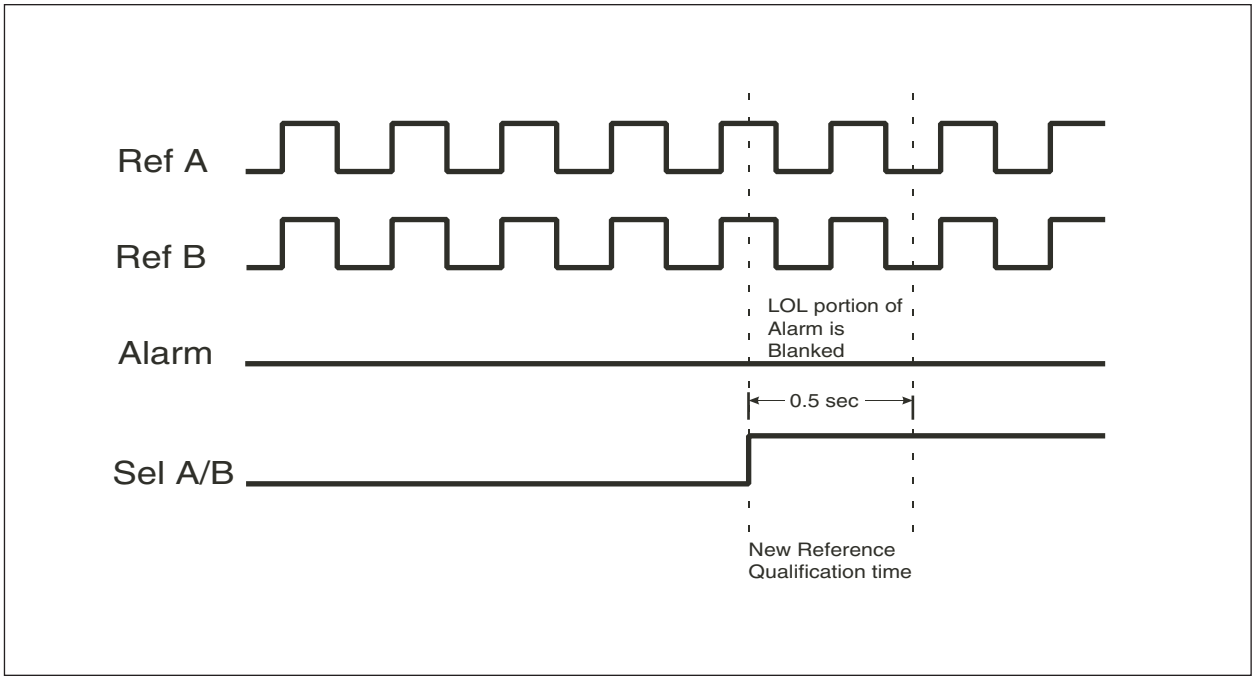
Loss of Lock Condition Alarm Timing

Figure 8



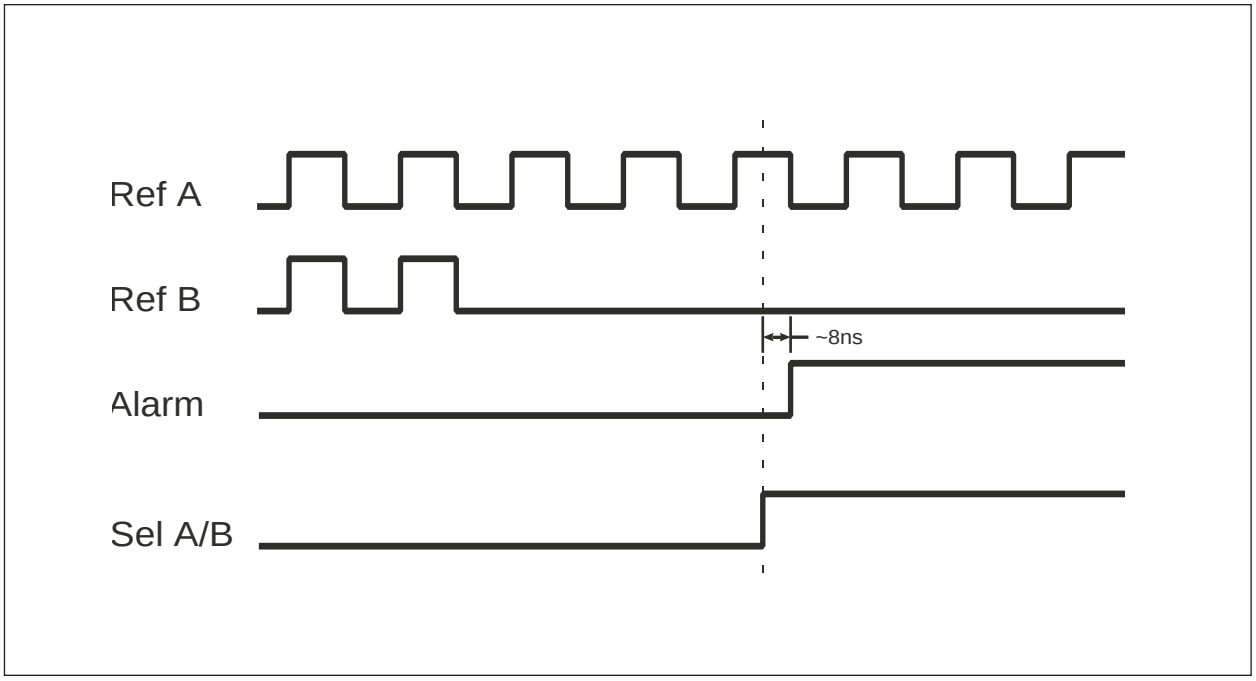
Switch from A to B when both are good signals

Figure 9



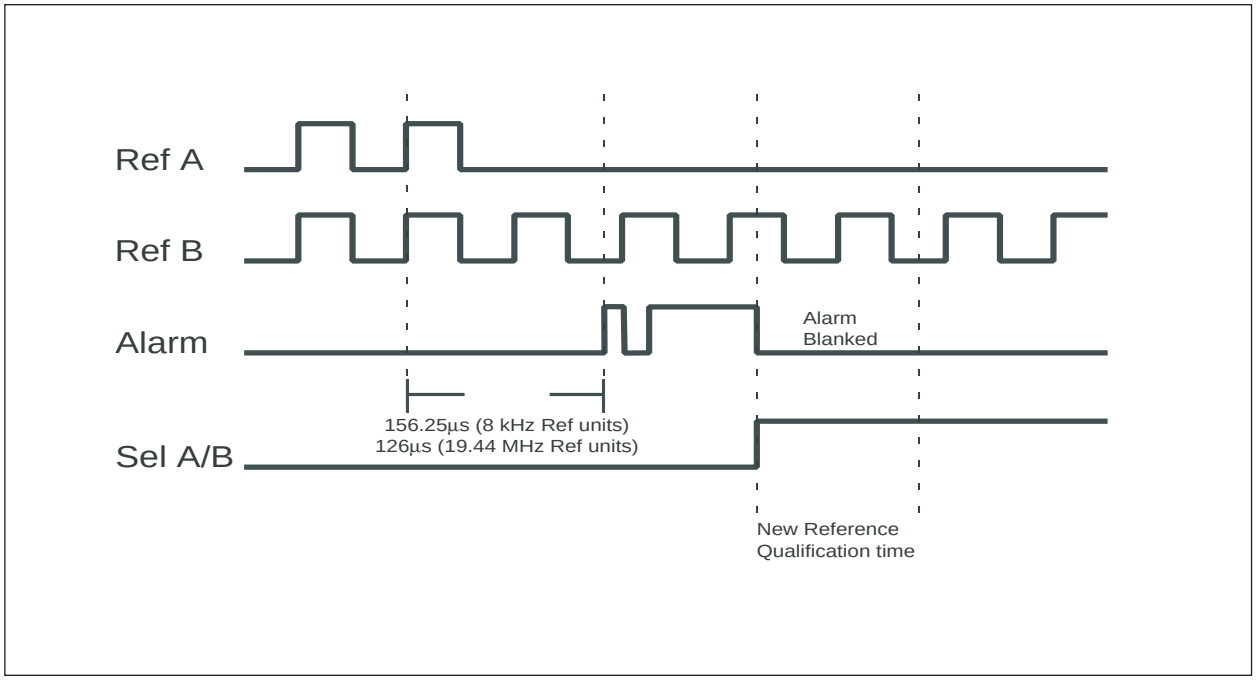
Switch from A to B when Reference B is lost

Figure 10



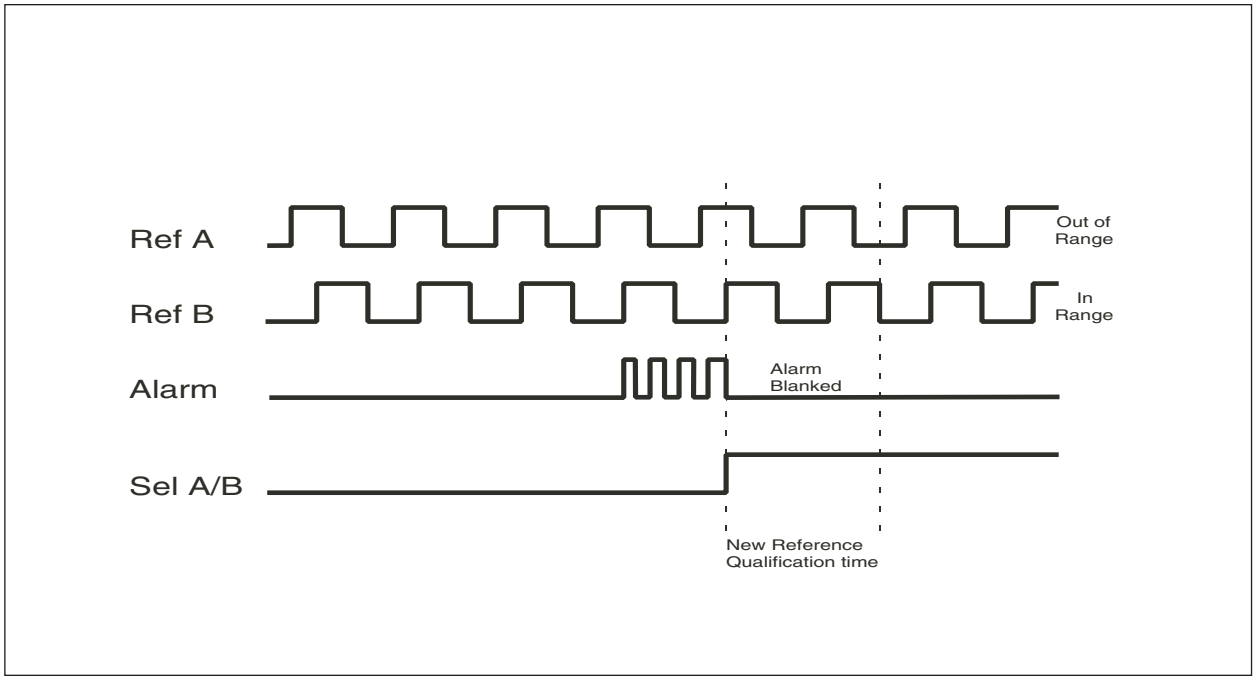
Switch from A to B after Reference A is lost

Figure 11



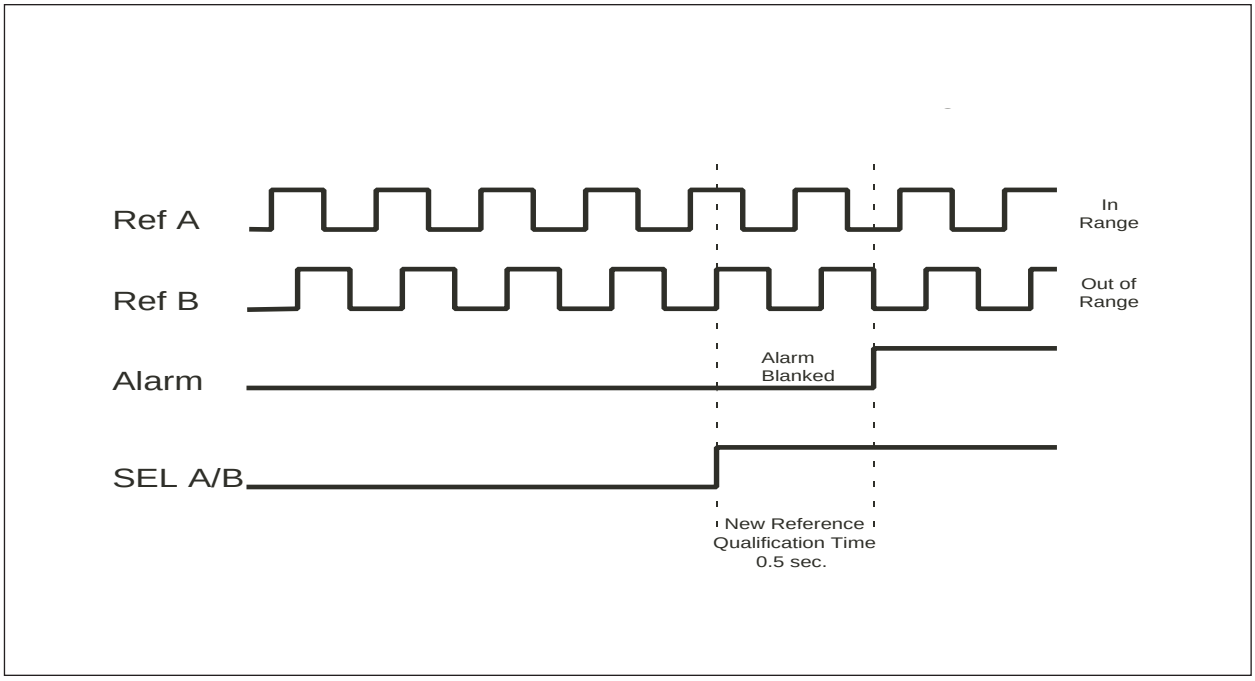
Switch from A to B when A is out of range

Figure 12



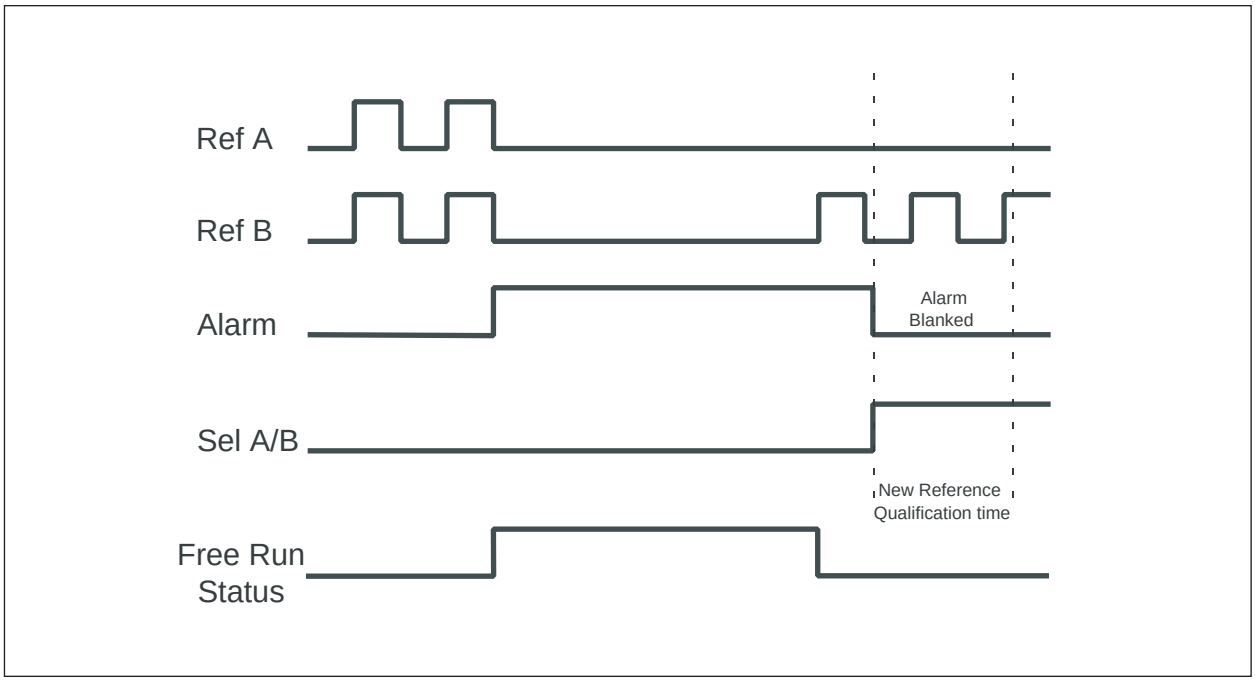
Switch from A to B when B is out of range

Figure 13



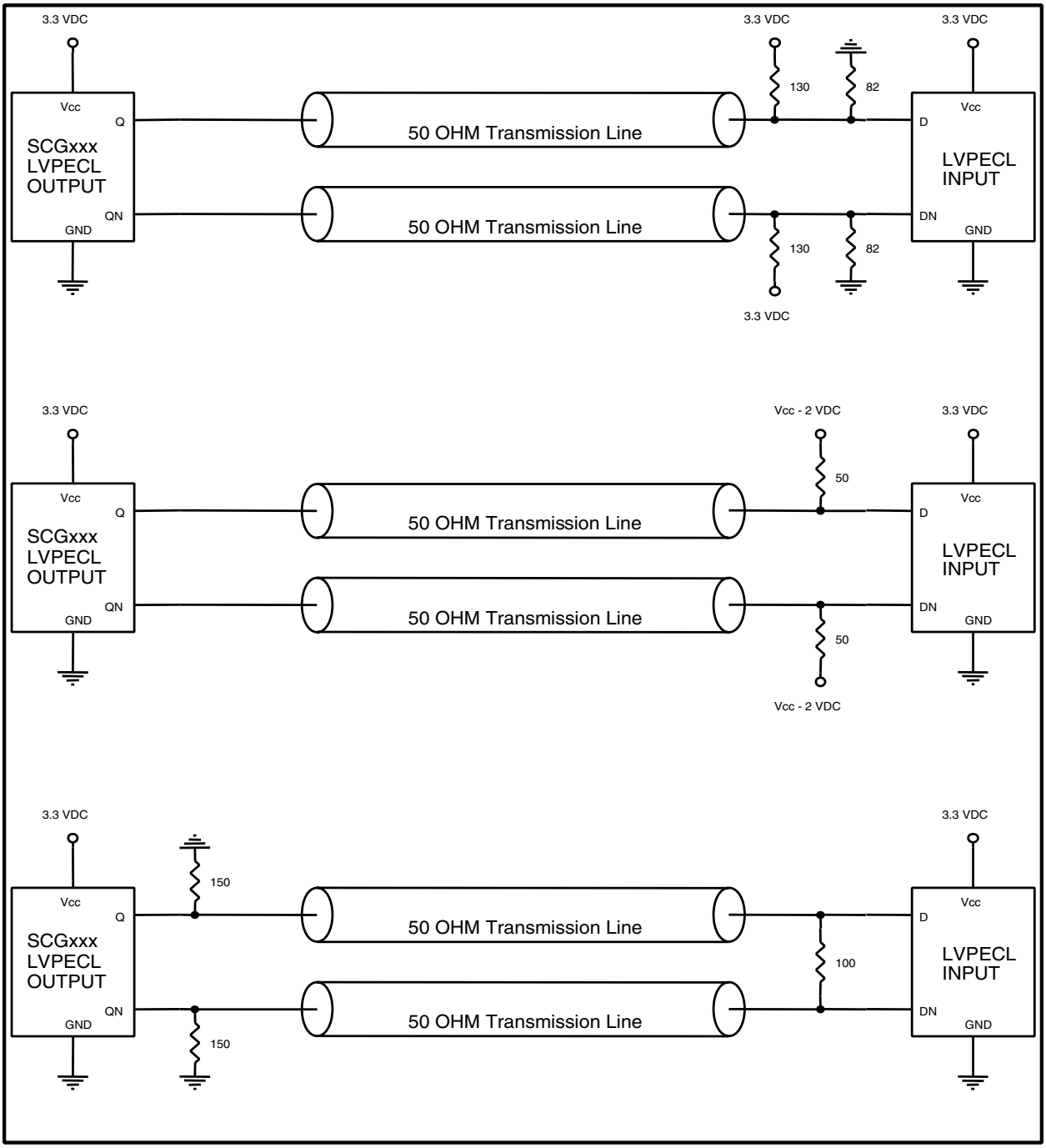
Switch from A to B when both references have been lost and Ref B returns (Automatic Free Run)

Figure 14



Recommended PECL Termination

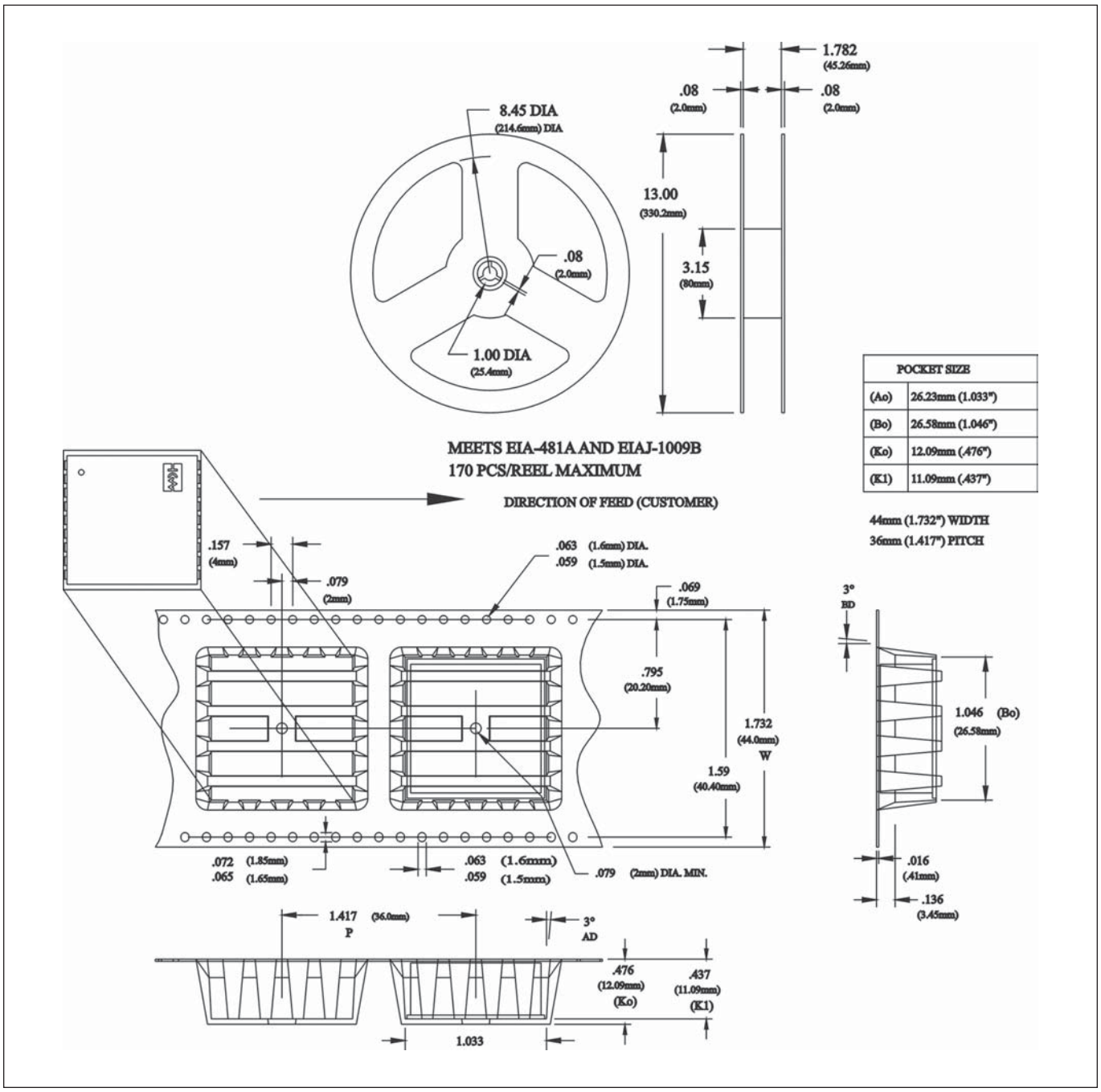
Figure 15



If PECL outputs do not drive a long line (< 0.5”),
a single 150Ω termination resistor to ground may be used for each pin.

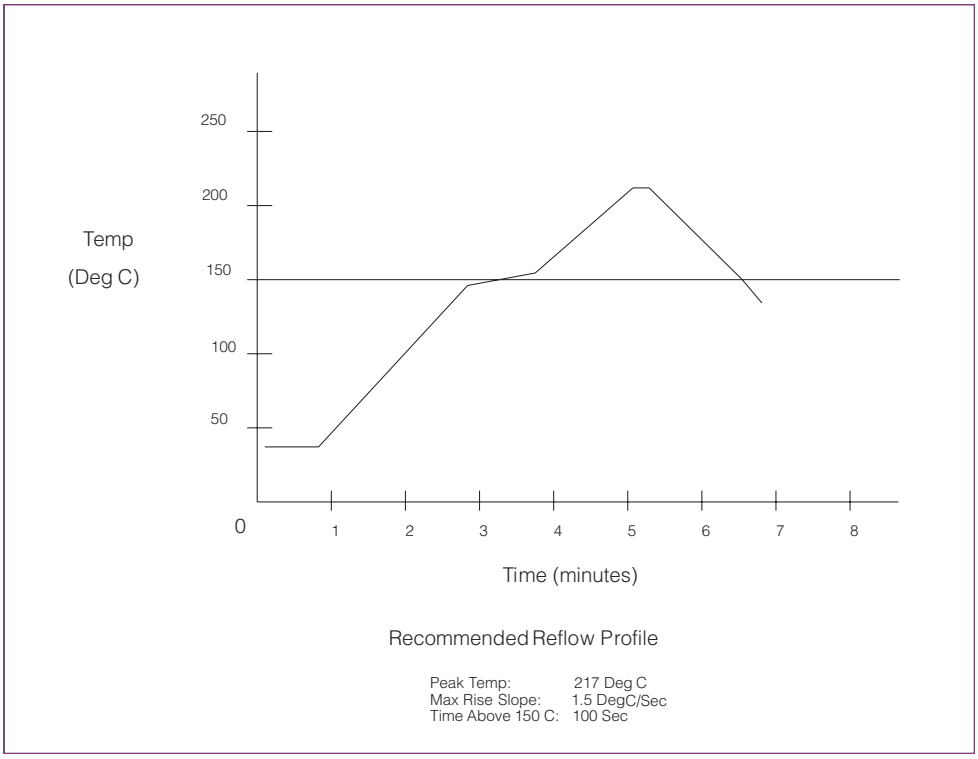
Tape and Reel Packaging

Figure 16



Solder Profile

Figure 17



Model Comparison Table

Table 8

Model	Input Ref Freq	Max Duty Cycle	Oscillator Output (Synchronized Output)	Notes
SCG4500	2@8 kHz	40/60	77.76 MHz,155.52 MHz,125 MHz	Basic Model
SCG4503	2@8 kHz	40/60	155.52 MHz	27-64 Hz Jitter Bandwidth
SCG4510	2@1.544 MHz	40/60	155.52 MHz	
SCG4520	2@19.44 MHz	40/60	77.76 MHz,155.52 MHz	
SCG4540	2@10 kHz	40/60	163.84 MHz	

Other low jitter line card solutions from Connor-Winfield

SCG51 Series	Single input, jitter filtered with Free Run, 1 CMOS and 3 LVPECL outputs up to 622.08 MHz.
SCG102A/104A	Single input, frequency selectable, LVPECL clock smoothers from 77.76 to 777.76 MHz.
SCG2000 Series	Single input, jitter filtered with 20ppm Free Run, CMOS outputs from 8 kHz to 125.0 MHz.
SCG2500 Series	Dual input, jitter filtered with Free Run, CMOS outputs up to 125.0 MHz.
SCG3000 Series	Single input, jitter filtered with Dual LVPECL outputs.
SCG4000 Series	Single input, jitter filtered with 20ppm Free Run, LVPECL outputs from 77.76 MHz to 180 MHz.
SCG4600 Series	Dual input, jitter filtered with Free Run, 1 CML differential pair output up to 622.08 MHz.

Revision	Revision Date	Note
00	06/17/05	Final Release