# NPIC6C596A-Q100

## Power logic 8-bit shift register; open-drain outputs

Rev. 1 — 18 October 2013 **Product data sheet**

## 1. General description

The NPIC6C596A-Q100 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ resets both the shift register and storage register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. To provide additional hold time in cascaded applications, the serial output QS7 is clocked out on the falling edge of SHCP. Data in the storage register drives the gate of the output extended-drain NMOS (EDNMOS) transistor whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs, provide protection against inductive transients. These voltage clamps make the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Wide supply range 2.3 V to 5.5 V
- Low $R_{DSon}$
- Eight Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption
- ESD protection:
  - HBM AEC-Q100-002 revision D exceeds 2500 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V

## 3. Applications

- LED sign
- Graphic status panel
- Fault status indicator

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| NPIC6C596AD-Q100 | –40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| NPIC6C596APW-Q100 | –40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| NPIC6C596ABQ-Q100 | –40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

## 5. Functional diagram

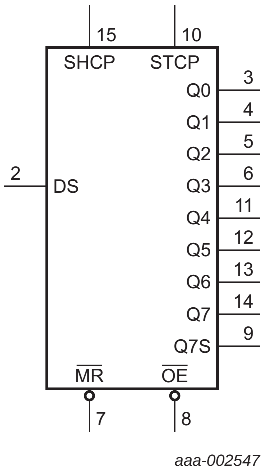



**Fig 1. Logic symbol**

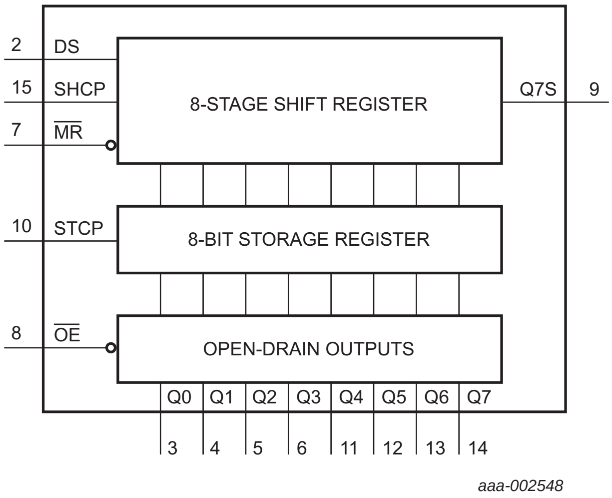



**Fig 2. Functional diagram**

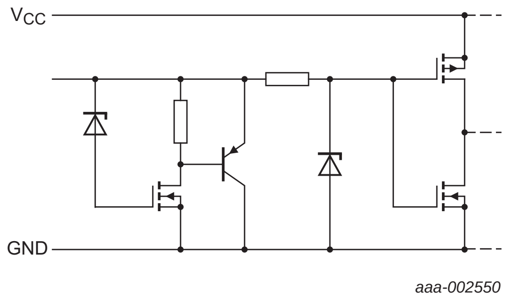



Fig 3. Schematic of all inputs

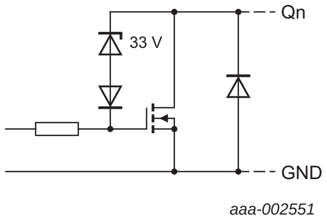



Fig 4. Schematic of open-drain outputs (Qn)

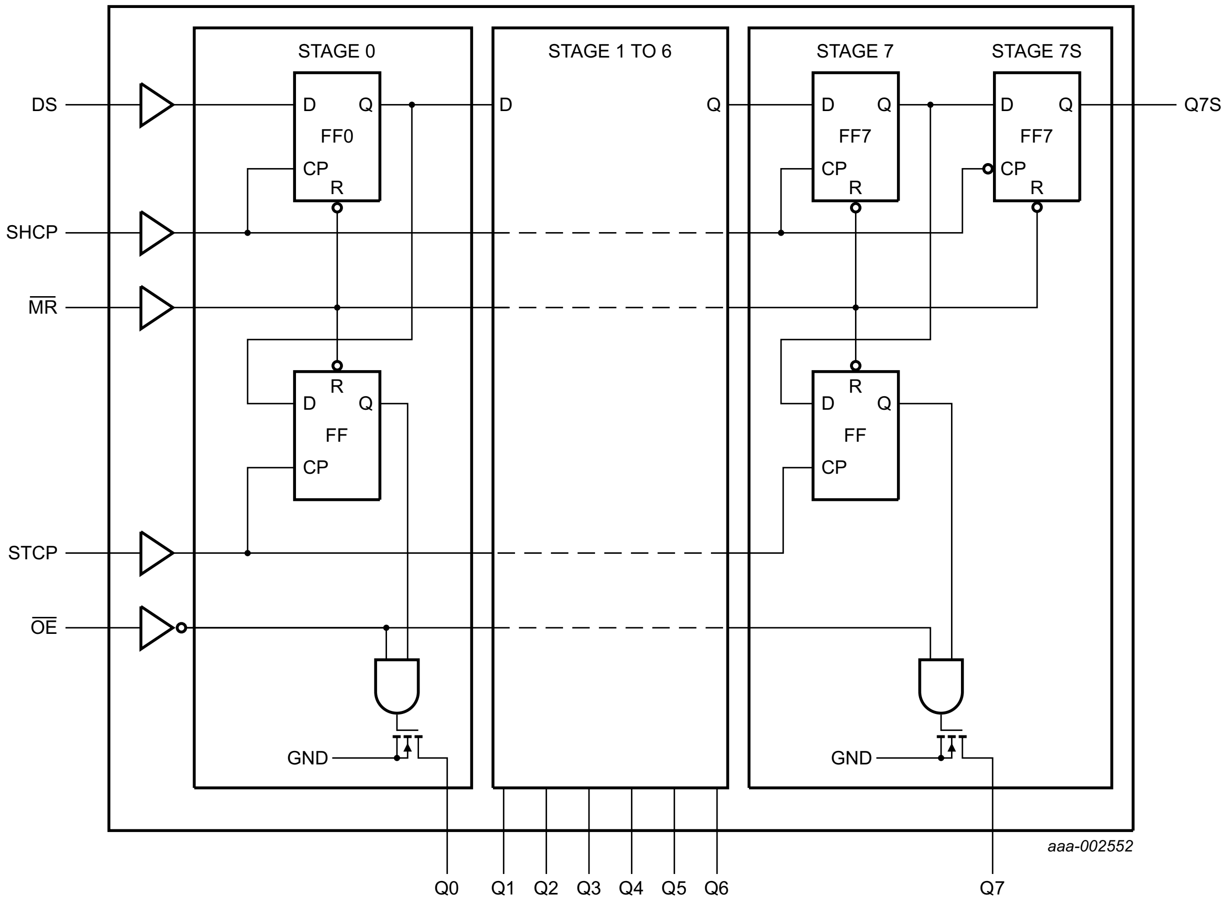



Fig 5. Logic diagram

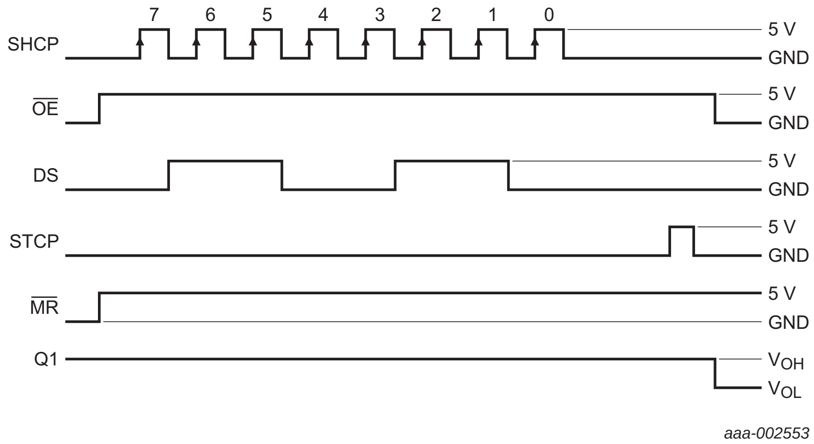



Fig 6. Timing diagram

# 6. Pinning information

## 6.1 Pinning

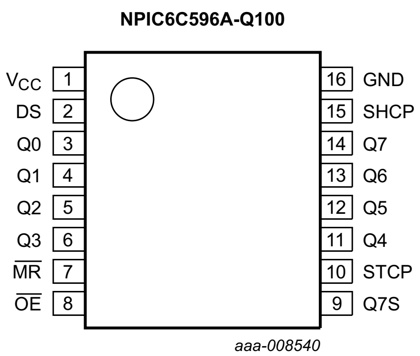
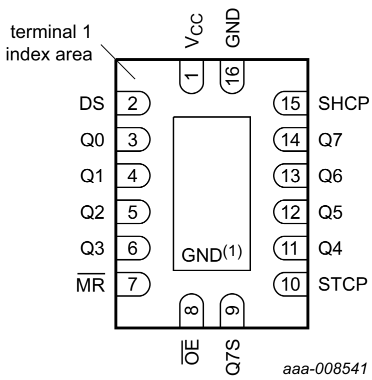



Fig 7. Pin configuration SO16 and TSSOP16




(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 8. Pin configuration DHVQFN16

### 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{CC}$ | 1 | supply voltage |
| DS | 2 | serial data input |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 3, 4, 5, 6, 11, 12, 13, 14 | parallel data output (open-drain) |
| $\overline{MR}$ | 7 | master reset (active LOW) |
| $\overline{OE}$ | 8 | output enable input (active LOW) |
| Q7S | 9 | serial data output |
| STCP | 10 | storage register clock input |
| SHCP | 15 | shift register clock input |
| GND | 16 | ground (0 V) |

## 7. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | | –0.3 | +7.0 | V |
| $V_{DS}$ | drain-source voltage | power EDNMOS drain-source voltage | [1] | - | +33 | V |
| $I_{d(SD)}$ | source-drain diode current | continuous | | - | 250 | mA |
| | | pulsed | [2] | - | 500 | mA |
| $I_D$ | drain current | $T_{amb}$ = 25 °C | | | | |
| | | continuous; each output; all outputs on | | - | 100 | mA |
| | | pulsed; each output; all outputs on | [2] | - | 250 | mA |
| $I_{DM}$ | peak drain current | single output; $T_{amb}$ = 25 °C | [2] | - | 250 | mA |
| $E_{AS}$ | non-repetitive avalanche energy | single pulse; see Figure 9 | [3] | - | 30 | mJ |
| $I_{AL}$ | avalanche current | see Figure 9 | [3] | - | 200 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |

**Table 3. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{amb}$ = 25 °C | [4] | | | |
| | | SO16 | | - | 800 | mW |
| | | TSSOP16 | | - | 725 | mW |
| | | DHVQFN16 | | - | 1825 | mW |
| | | $T_{amb}$ = 125 °C | [4] | | | |
| | | SO16 | | - | 160 | mW |
| | | TSSOP16 | | - | 145 | mW |
| | | DHVQFN16 | | - | 365 | mW |

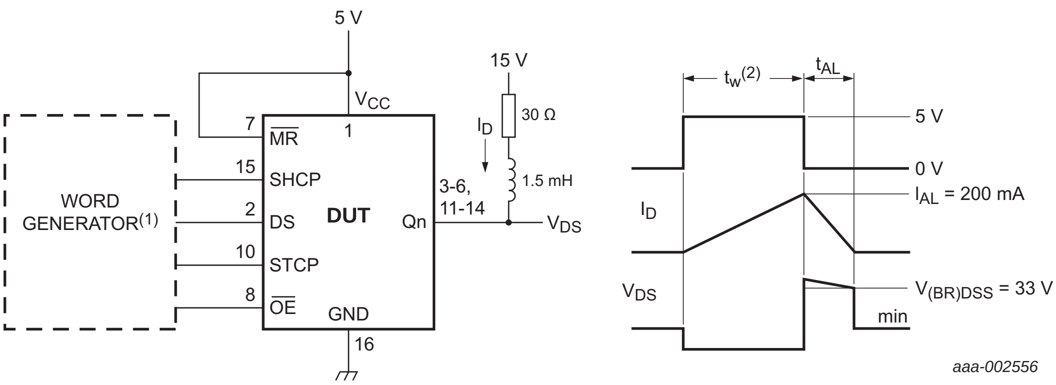
[1] Each power EDNMOS source is internally connected to GND.

[2] Pulse duration ≤ 100 μs and duty cycle ≤ 2 %.

[3] $V_{DS}$ = 15 V; starting junction temperature ($T_j$) = 25 °C; L = 1.5 H; avalanche current ($I_{AL}$) = 200 mA.

[4] For SO16 packages: above 25 °C the value of $P_{tot}$ derates linearly with 6.4 mW/°C.
For TSSOP16 packages: above 25 °C the value of $P_{tot}$ derates linearly with 5.8 mW/°C.
For DHVQFN16 packages: above 25 °C the value of $P_{tot}$ derates linearly with 14.6 mW/°C.

## 7.1 Test circuit and waveform




(1) The word generator has the following characteristics: $t_r$, $t_f$ ≤ 10 ns; $Z_O$ = 50 Ω.

(2) The input pulse duration ($t_W$) is increased until peak current $I_{AL}$ = 200 mA. Energy test level is defined as: $E_{AS} = I_{AL} \times V_{(BR)DSS} \times t_{AL}/2$ = 30 mJ.

**Fig 9. Test circuit and waveform for measuring single-pulse avalanche energy**

## 8. Recommended operating conditions

**Table 4. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | 2.3 | - | 5.5 | V |
| $V_I$ | input voltage | | | 0 | - | 5.5 | V |
| $I_D$ | drain current | pulsed drain output current; $V_{CC}$ = 5 V; $T_{amb}$ = 25 °C; all outputs on | [1][2] | - | - | 250 | mA |
| $T_{amb}$ | ambient temperature | | | –40 | - | +125 | °C |

[1] Pulse duration ≤ 100 µs and duty cycle ≤ 2 %.

[2] Technique should limit $T_j - T_{amb}$ to 10 °C maximum.

## 9. Static characteristics

**Table 5. Static characteristics**

*At recommended operating conditions unless otherwise specified. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 3.0 V to 5.5 V | | 0.85$V_{CC}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 3.0 V to 5.5 V | | - | - | 0.15$V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | serial data output Q7S; $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –20 µA; $V_{CC}$ = 3.0 V | | 2.64 | 4.49 | - | V |
| | | $I_O$ = –4 mA; $V_{CC}$ = 3.0 V | | 2.4 | 4.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | serial data output Q7S; $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 3.0 V | | - | 0.005 | 0.12 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 3.0 V | | - | 0.3 | 0.6 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{CC}$ | | - | - | 1 | µA |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 1 mA | | 33 | 37 | - | V |
| $V_{SD}$ | source-drain voltage | diode forward voltage; $I_F$ = 100 mA | | - | 0.85 | 1.2 | V |
| $I_{CC}$ | supply current | logic supply current; $V_{CC}$ = 5.5 V; $V_I$ = $V_{CC}$ or GND | | | | | |
| | | all outputs off | | - | 0.004 | 200 | µA |
| | | all outputs on | [2] | - | 0.006 | 500 | µA |
| | | all outputs off; SHCP = 5 MHz; $C_L$ = 30 pF; see Figure 14 and Figure 16 | | - | 0.75 | 5 | mA |
| $I_{O(nom)}$ | nominal output current | $V_{DS}$ = 0.5 V; $T_{amb}$ = 85 °C; $I_{out}$ = $I_D$ | [3][4][5] | - | 140 | - | mA |
| $I_{DSX}$ | drain cut-off current | $V_{CC}$ = 5.5 V; $V_{DS}$ = 30 V | | - | 0.002 | 0.2 | µA |
| | | $V_{CC}$ = 5.5 V; $V_{DS}$ = 30 V; $T_{amb}$ = 125 °C | | - | 0.15 | 0.3 | µA |

**Table 5. Static characteristics** *…continued*

*At recommended operating conditions unless otherwise specified. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $R_{DSon}$ | drain-source on-state resistance | see Figure 17 and Figure 18 | [3][4] | | | | |
| | | $V_{CC}$ = 3.0 V; $I_D$ = 50 mA | | - | 3.0 | 11 | Ω |
| | | $V_{CC}$ = 3.0 V; $I_D$ = 50 mA; $T_{amb}$ = 125 °C | | | 5.4 | 14 | Ω |
| | | $V_{CC}$ = 3.0 V; $I_D$ = 100 mA | | - | 3.1 | 12 | Ω |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 5.0 V.

[2] Output currents below 250 mA current limit.

[3] Technique should limit $T_j - T_{amb}$ to 10 °C maximum.

[4] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

[5] Nominal output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_{amb}$ = 85 °C.

## 10. Dynamic characteristics

**Table 6. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); For test circuit, see Figure 14.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $t_{PLH}$ | LOW to HIGH propagation delay | $\overline{OE}$ to Qn; $I_D$ = 75 mA; see Figure 10 and Figure 19 | | - | 97 | - | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | $\overline{OE}$ to Qn; $I_D$ = 75 mA; see Figure 10 and Figure 19 | | - | 9 | - | ns |
| $t_r$ | rise time | $\overline{OE}$ to Qn; $I_D$ = 75 mA; see Figure 10 and Figure 19 | | - | 60 | - | ns |
| $t_f$ | fall time | $\overline{OE}$ to Qn; $I_D$ = 75 mA; see Figure 10 and Figure 19 | | - | 18 | - | ns |
| $t_{pd}$ | propagation delay | SHCP to Q7S; $I_D$ = 75 mA; see Figure 11 | [2] | - | 5 | - | ns |
| $f_{max}$ | maximum frequency | SHCP; $I_D$ = 75 mA; see Figure 11 | [3] | - | - | 10 | MHz |
| $t_{rr}$ | reverse recovery time | $I_F$ = 100 mA; dI/dt = 10 A/μs; see Figure 13 | [4][5] | - | 120 | - | ns |
| $t_a$ | reverse recovery current rise time | $I_F$ = 100 mA; dI/dt = 10 A/μs; see Figure 13 | [4][5] | - | 100 | - | ns |
| $t_{su}$ | set-up time | DS to SHCP; see Figure 12 | | 15 | - | - | ns |
| $t_h$ | hold time | DS to SHCP; see Figure 12 | | 15 | - | - | ns |
| $t_W$ | pulse width | | | 40 | - | - | ns |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 5.0 V.

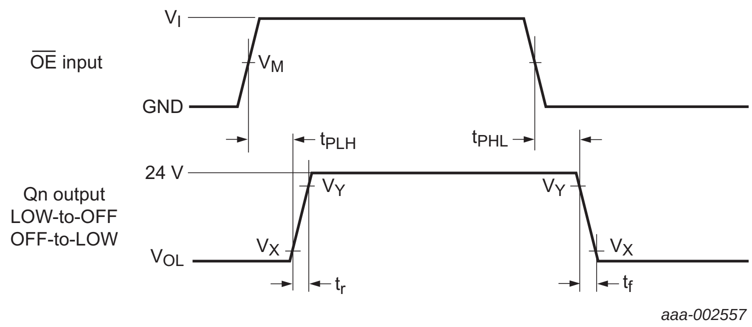
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SHCP → Q7S propagation delay and setup time plus some timing margin.

[4] Technique should limit $T_j - T_{amb}$ to 10 °C maximum.

[5] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

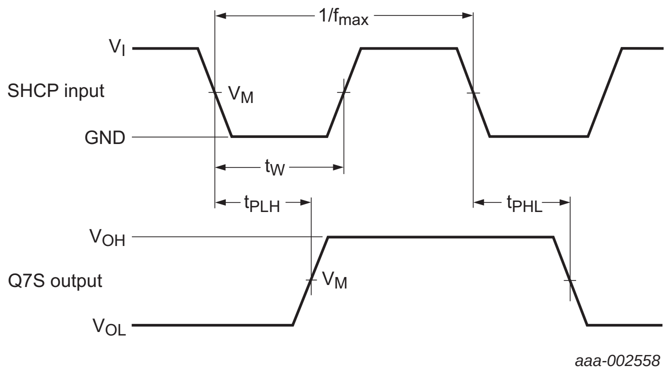
## 10.1 Test circuits and waveforms




Measurement points are given in Table 7.

$V_{OL}$ is the typical output voltage drop that occurs with the output load.

**Fig 10. The output enable ($\overline{OE}$) input to data output (Qn) propagation delays and (Qn) output rise and fall times**



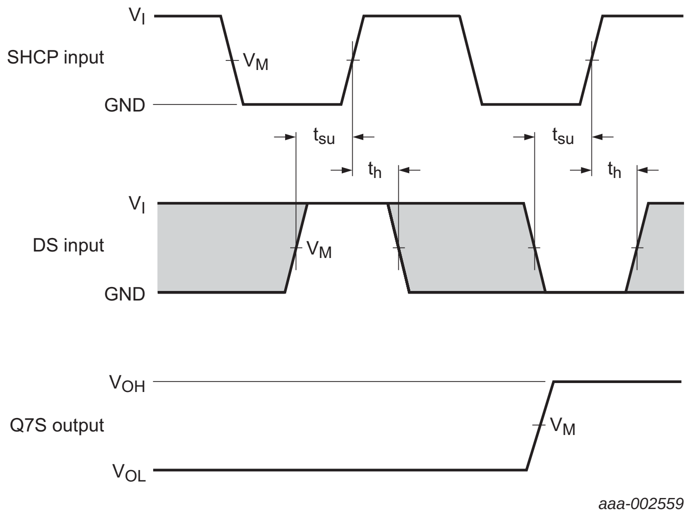

Measurement points are given in Table 7.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 11. The shift clock (SHCP) to serial data output (Q7S) propagation delays with the minimum shift clock pulse width and maximum shift clock frequency**

**Table 7. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 5 V | $0.5V_{CC}$ | $0.5V_{DS}$ | $0.1V_{DS}$ | $0.9V_{DS}$ |




Measurement points are given in Table 8.

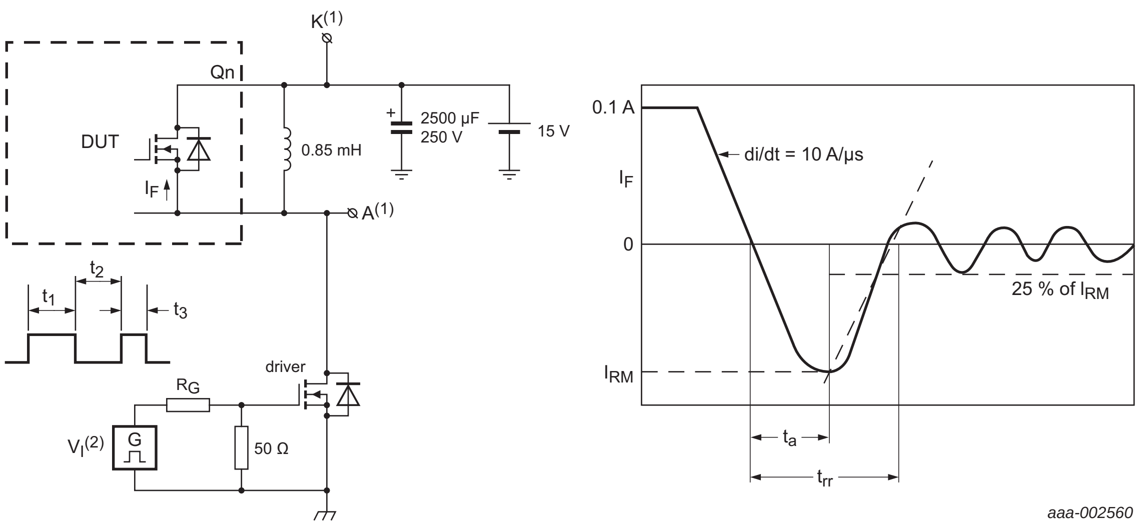
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$ and $V_{OH}$ are the typical output voltage levels that occur with the output load.

**Fig 12. The data set-up and hold times for the serial data input (DS)**

**Table 8. Measurement points**

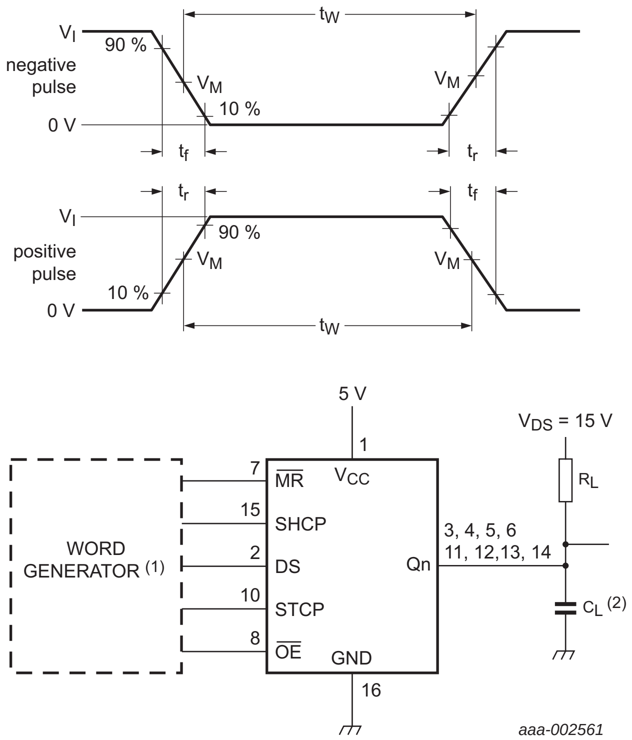
| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| 5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |




(1) The open-drain Qn terminal under test is connected to testpoint K. All other terminals are connected together and connected to testpoint A.

(2) The $V_I$ amplitude and $R_G$ are adjusted for dI/dt = 10 A/μs. A $V_I$ double-pulse train is used to set $I_F$ = 0.1 A, where $t_1$ = 10 μs, $t_2$ = 7 μs and $t_3$ = 3 μs.

**Fig 13. Test circuit and waveform for measuring reverse recovery current**




(1) The word generator has the following characteristics: $t_r$, $t_f \leq 10$ ns; $t_W = 300$ ns; pulsed repetition rate (PRR) = 5 kHz; $Z_O = 50\ \Omega$.

(2) $C_L$ includes probe and jig capacitance.

Test data is given in Table 9. Definitions for test circuit:

$V_{DS}$ = External voltage for Power EDNMOS drain-source voltage.

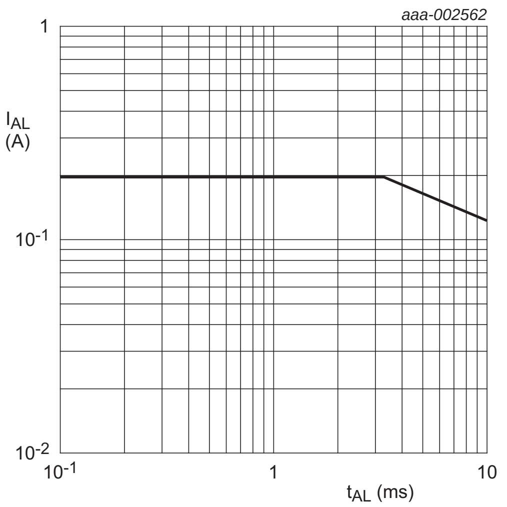
$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

**Fig 14. Test circuit for measuring switching times**

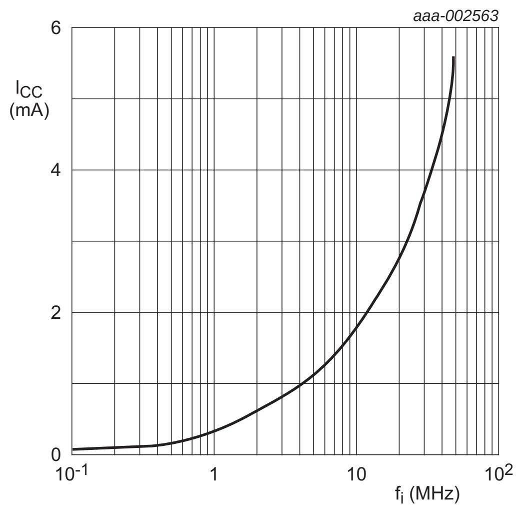
**Table 9. Test data**

| Supply voltage | Input | | | Load | |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $V_M$ | $C_L$ | $R_L$ |
| 5 V | 5 V | ≤ 10 ns | 50% | 30 pF | 200 Ω |



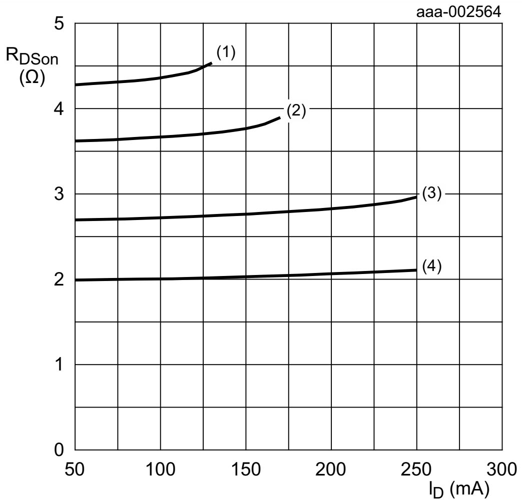

$T_{amb}$ = 25 °C.

**Fig 15. Avalanche current (peak) versus time duration of avalanche**




$T_{amb}$ = –40 °C to 125 °C; $V_{CC}$ = 5 V.

**Fig 16. Supply current versus frequency**




$V_I$ = $V_{CC}$ or GND and $V_O$ = GND or $V_{CC}$.

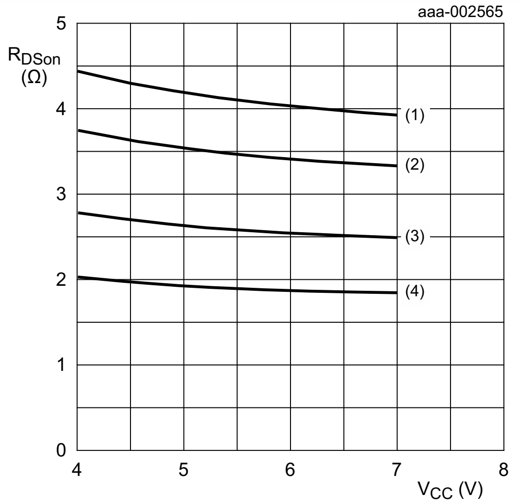
(1) $T_{amb}$ = 125 °C

(2) $T_{amb}$ = 85 °C

(3) $T_{amb}$ = 25 °C

(4) $T_{amb}$ = –40 °C

**Fig 17. Drain-source on-state resistance versus drain current**




$V_I$ = $V_{CC}$ or GND and $V_O$ = open circuit.

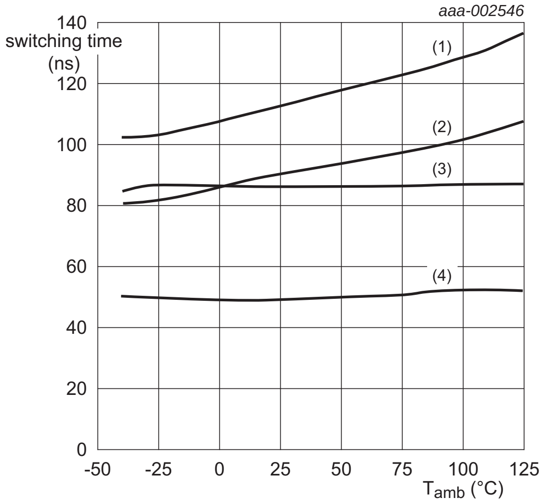
(1) $T_{amb}$ = 125 °C

(2) $T_{amb}$ = 85 °C

(3) $T_{amb}$ = 25 °C

(4) $T_{amb}$ = –40 °C

**Fig 18. Static drain-source on-state resistance versus supply voltage**




Technique should limit $T_J - T_C$ to 10 °C maximum.

(1) $t_{PLH}$.

(2) $t_r$.

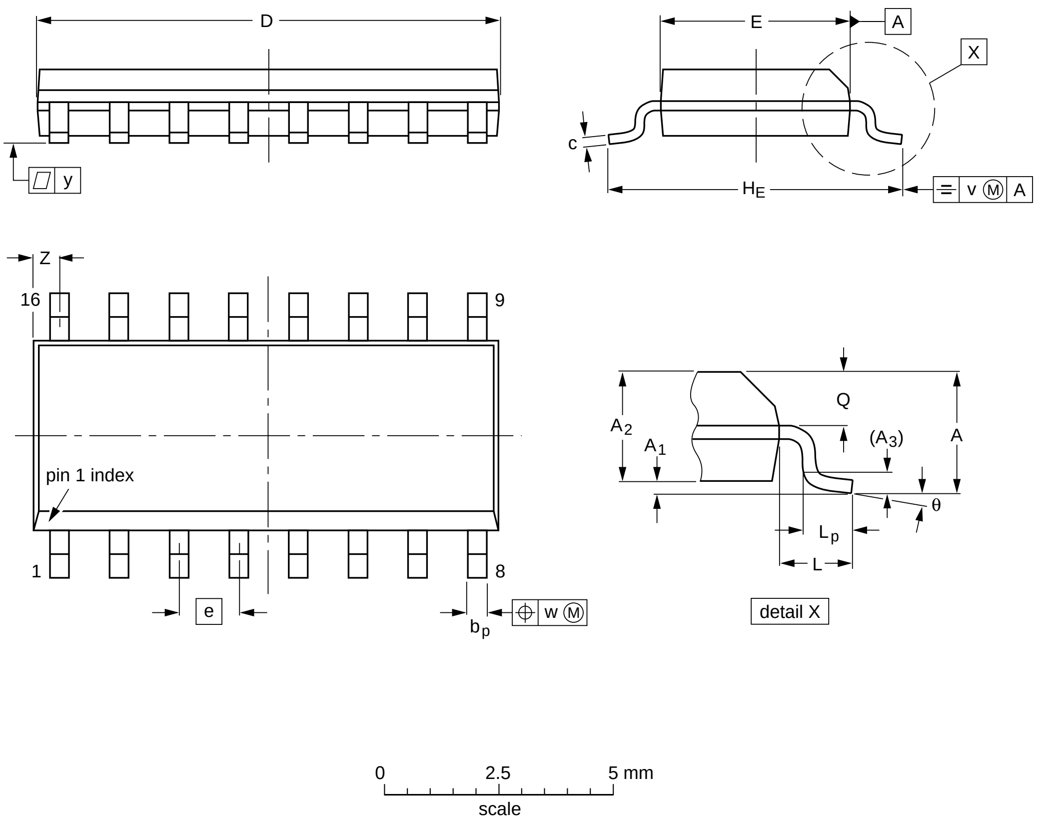
(3) $t_f$.

(4) $t_{PHL}$.

**Fig 19. Switching time versus case temperature**

## 11. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D[(1)] | E[(1)] | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z[(1)] | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

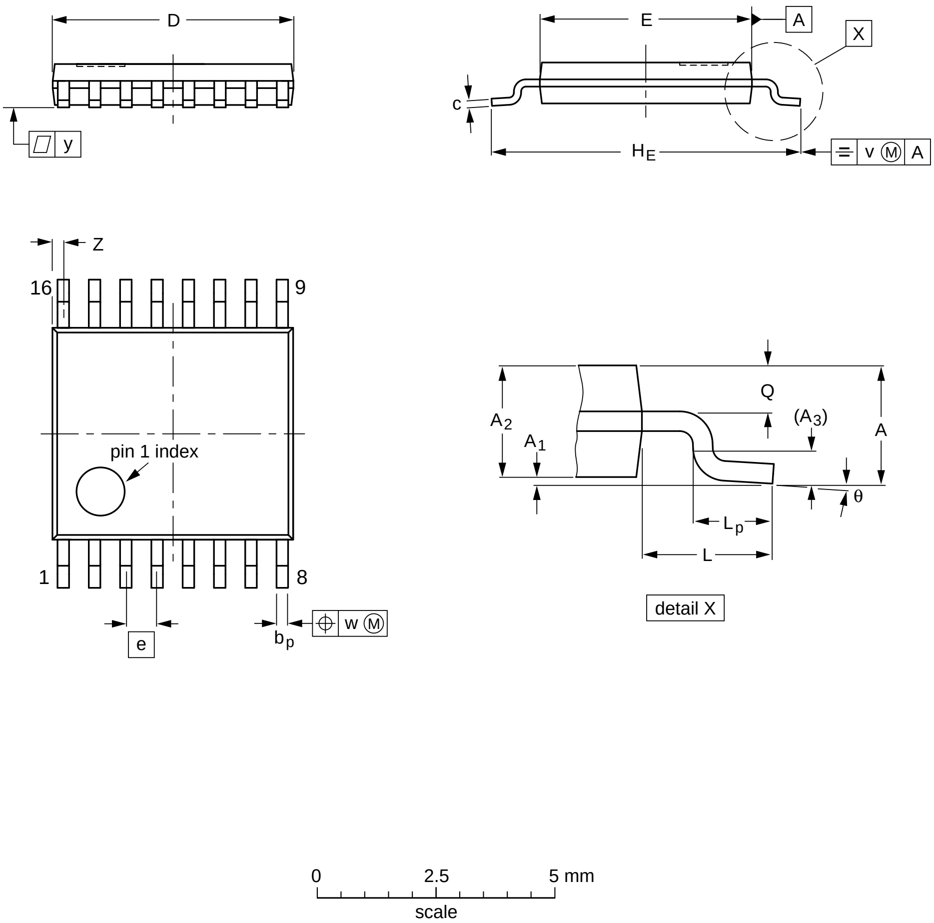
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 20. Package outline SOT109-1 (SO16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

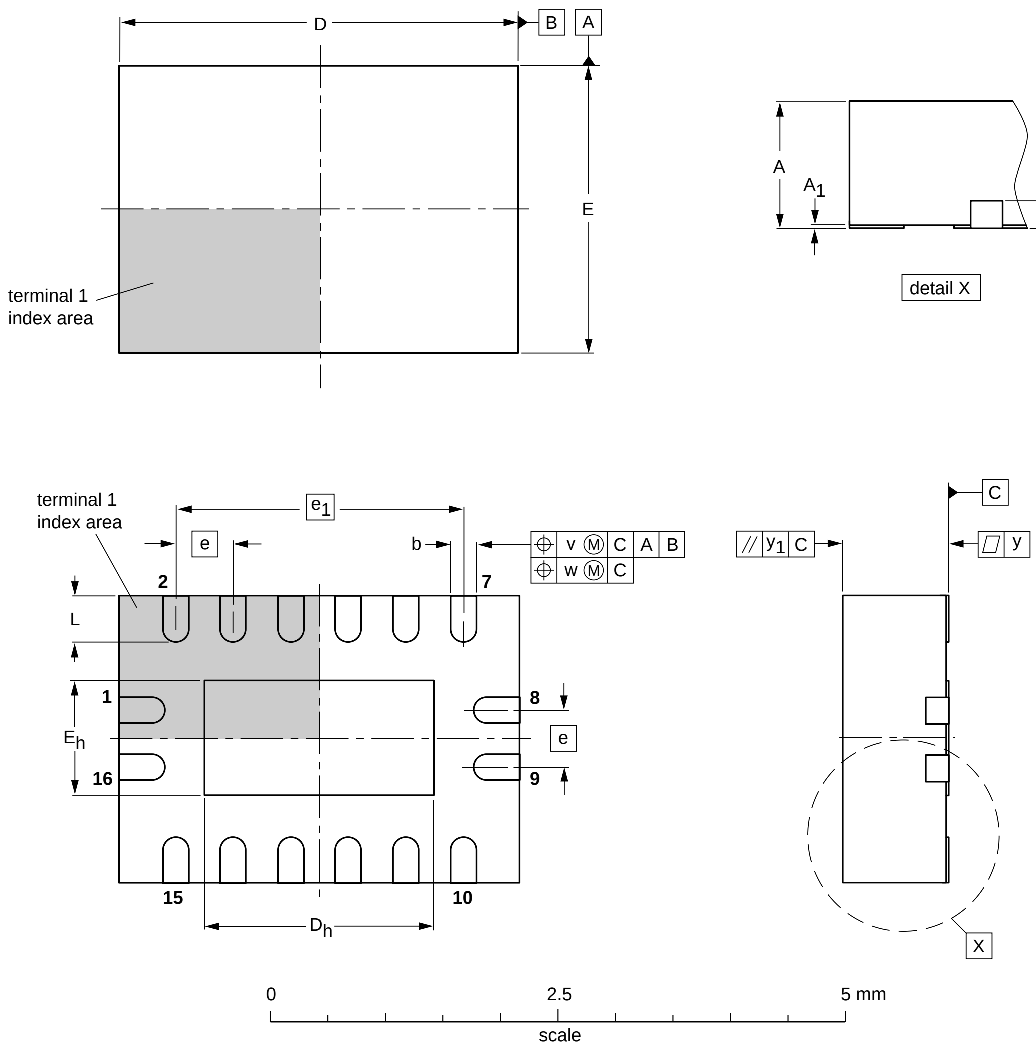
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 21. Package outline SOT403-1 (TSSOP16)**

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 22. Package outline SOT763-1 (DHVQFN16)**

## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| EDNMOS | Extended Drain Negative Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NPIC6C596A_Q100 v.1 | 20131018 | Product data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 16. Contents





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