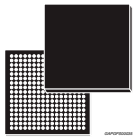
STA2065

Cartesio™ family
Infotainment application processor with embedded GPS

Data brief – production data

Features

- ARM1176 754/624/533 MHz host processor
  - Cache: 32 KB instruction, 32 KB data
  - Vector floating point unit
- High performance embedded GPS subsystem
  - Parallel acquisition engines for 8 GPS satellites or 4 Galileo satellites
  - 32 tracking channels for all satellites in view
  - 5 correlators per channel for urban canyon robustness
  - Multibit signal processing hardware
- Advanced power management
  - Separated power islands for ultra low power mode
  - Dynamic core frequency scaling
  - 512-Byte embedded SRAM for back-up
- System infrastructure
  - LP DDR/DDR2 controller: 16/32-bit data 512 MB addressable (333 MHz DDR2, 200 MHz LPDDR)
  - One bank of 32 KB embedded SRAM
  - 64-channel vector interrupt controller (VIC)
  - 2 DMA controllers, 16 physical channels
  - 32 DMA request for each controller
  - Two external DMA requests are supported
- Display and graphics
  - Color LCD controller for STN,TFT or HR-TFT panels with 24-bit parallel RGB interface
  - Integrated touch screen controller and ADC
  - 3D advanced graphics acceleration
  - Video input port (VIP) interface
  - JPEG baseline profile decoder
- High throughput interfaces
  - 2 ports USB 2.0 OTG with integrated physical layers
  - 3 SD/MMC up to 8 bit data, all bootable



TFBGA372+100 (16x16x1.2mm)

- Audio interfaces and features
  - Four multichannel serial ports (I2S/TDM)
  - SPDIF input interface
  - C3 hardware reed-solomon decoder
  - Sample rate converter
- Standard interfaces
  - Four 16-bit input capture/output compare
  - Pulse width light modulator (PWL)
  - Four autobaud UART
  - Three I^2C multimaster/slave interfaces
  - Two synchronous serial port (SSP, SPI)
  - Smartcard interface
  - 160 GPIO over 5 32-bit ports
- Two controllers area network (CAN) in automotive versions
- Programmable voltage IOs: 1.8 V, 2.5 V, 3.3 V
- V_{DDIO_ON}: 1.8 ±10%V, V_{DD_ON}: V_{DD}, 1.25 ±3%V
- TFBGA 372+100 0.65 mm pitch package, packing in tray
- Ambient temperature range: -40 / +85 °C

Table 1. Device summary

Order code	Grade	CPU freq.	CAN
STA2065N2	Consumer	533 MHz	No
STA2065P2	Consumer	624 MHz	No
STA2065Z2	Consumer	754 MHz	No
STA2065A2	Automotive	533 MHz	2x
STA2065X2	Automotive	624 MHz	2x
STA2065Y2	Automotive	754 MHz	2x

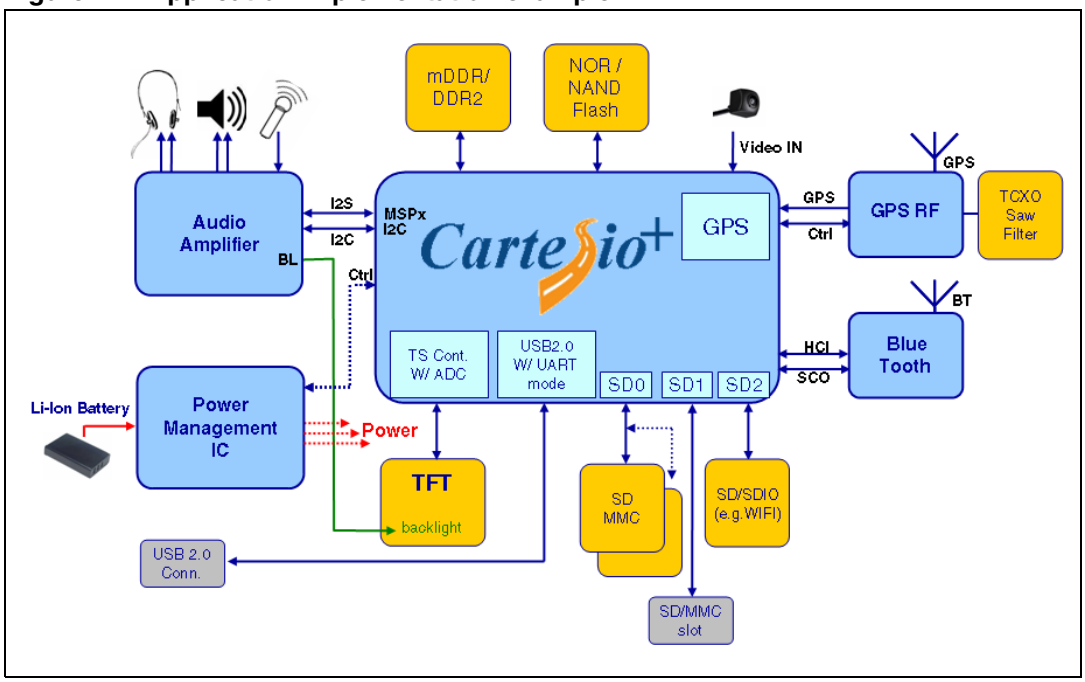
Contents

1 Description

STA2065 is a highly integrated SOC application processor combining host capability with high performance embedded GPS.

STA2065 targets vehicle head units and mobile navigation (PND), telematics, infotainment, advanced audio and connectivity systems. The STA2065 provides all the elements that are essential to build a cost effective solution.

Figure 1. Application implementation example



2 System block diagram description

The STA2065 comprises the following functional blocks:

2.1 MCU

ARM1176-JZF Advanced Risc Machine CPU up to 624 MHz (with V_{DD} greater or equal to 1.20V and under process and temperature worst case conditions).

2.2 Embedded memories

2.2.1 Embedded SRAM (eSRAM)

The embedded SRAM is 8K x 32 (32 KByte).

2.3 System functions

2.3.1 System and reset controller (SRC)

This provides a control interface for clock generation components external to the subsystem. It also controls system-wide and peripherals-specific energy management features.

2.3.2 PMU

The Power Manager module controls the SLEEP to DEEP-SLEEP modes transition, controls the external voltage switches on the V_{DD} and V_{DDIO}, monitors the external power supply (via two signals, VDDOK and BATOK), can force the emergency entry of the SDRAM in self-refresh, and controls the wake-up from DEEP-SLEEP mode.

2.3.3 DMA

Direct memory access can be used with DMA peripherals. FIFO fill/empty requests from these peripherals can be serviced immediately by the DMA Controller without CPU interaction. Peripheral-to-peripheral and memory-to-memory DMA are also supported. STA2065 features two DMA engines. Each DMA supports up to 8-channels and up to 32 requests.

2.3.4 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts.

2.3.5 GPIOs

Five GPIO ports provide 160 programmable inputs or outputs that can be controlled in two modes:

- software mode through an APB bus interface
- hardware mode through a hardware control interface

2.3.6 Real time clock (RTC)

The RTC provides a one second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed ‘alarm’ time is reached. It has a clock trimming feature to compensate the drift of the 32.768 kHz crystal.

2.3.7 Real time timer (RTT)

The RTT has the possibility of being clocked off. This reduces the always_on domain consumption during Deep Sleep. By default the RTT has its clock enabled.

2.3.8 Always_ON supply

The “Always_ON” domain retains its two separate supplies, one for the core logic (V_{DD_ON}) and one for the IOs (V_{DDIO_ON}).

The V_{DD_ON} supply is equal to V_{DD} during normal operation.

2.3.9 Enhanced function timer (EFT)

STA2065 features 4 16-bit EFTs. Each of the four EFT timers has a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

2.3.10 Watchdog timer (WDT)

This OS resource is used to trigger a system reset in the event of software failure.

2.4 Memory interfaces

2.4.1 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) supports, with two chip selects:

- ROM
- Static RAM
- NOR type flash memories, not multiplexed
- NOR type flash memories, multiplexed

It also supports, with two additional separate chip selects:

- NAND type flash memories, SLC small or large page
- NAND type flash memories, MLC

For NAND type of memories, the FSMC has been enhanced to implement an error correction in hardware, based on the Bose-Chaudhuri-Hocquenghem (BCH) code, able to correct up to 8-bit over 512 bytes+syndrome. The BCH code will calculate, in hardware, the syndrome only. The actual correction will be implemented through S/W intervention.

2.4.2 SD/MMC

STA2065 features two SD/SDIO/MMC interfaces up to 52 MHz / 8-bit. The main clock available to the peripherals is:

- PLL2CLK/13 (when PLL2CLK is 624 MHz and SRC_MMC52 = 0, 48 MHz will be generated)
- PLL2CLK/12 (when PLL2CLK is 624 MHz and SRC_MMC = 1, 52 MHz will be generated)
- PLL2CLK/9 (when PLL2CLK is 432 MHz, 48 MHz will be generated)

The peripheral is compliant to the following standards:

- MMC 4.4
- SD 2.0/Part 1 - Physical Layer
- SD 2.0/Part E1 - SDIO Specification

2.4.3 DDR-SDRAM controller

The SDRAM controller has been designed to support up to 1Gbit over each of the two chip selects (or up to 2 Gbit over a single chip select) of:

- LP DDR-SDRAM
- DDR2

The memory data bus will be 16 or 32-bit wide for LP DDR-SDRAM memories (under software control). This same configuration is also supported for DDR2 type of memories.

2.4.4 Smart card interface

STA2065 features a Smart Cart interface compliant to the standard ISO7816-3.

STA2065 supports 3.0 V or 1.8 V type of Cards.

2.5 Audio/video functions

2.5.1 C3

It is composed of CD-ROM Decoder Block, responsible for performing sector de-scrambling and 3rd level of error correction embedded in the sector specific to CD-ROM mode1 and XA Form1, and Data Filter block supporting frame data filtering and different block layout organization possibilities. The C3 block can take its input data directly from SPDIF or from the memory space, and delivers back its output data to memory, supporting DMA requests.

2.5.2 Sample rate converter (SaRaC)

This block offers a fully digital stereo asynchronous sample rate conversion, using an automatic Digital Ratio Locked Loop. Its main features are:

- Up to 20-bit input and 22-bit output sample size
- DMA optimized 16-bit stereo sample interface
- Input sample rate from selectable MSP or SPDIF interface (32 kHz to 48 kHz)
- Output sample rate from selectable MSP interface (44.1 kHz to 48 kHz)
- Internally generated input sample rate (8 kHz to 48 kHz) for compressed audio decoding

2.5.3 JPEG decoder

The JPEG decoder block performs Baseline DCT sequential decoding up to 16Mpix/sec. JPEG compressed thumbnails are also supported.

2.5.4 Video input

STA2065 has a Video Input Port. The VIP allows to grab images from external devices, supporting parallel CCIR-656 interface up to 80 MHz.

This block can be used in camera mode with an imaging co-processor or a CVBS video decoder to store pixel information into system memory. It can be also used in raw mode to directly store raw data from an external sensor.

2.5.5 Smart graphics accelerator (SGA)

The Smart Graphic Accelerator (SGA) provides an efficient 2D and 3D primitive drawing tool that breaks down the Mips and power consumption concerns of pixel processing.

2.5.6 Color LCD controller (CLCD)

This interface (18-bit parallel RGB) drives LCD panels. It supports single or dual-panel color and monochrome STN displays and color TFT or HR-TFT displays. The resolution can be 1, 2 or 4 bit-per-pixel (bpp) palletized for mono STN, 1, 2, 4 or 8 bpp palletized for color STN and TFT, 16-bpp true-color non palletized for Color STN and TFT, 24-bpp packed or not packed true color non pallettized for color TFT. It also offers Frame Modulation to deliver enhanced colors on 12, 16 or 18 bits (HR-) TFT panels from up to 24-bpp format.

2.6 Communication interfaces

2.6.1 USB

STA2065 embeds one USB2.0 OTG high-speed interface named USB0 featuring:

- High-speed signalling rate at 480 Mbit/s
- Support for full-speed (12 Mbit/s) signaling bit rate
- Support for session request protocol (SRP) and host negotiation protocol (HNP)
- Up to 7 bidirectional endpoints plus control endpoint 0
- 8192 bytes maximum FIFO dimension
- Dynamic FIFO allocation

USB0 is equipped with a built-in USB 2.0 HIGH-SPEED / OTG PHY, while USB1 is equipped with both an USB 2.0 FULL-SPEED PHY and a standard ULPI interface able to connect to an external Single Date Rate PHY.

With the goal of reducing the BOM cost for the customer, the USB 2.0 PHY also supports this additional muxing scheme:

- the USB D- wire is used as either the USB D- signal or UARTn transmit data signal
- the USB D+ wire is used as either the USB D+ signal or the UARTn receive data signal

2.6.2 UART

STA2065 features four Autobaud UARTs. One offers all modem control/status signals. They are enhanced versions of the industry-standard 16C550 UART.

2.6.3 I^2C

The I^2C controller is an interface designed to support the physical and data link layer according to I^2C standard revision 2.1 (January 2000). The I^2C bus is a 2-wire serial bus that provides a low-cost interconnection between ICs. STA2065 features three I^2C interfaces.

2.6.4 MSP

The multichannel serial port (MSP) is a synchronous receive and transmit serial interface. STA2065 features three MSPs.

2.6.5 SSP

STA2065 features two SSPs up to 24Mbit/sec for synchronous serial communication with external peripherals. SPI, MicroWire, T.I. and mono-directional protocols are supported with programmable word length up to 32 bits.

2.6.6 SPDIF

This interface takes SPDIF as input and extracts data and other channel information encrypted in SPDIF Frame format as per IEC958 standards. Data can be transferred to memory, using DMA support, or directly to C3 decoder without CPU intervention. SPDIF block supports up to 2X data streams.

2.6.7 AC97 controller

AC97 audio controller enables SOC to control external AC97 CODECs using SOC AMBA interconnect. It is implemented in a way to minimize audio data handling by SOC processor with dedicated audio DMA engine. AC97 Audio Controller supports AC97 revision 2.3 compliant audio CODECs. External interface supports one external AC97 CODEC with 6 output (3 of them can be Double Rate Audio) and 3 input channels.

2.6.8 CAN

STA2065 features one CAN module that is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

2.7 Specific functions

2.7.1 GPS

STA2065 integrates HPGPS_G2, ST's proprietary GPS IP, which is ST's 2nd generation High-Sensitivity Baseband. The Baseband is fully compliant with GPS and Galileo L1/E1 signal specifications, and is optimized to maximize sensitivity for both acquisition and tracking in difficult environments. Please refer to GPS solution specifications and software release notes for more specific performance details.

The baseband accepts a 3-bit signal at a 4MHz IF from its companion RF chip, the STA5630. It down-converts this to baseband and feeds it to the acquisition engines (for up to 8 satellites simultaneously) and the tracking channels (for up to 32 satellites simultaneously).

The highly parallel correlators in the acquisition engines identify each satellite signal in time and frequency domains, and the results are passed to the tracking channels. The tracking channels fine-tune the lock, then track continuously, providing orbit data and timing measurements to the ARM CPUs.

The management of the hardware for these operations, and the myriad of complex conditions that arise, is performed in a complete GPS software library supplied by ST. This library also takes the resultant measurement data and processes it to maintain satellite databases and calculate the user's position, velocity and time (PVT) solutions.

The PVT solution, and other useful data, is made available to the user's application via an API in the ST GPS library. This runs on a royalty-free real-time kernel (OS20), with ports to industry-standard operating systems also available. In stand-alone mode, the outputs are generated in standard NMEA message format.

Options are also available in the software library to support ST Self-Trained Assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with Autonomous Ephemeris prediction when no network is available, and with simple download when a network is available followed by prediction for the following 7 days.

The GPS subsystem is based on an ARM966 processor and is clocked by two clocks:

- MCLK: ARM966 CPU clock
- RFCLK: 16f0 or 32f0, from RF chip

MCLK is derived from the PLL2 clock with a divisor from 3 to 16, giving an ARM966 operating frequency in the range from 208 to 39 MHz, in the case the PLL2 is running at 624

MHz. The same divisor will be from 2 to 16 when the PLL2 is running at 432 MHz, giving an operating frequency in the range from 216 to 27 MHz.

The GPS baseband clock will be derived from the MCLK clock with a divider, internal to the subsytem, by 1, 2,3 or 4, under ARM11 control. RFCLK is the clock received from the RF front-end chip.

2.7.2 Touchscreen controller/ADC

STA2065 embeds a 4-wire Touch Screen Controller. The Touch Screen Controller main characteristics are:

- Active Window Clip
- Movements Tracking
- 12-bit SAR ADC resolution when used for Touch screen (with averaging)
- Measurement oversampling from 2 to 8
- Up to 128 coordinates FIFO, with programmable FIFO threshold
- ADC minimum conversion time of 1 µs
- Capability to support 2 additional analog inputs for auxiliary functions like battery voltage monitoring and accessory control.

The ADC of the Touch Screen Controller can be also used for the conversion of external analog signals. In this case the ADC has a 10-bit resolution (its native resolution).

2.7.3 Multisupply IO ring

STA2065 has multivoltage IOs capable of supporting 1.8 V, 2.5 V or 3.3 V interfaces. The rings are defined as follows:

a) All peripherals with exception of what belongs to other rings
b) LCD
c) DRAM
d) FSMC
e) MMC1 (GPIO40-47, GPIO76-82), CAN0

The default voltages applied to each ring will be:

a) 1.8V
b) 1.8V
c) 1.8V
d) 1.8V
e) 3.3V

The “Always ON” ring remains separated as in the current STA2065 and supplied by V_{DDIO_ON}.

Note: For 1.8V and 3.3V IO interfaces, pads are compensated across temperature and voltage variations but for 2.5V interface, pads are not compensated.

2.7.4 Driving strength and slew rate programmability

- The IO Driving Strength is programmable for the following interfaces as follows:
- SD/MMC0 (4, 6, 8 mA) (default 8mA)
- SD/MMC1 (4, 6, 8 mA) (default 8mA)
- SD/MMC2 (4, 6, 8 mA) (default 8mA)
- LCD (4, 8 mA) (default 8mA)
- DRAM (weak 70W, strong 50W) (default strong, 50W)
- FSMC (4, 8 mA) (default 8mA)

The Slew Rate is also controllable for the following interface as follows:

- SD/MMC0 (Nominal, Fast) (default Nominal slew rate)
- SD/MMC1 (Nominal, Fast) (default Nominal slew rate)
- SD/MMC2 (Nominal, Fast) (default Nominal slew rate)
- LCD (Nominal, Fast) (default Fast slew rate)
- FSMC (Nominal, Fast) (default Fast slew rate)
- DRAM (200, 266, 333 MHz) (default 200 MHz)
- ULPI (Nominal, Fast) (default Fast slew rate)
- MSP0 (Nominal, Fast) (default Nominal slew rate)
- MSP1 (Nominal, Fast) (default Nominal slew rate)

3 System features introduction

In this chapter, an introduction to the main STA2065 system features is given. These will be explained in detail later in this document.

3.1 Power region partition

STA2065 is a device targeted to a wide range of applications, starting from handheld battery powered devices thanks to an optimized power management but also addressing in dash automotive power requirements thanks to its flexible multi-voltage IO.

Three main power regions are identified:

- V_{DD_ON}: It is the core voltage that powers the RTC (Real Time Clock), the PMU (Power Management Unit), SRC (System Clock and Reset controller) and the Backup RAM of STA2065. V_{DD_ON} remains usually powered even when the device is in DEEP-SLEEP mode. For this reason, the static power consumption of this region stays below 20µA worst case.
- V_{DD}: It is the core voltage that powers the overall chip (apart from the IOs). This voltage is not applied in very low power state condition. When applied, the V_{DD_ON} and V_{DD} are at the same voltage. A maximum of 10% variation between the two regions is required.
- V_{DDIO}: It is the power region dedicated to the IOs. The overall IOs are divided in seven groups and each of them can be powered at different, independent voltages. Some groups may have specific constraints in terms of power voltage range in order to meet specific electrical characteristics compliant to some standards; some of these groups are, for example, in the DDR interface and the 1.1 embedded USB transceiver. There is also a group of IOs called V_{DDIO_ON} that identifies the IOs that must be always powered (also in the lowest power consumption state of STA2065) in order to make the wake-up possible. The other five regions (called also V_{DDIOX}) cannot be powered while in this state. For more information, please refer to *Chapter 3.6: IO groups on page 17*

3.2 Frequency region partition

STA2065 is designed so that there are two PLLs. PLL1 generates clock frequencies for the ARM core and the internal buses, while the PLL2 generates clock frequencies for each peripheral kernel and also for each peripheral interface. This means that each peripheral receives the clock derived from the PLL1 at its internal interface, then it works with the clock derived from the PLL2. Despite the use of two PLLs, a single system clock input or a single external crystal is needed (in addition to the RTC clock (or crystal)).

3.3 Frequency and power range

The core voltage range is 1.25 ±4% V while the IO voltage ranges are 1.8±10% V, 2.5 ±10% V and 3.3 ±10% V

Table 2 shows some use cases of STA2065 in NORMAL mode:

Table 2. Frequency and power use cases

V_{dd} and V_{dd_on} (V)	Core Freq [MHz]	Bus Freq [MHz]	DDR Freq [MHz]	Sync/Async [S/A]
1.2 5(±4%)	624	208	312	A, DDR2
1.2 5(±4%)	624	156	156	S
1.2 5(±4%)	624	124.8	124.8	S
1.2 5(±4%)	533	177.67	177.67	S
1.2 5(±4%)	533	133.25	133.25	S
1.2 5(±4%)	533	177.67	312	A, DDR2
1.2 5(±4%)	520	208	130	A
1.2 5(±4%)	520	173.34	173.34	S
1.2 5(±4%)	520	130	130	S
1.2 5(±4%)	520	208	312	A, DDR2
1.2 5(±4%)	494	197.6	197.6	S
1.2 5(±4%)	494	164.67	164.67	S
1.2 5(±4%)	494	123.5	123.5	S
1.2 5(±4%)	494	208	329.34	A, DDR2

The background of *Table 2* is the maximization of data throughput on the DRAM interface, matching the currently available DRAM speed grades: 133 MHz, 166 MHz and 200 MHz (LP DDR) and 333 MHz (DDR2). Regardless of the memory speed grade it is possible to program the ARM core, the internal bus and the DDR to run at different speeds than the ones mentioned in *Table 2*. The ARM bus clock and the bus clock are derived from the same common source (VCO of the PLL1) but are asynchronous each other. The DDR frequency can be the same (synchronous) or derived with a different pre-scaling (1, 2, 3, 4, 5, 6, 8, 9 or 10) from the VCO of PLL1 or PLL2 (asynchronous configuration).

STA2065 embeds a complete GPS subsystem where both gate logic and dedicated DSP work together. There are specific constraints in this subsystem in terms of minimum frequency in order to guarantee the target GPS specifications.

In the lowest power consumption state possible, only V_{DD_ON} is powered and the target current drawn is 20 µA. In this state, the clock is not running and the current leakage is mainly due to the Backup memory. The 20 µA current limit has to be considered with Process best (leakage worst case condition), V_{DD_ON} 1.3V (1.25V plus 4% tolerance) and Junction Temperature 50°C (considering, while in this state, the ambient temperature is equal to the junction temperature).

3.4 Power states

The following power states are defined:

- **OFF**: V_{DD_ON} and V_{DD} are not applied (all data in the backup RAM is lost): no data retention is kept in the SDRAM
- **NORMAL**: Each peripheral runs at its nominal speed with the possibility of turning off all the unused peripherals (peripheral kernel clock gated)
- **SLOW**: PLL1 bypassed. ARM and bus runs at crystal clock. PLL2 runs at its nominal speed. PLL1 can be optionally put in power down
- **DOZE**: It is like SLOW mode with the ARM running either at 19 MHz or 32 KHz
- **STANDBY**: This power mode is achieved through software configuration of the Normal mode. PLLs run at their nominal speed. ARM1176 is in WFI (Wait For Interrupt) state and its clock is automatically gated off.
- **DEEP-SLEEP**: V_{DD} powered off. V_{DD_ON} powered (RTC, few GPIOs, backup RAM) and clocked at 32 KHz making the wakeup possible. The context is put, optionally, in the external SDRAM if they are in self refresh mode. Only the V_{DD} and V_{DDIO_ON} regions must be powered
- **SLEEP**: It is like the DEEP-SLEEP mode, with the difference that V_{DD} and V_{DDIO} are also applied and the PLLs are off (optional for PLL2)

While in NORMAL, SLOW AND STANDBY, V_{DD_ON} and V_{DD} are the same (10% tolerance between them) and cannot be changed. Also the power to the several IO groups is kept unchanged.

In order to change the V_{DD_ON} and V_{DD} values, the system has to transit to either OFF, SLEEP, DEEP-SLEEP and then back to the selected state.

In order to keep the power consumption as low as possible, the target voltage mentioned in DEEP-SLEEP is considered at 1.0V.

A dedicated FSM manages the power state transitions among NORMAL, SLOW, DOZE AND SLEEP. All other states mentioned above are SW variants of the ones managed by the FSM.

Table 3 shows the summary of the power states supported by STA2065.

Table 3. Power mode states

Power State	32kHz	PLL1	PLL2	V_{DD_ON}	V_{DD}	IOs
OFF	off	off	off	off	off	off
NORMAL	on	on	on	= V_{DD}	1.2V to 1.3V (1.25V typ)	1.7 to 3.6V
SLOW	on	Off. Bypassed by main oscillator	off (SW can take it on)	= V_{DD}	1.2V to 1.3V (1.25V typ)	1.7 to 3.6V
DOZE	on	Off. Bypassed by 32 kHz	off (SW can take it on)	= V_{DD}	1.2V to 1.3V (1.25V typ)	1.7 to 3.6V
STANDBY	on	on (clk gated) ARM in WFI	on (clk gated)	= V_{DD}	1.2V to 1.3V (1.25V typ)	1.7 to 3.6V

Table 3. Power mode states (continued)

Power State	32kHz	PLL1	PLL2	V_{DD_ON}	V_{DD}	IOs
SLEEP	on	off	off (SW can take it on)	= V_{DD}	1.2V to 1.3V (1.25V typ)	1.7 to 3.6V
DEEP-SLEEP	on	off	off	1.2 to 1.3V (1.25V typ)	off	Refer *section 3.5*

3.5 System wakeup and power down

Typically the system using STA2065 will never be powered off, even when the user switches the device off using the main power switch. The main power switch works in a way that puts the device in DEEP-SLEEP mode. In this state, the only blocks within STA2065 that are powered are the RTC, PMU, PWL, SRC and the backup RAM; at system level, only the V_{DD_ON} is powered.

The following wakeup methods are possible:

- The user presses a button on the unit that causes all of the main power supplies to start. After an appropriate delay, the processor's reset line is lifted and allows the code to start executing.
- The internal alarm feature triggers a dedicated signal that will cause all of the main supplies to start. After an appropriate delay, the processor's reset line is lifted and allows the code to start execution.

Considering the above mentioned wakeup system, while in DEEP-SLEEP, some dedicated IO lines must be powered:

- POR (input)
- POWEREN (output)
- VDDOK and BATOK (input)
- WAKE (input)
- 32KHz xtal (SXTALI and SXTALO)
- OSC32KOUT (output)

In order to keep the external DRAM in self refresh while in DEEP-SLEEP, CKE of the DRAM must be kept low. Since all the IOs are not powered in DEEP-SLEEP, in order to make the self refresh working, an external pulldown resistor is needed.

3.6 IO groups

V_{DDIO} is split into the following groups:

- V_{DDIO_ON} [a]
- V_{DDIOx} (This is split into 5 types: V_{DDIOA}, V_{DDIOB}, V_{DDIOC}, V_{DDIOD}, V_{DDIOE})
- V_{USBPHY} (USB 2.0 HS PHY transceiver)

The IO supply type and corresponding pads details are as follows:

- V_{DDIO_ON}: Power Supply pins for the IO buffers of the always ON section. It supplies POR, PWREN, VDDOK, BATOK, WAKE, SXTALI, SXTALO, OSC32KOUT.
- V_{DDIOA}: Power Supply pins for the IO buffers. It supplies most GPIOs, dedicated pads for JTAG, MMC0 and GPS and dedicated pads for test (SCANEN, TAPSEL).
- V_{DDIOB}: Power Supply pins for the IO buffers. Supplies to the CLCD IOs.
- V_{DDIOC}: Power Supply pins for the IO buffers. Supplies the Synchronous Dynamic Memory Controller (SDMC) IOs.
- V_{DDIOD}: Power Supply pins for the IO buffers. Supplies the following IOs: GPIO9, GPIO48:50, GPIO64:67, GPIO83:127 (FSMC).
- V_{DDIOE}: Power Supply pins for the IO buffers. Supplies the following IOs: CAN, MSP, GPIOs related to SD/MMC1 functionality.
- V_{USBPHY}: 3.3 V ±10% USB PAD power supply (it can be derated to 1.8 V in UART over USB mode and 1.8V signalling is desired).
- V_{DDTSC}: 3.3 V Touchscreen PAD power supply

a. VDDIO_ON is always 1.8V.

4 Package information

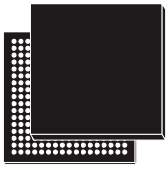
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 2. TFBGA372+100 (16x16x1.2mm) mechanical data and package dimensions

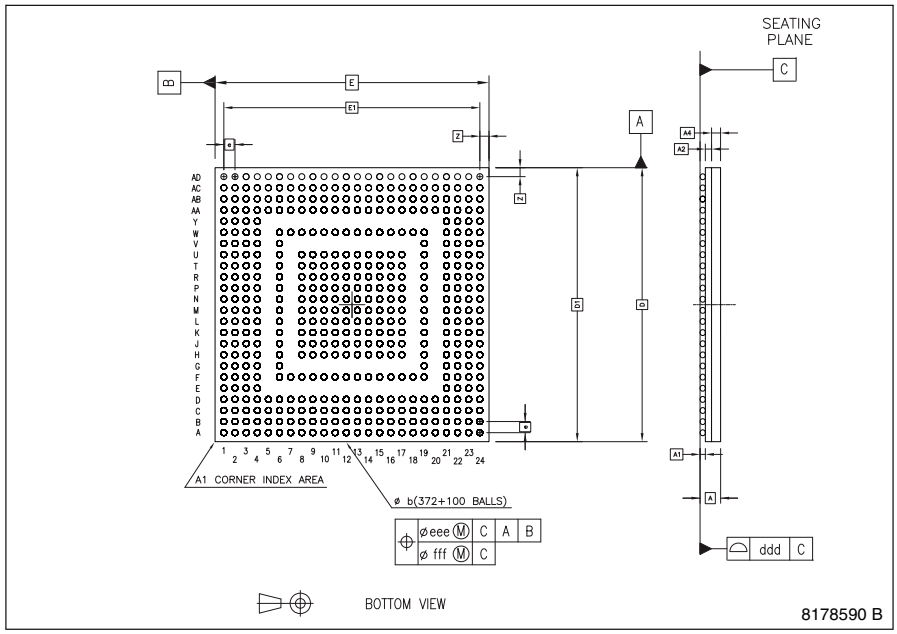
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.0472
A1						
A2		0.300			0.0118	
A4			0.600			0.0236
b	0.300	0.350	0.420	0.0118	0.0138	0.0165
D		16.000			0.6299	
D1		14.950			0.5886	
E		16.000			0.6299	
E1		14.950			0.5886	
e		0.650			0.0256	
Z		0.530			0.0209	
ddd			0.150			0.0059
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 16 x 16 x 1.2mm, pitch 0.65mm

TFBGA372+100
Thin profile **F**ine Pitch **B**all **G**rid **A**rray



GAPGPS01959

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
23-Jul-2009	1	Initial release.
13-Oct-2009	2	Updated features list on page 1.
19-Oct-2009	3	Updated “High throughput interfaces” feature on cover page.
15-Oct-2012	4	Updated *Table 1: Device summary on page 1*.
20-Sep-2013	5	Updated disclaimer.

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