Elektronische Bauelemente

SSD20P15-295D

-10.7A, -150V, $R_{DS(ON)}$ 295mΩ

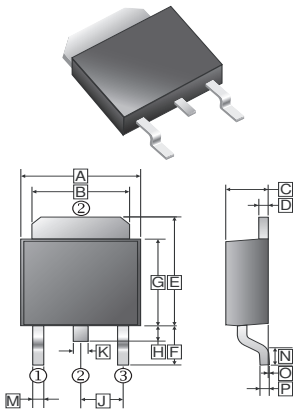
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process.Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making thisdevice ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

TO-252(D-Pack)



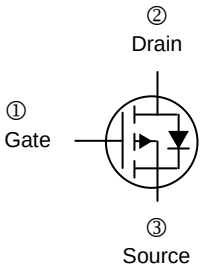
REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	6.4	6.8	J	2.30 REF.	
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Miniature TO-252 surface mount package saves board space.
- High power and current handling capability.

PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13' inch



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25℃	I_D	-10.7	A
Pulsed Drain Current [2]		I_{DM}	-60	A
Continuous Source Current (Diode Conduction) [1]		I_S	-42.6	A
Total Power Dissipation [1]	T_C=25℃	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ 175	℃
Thermal Resistance Ratings				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	40	℃ / W
Maximum Thermal Resistance Junction-Case		$R_{\theta JC}$	3	℃ / W

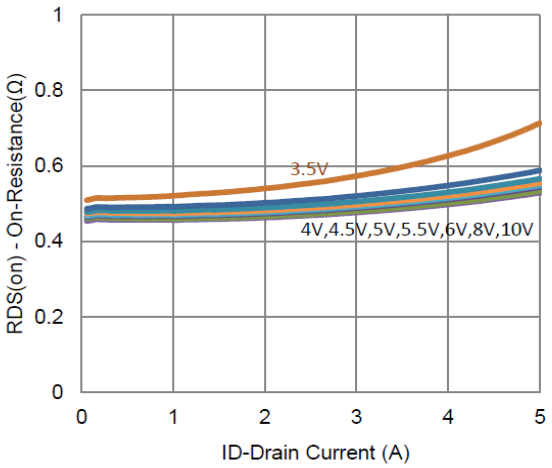
Notes：
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

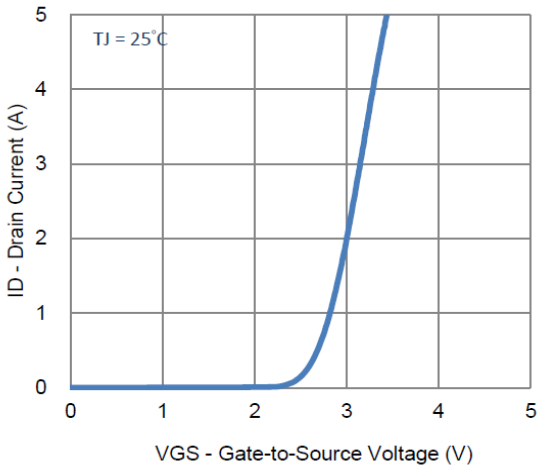
Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	V_{DS}= V_{GS}, I_D= -250μA
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -120V, V_{GS}=0
		-	-	-25		V_{DS}= -120V, V_{GS}=0, T_J=55℃
On-State Drain Current [1]	$I_{D(on)}$	-10	-	-	A	V_{DS}= -5V, V_{GS}= -10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	295	mΩ	V_{GS}= -10V, I_D= -5A
		-	-	580		V_{GS}= -5.5V, I_D= -4A
Forward Transconductance [1]	g_{fs}	-	22	-	S	V_{DS}= -15V, I_D= -5A
Diode Forward Voltage	V_{SD}	-	-1.03	-	V	I_S= -21.3A, V_{GS}=0
Dynamic [2]						
Input Capacitance	C_{iss}	-	1080	-	pF	V_{DS}= -15V V_{GS}=0 f=1MHz
Output Capacitance	C_{oss}	-	98	-		
Reverse Transfer Capacitance	C_{rss}	-	71	-		
Total Gate Charge	Q_g	-	6	-	nC	I_D= -5A V_{DS}= -75V V_{GS}= -4.5V
Gate-Source Charge	Q_{gs}	-	2.4	-		
Gate-Drain Charge	Q_{gd}	-	2.8	-		
Turn-On Delay Time	$T_{d(on)}$	-	8	-	nS	V_{DS}= -75V I_D= -5A V_{GEN}= -10V R_L=15Ω R_G=6Ω
Rise Time	T_r	-	18	-		
Turn-Off Delay Time	$T_{d(off)}$	-	54	-		
Fall Time	T_f	-	77	-		

Notes:
1. Pulse test：PW ≦ 300μs duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.

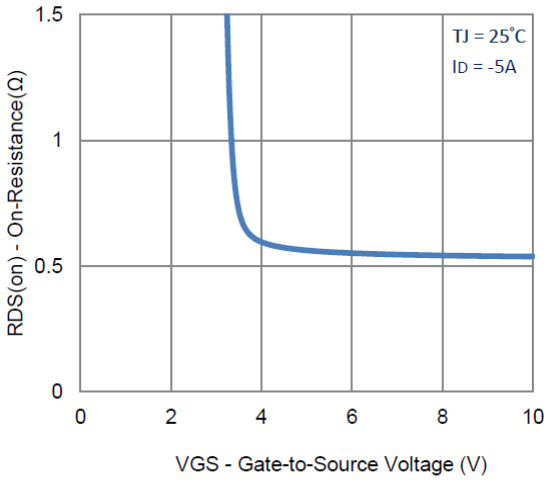
CHARACTERISTIC CURVES



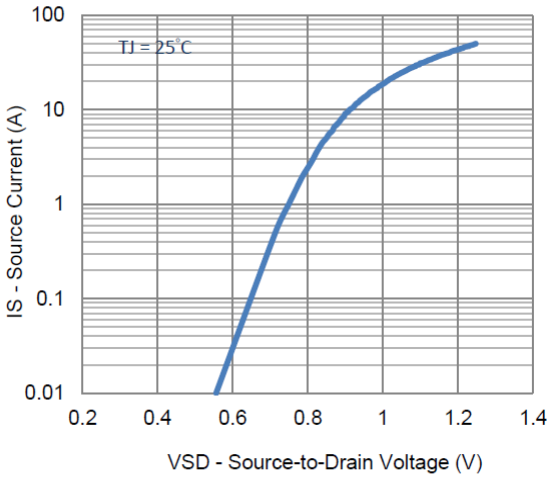
1. On-Resistance vs. Drain Current



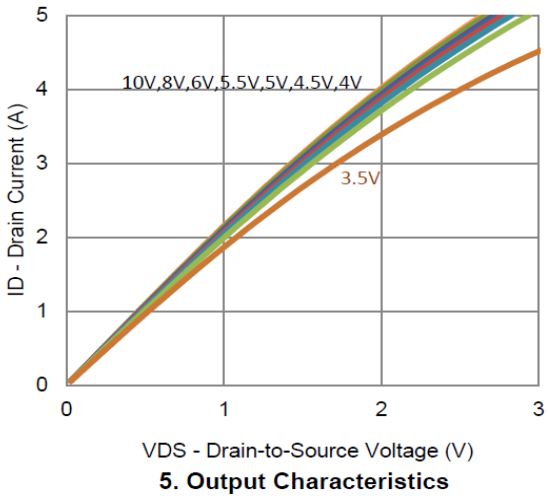
2. Transfer Characteristics



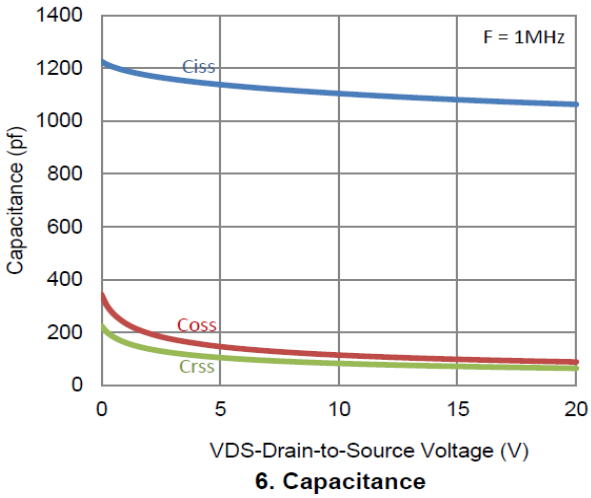
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

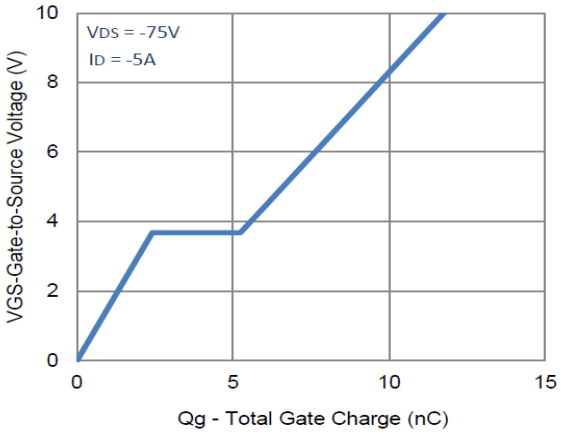


5. Output Characteristics

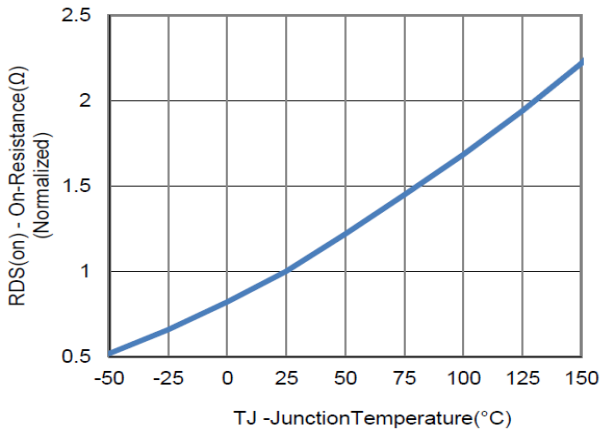


6. Capacitance

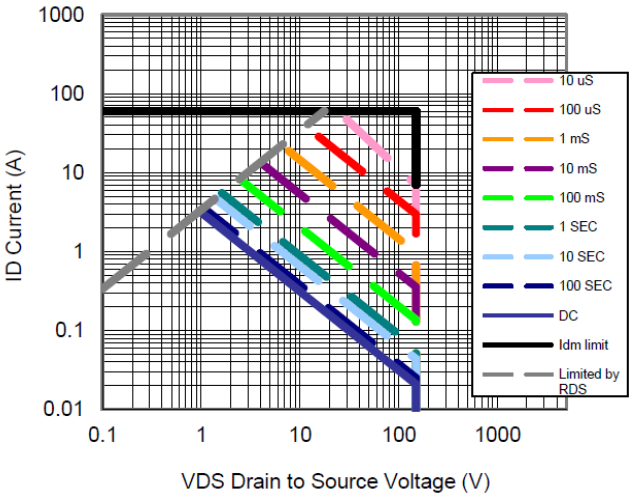
CHARACTERISTIC CURVES



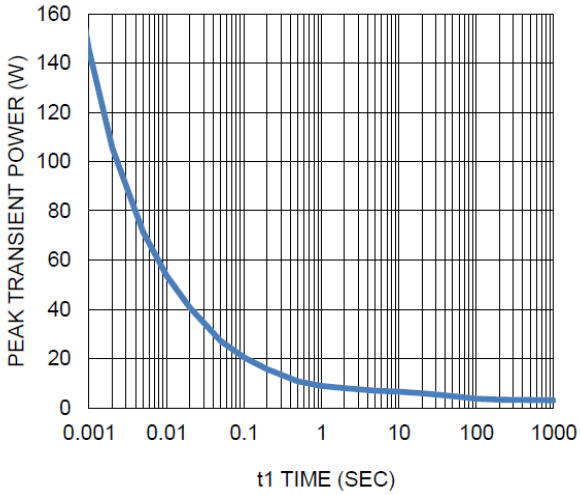
7. Gate Charge



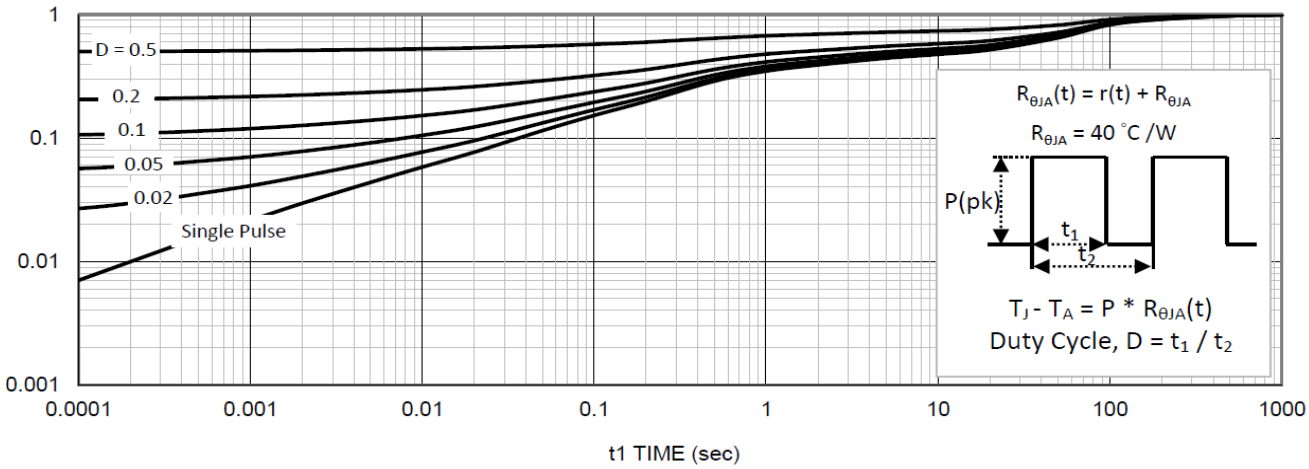
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area



10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient