❑ MN103SD3 Series

Type	MN103SD3P	MN103SFD3R
Internal ROM type	Mask ROM	FLASH
ROM (byte)	640K	1024K
RAM (byte)	40K	64K
Package (Lead-free)	LQFP100-P-1414	
Minimum Instruction Execution Time	16.7 ns (at 2.7 V to 3.6 V, 60 MHz)	

■ Interrupts

RESET. IRQ × 8. NMI. Timer × 32. I²C × 3. SIF × 16. DMA × 12. WDT. A/D. Time base timer × 2. System error. Key input. Remote control × 4

■ Timer Counter

8-bit timer A × 10

Reload-down count. Cascade connection possible (usable as a 16-bit to 32-bit timer)

8-bit timer B × 3

Interval timer. Event count. Square-wave output. Simple pulse width measurement. PWM output

16-bit timer × 6

Up-down count. Input capture. PWM output. Compare/capture register 2 channnels

Time base timer × 1

Watchdog timer × 1

■ Serial interface

UART/Synchronous/Multi-master I²C interface selective × 3

UART/Synchronous interface selective × 5

■ Remote Contorol Interface

Remote control reception: Correspondence with AEHA (Association for Electric Home Appliances) format. Queued reception by low speed clock

■ DMA controller

Number of channels: 4 channels

Unit of transfer: 8/16/32 bits

Maximum transfer cycles: 65535

Starting factor: External interrupt. Timer. Serial transmission/reception. A/D conversion finish. I²C transmission/reception. Software. Remote control data reception

Transfer method: 2-bus cycle transfer

Adressing modes: Fixed. Increment. Decrement

Transfer mode: Word transfer. Burst transfer. Intermittent transfer

■ I/O Pins

I/O 81 : Common use

Input 1 : Common use

■ A/D converter

10-bit × 8 channels

■ ROM Correction

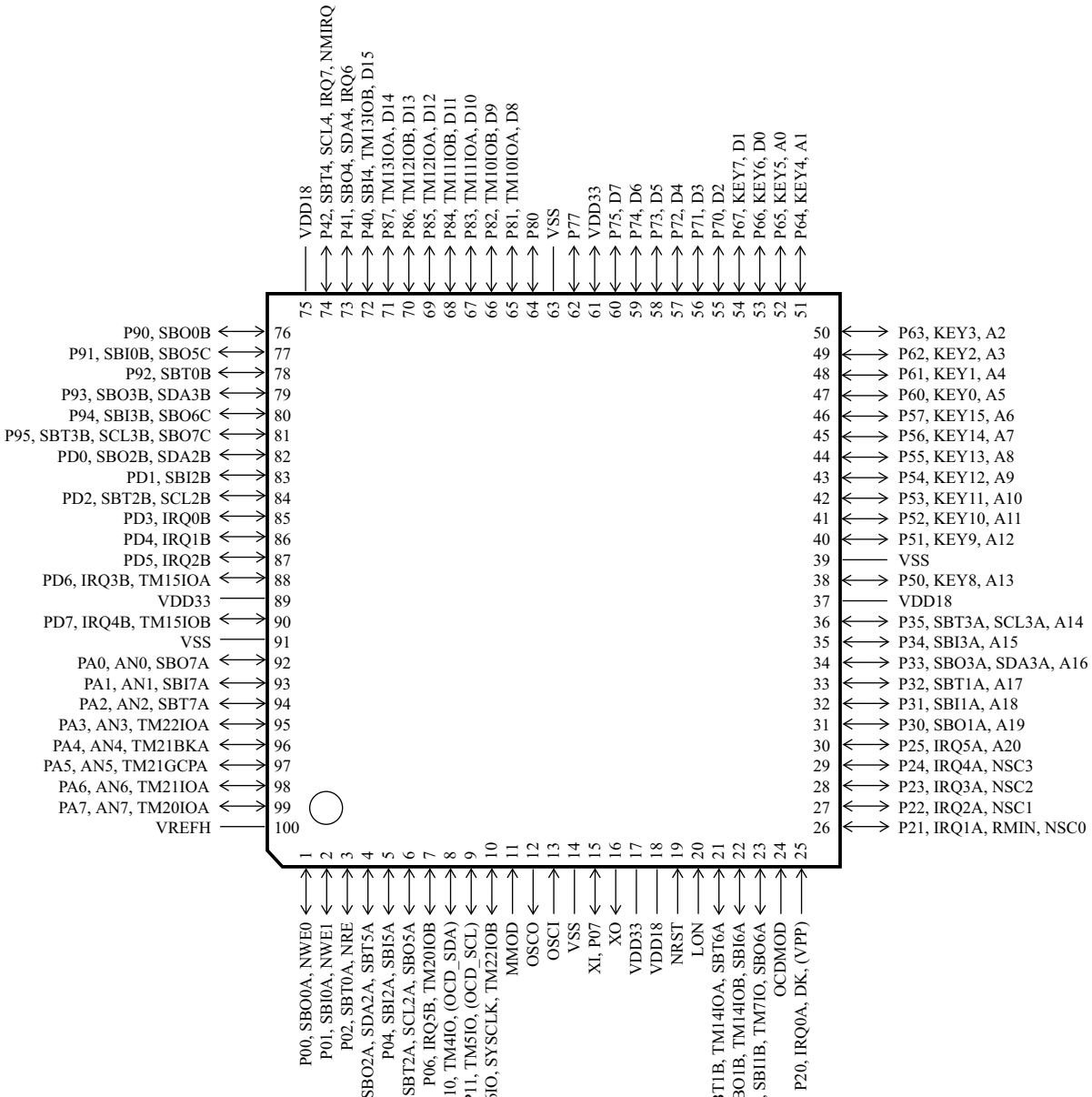
8 channels

■ Electrical Charactreistics (A/D converter characteristics)

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
Non-linear error		VDD33 = VREFH = 3.3 V. VSS = 0 V			±4	LSB
Differential non-linearity error					±4	LSB

■ Pin Assignment

LQFP100-P-1414



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