ML7033

Dual-Channel Line Card CODEC

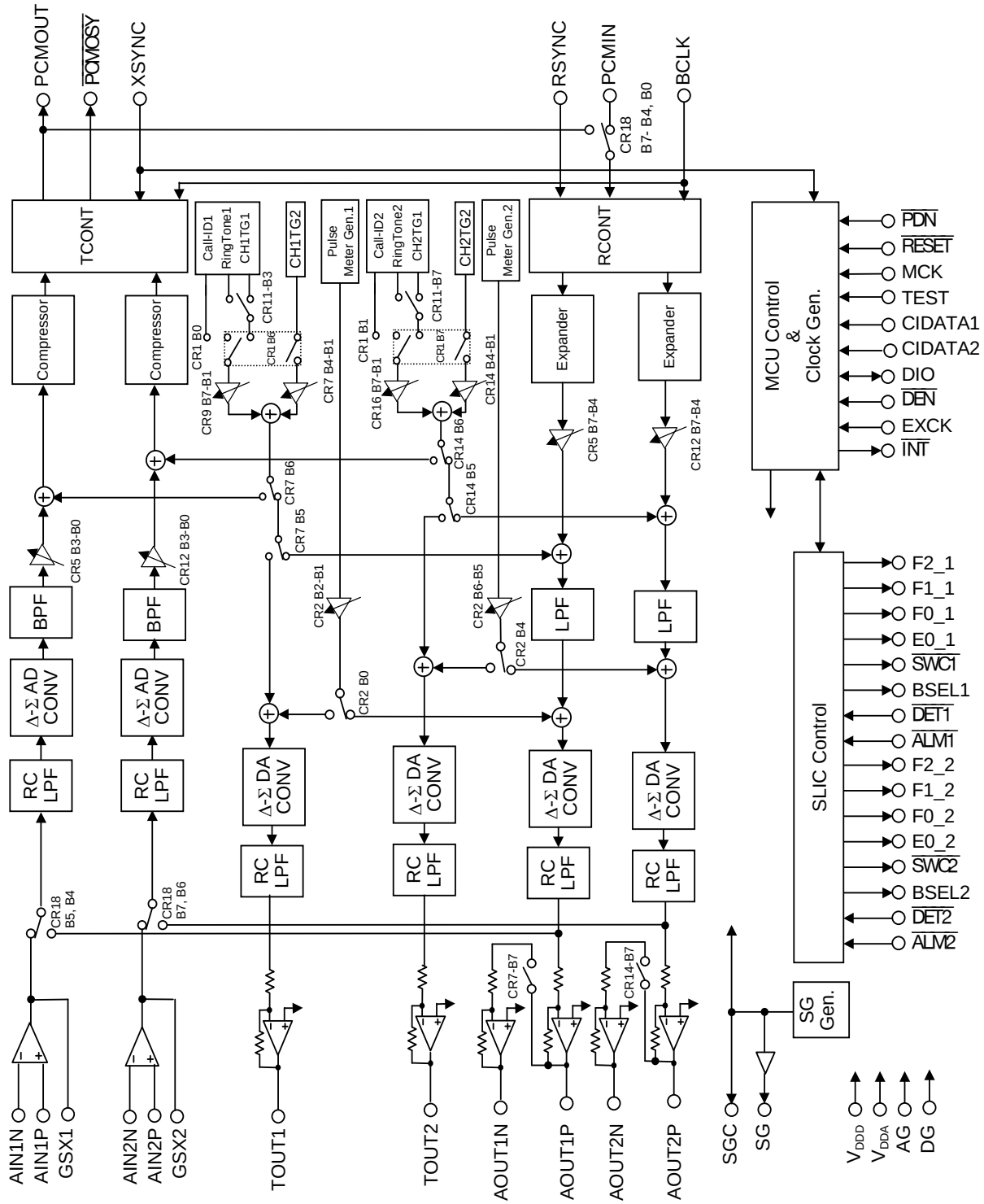
GENERAL DESCRIPTION

The ML7033 is a 2-channel PCM CODEC CMOS IC designed for Central Office (CO) and Customer Premise Equipment (CPE) environments. The ML7033 device contains 2-channel analog-to-digital (A/D) and digital-to-analog (D/A) converters with multiplexed PCM input and output. The ML7033 is designed for single-rail, low power applications. The high integration of the ML7033 reduces the number of external components and overall board size. The ML7033 is best suited for line card applications and provides an easy interface to subscriber line interface circuits (SLIC's), in particular the Intersil RSLIC™ series.

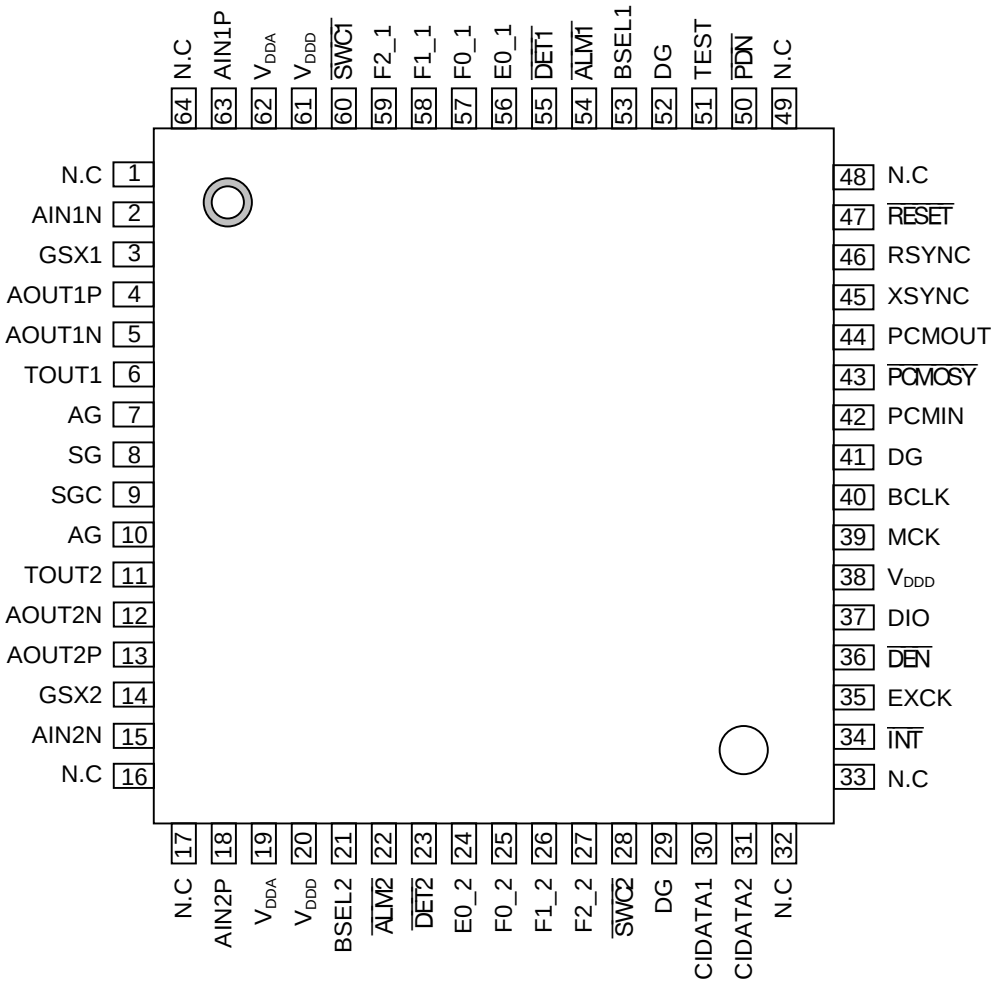
FEATURES

- Seamlessly interfaces with Intersil RSLIC™ series devices
- Single 5 volt power supply (4.75 V to 5.25 V)
- Δ-Σ ADC and DAC
- PCM format: μ-law/A-law (ITU-T G.711 compliant), 14-bit linear (2's complement)
- Optional wideband filter for V.90 data modem applications
- Low power consumption
  - 2-channel operating mode: 115 mW (typical) 180 mW (max)
  - 1-channel operating mode: 80 mW (typical) 115 mW (max)
  - Power-down mode: 0.1 mW (typical) 0.25 mW (max); PDN pin = logic "0"
- Power-on reset
- Dual programmable tone generators (300 Hz to 3400 Hz; 10 Hz intervals; 0.1 dB intervals)
  - Call progress tone, DTMF tone
- Ringing tone generator (15 Hz to 50 Hz; 1Hz intervals; 0.1 dB intervals)
- Pulse metering tone generator (12 kHz, 16 kHz; gain level selectable)
- Call ID tone generator (ITU-T V.23, Bell 202)
- Analog and digital loop back test modes
- Time-slot assignment
- Serial MCU interface
- Master clock: 2.048 MHz/4.096 MHz selectable
- Serial PCM transmission data rate: 256 kbps to 4096 kbps
- Adjustable transmit/receive gain (1 dB intervals)
- Built-in reference voltage generator
- Differential or single-ended analog output selectable
- Package: 64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Ordering Part number: ML7033GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	N.C	—	(Leave unconnected)
2	AIN1N	I	CH1 Transmit Op-amp Input Negative
3	GSX1	O	CH1 Transmit Op-amp Output
4	AOUT1P	O	CH1 Receive Output Positive
5	AOUT1N	O	CH1 Receive Output Negative
6	TOUT1	O	CH1 Tone Output
7	AG	—	Analog Ground
8	SG	O	Signal Ground for External Circuit
9	SGC	O	Signal Ground for Internal Circuit
10	AG	—	Analog Ground
11	TOUT2	O	CH2 Tone Output
12	AOUT2N	O	CH2 Receive Output Negative
13	AOUT2P	O	CH2 Receive Output Positive
14	GSX2	O	CH2 Transmit Op-amp Output
15	AIN2N	I	CH2 Transmit Op-amp Input Negative
16	N.C	—	(Leave unconnected)
17	N.C	—	(Leave unconnected)
18	AIN2P	I	CH2 Transmit Op-amp Input Positive
19	V_{DDA}	—	Power Supply for Internal Analog Circuit
20	V_{DDD}	—	Power Supply for Internal Digital Circuit
21	BSEL2	O	Output for SLIC2 Battery Select
22	$\overline{\text{ALM2}}$	I	Input from SLIC2 Thermal Shut Down Alarm Detector
23	$\overline{\text{DET2}}$	I	Input from SLIC2 Switch Hook, Ground Key or Ring Trip Detector
24	E0_2	O	Output for SLIC2 Detector Mode Selection
25	F0_2	O	Mode Control Output to SLIC2 F0
26	F1_2	O	Mode Control Output to SLIC2 F1
27	F2_2	O	Mode Control Output to SLIC2 F2
28	$\overline{\text{SWC2}}$	O	Output for SLIC2 Uncommitted Switch Control
29	DG	—	Digital Ground
30	CIDATA1	I	Call ID Data Input for CH1
31	CIDATA2	I	Call ID Data Input for CH2
32	N.C	—	(Leave unconnected)
33	N.C	—	(Leave unconnected)
34	$\overline{\text{INT}}$	O	Interrupt Output (from SLIC status)
35	EXCK	I	MCU Interface Data Clock Input
36	$\overline{\text{DEN}}$	I	MCU Interface Data Enable Input
37	DIO	I/O	MCU Interface Control Data Input/Output

Pin	Symbol	Type	Description
38	V_{DDD}	—	Power Supply for Internal Digital Circuit
39	MCK	I	Master Clock (2.048/4.096 MHz)
40	BCLK	I	PCM Data Shift Clock
41	DG	—	Digital Ground
42	PCMIN	I	PCM Data Input
43	$\overline{\text{PCMOSY}}$	O	PCM Data Output Indicator for Time-Slot Assignment
44	PCMOUT	O	PCM Data Output
45	XSYNC	I	Transmit Synchronizing Clock Input
46	RSYNC	I	Receive Synchronizing Clock Input
47	$\overline{\text{RESET}}$	I	Reset for Control Register
48	N.C	—	(Leave unconnected)
49	N.C	—	(Leave unconnected)
50	$\overline{\text{PDN}}$	I	Power-down Control
51	TEST	I	LSI Manufacturer's Test Input (keep logic "0")
52	DG	—	Digital Ground
53	BSEL1	O	Output for SLIC1 Battery Select
54	$\overline{\text{ALM1}}$	I	Input from SLIC1 Thermal Shut Down Alarm Detector
55	$\overline{\text{DET1}}$	I	Input from SLIC1 Switch Hook, Ground Key or Ring Trip Detector
56	E0_1	O	Output for SLIC1 Detector Mode Selection
57	F0_1	O	Mode Control Output to SLIC1 F0
58	F1_1	O	Mode Control Output to SLIC1 F1
59	F2_1	O	Mode Control Output to SLIC1 F2
60	$\overline{\text{SWC1}}$	O	Output for SLIC1 Uncommitted Switch Control
61	V_{DDD}	—	Power Supply for Internal Digital Circuit
62	V_{DDA}	—	Power Supply for Internal Analog Circuit
63	AIN1P	I	CH1 Transmit Op-amp Input Positive
64	N.C	—	(Leave unconnected)

Note: In this datasheet, "1" and "2" in names for pins which respectively exist for CH1 and CH2 are often substituted by "n" (in a small letter).

Ex) GSX1, GSX2 → GSXn
AOUT1N, AOUT2N → AOUTnN
$\overline{\text{DET1}}$, $\overline{\text{DET2}}$ → $\overline{\text{DETn}}$

Control Register Assignment

Register	Address					Data								R/W
	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	0	0	Filter2 SEL	Filter1 SEL	MCK SEL	SHORT	LIN	ALAW	MODE1	MODE0	R/W
CR1	0	0	0	0	1	CH2TG ON	CH1TG ON				CID FMT	CID CH2ON	CID CH1ON	R/W
CR2	0	0	0	1	0	PMG2 FRQ	PMG2 LV1	PMG2 LV0	PMG2 TOUT2	PMG1 FRQ	PMG1 LV1	PMG1 LV0	PMG1 TOUT1	R/W
CR3	0	0	0	1	1	TSAE	TSAC	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0	W
CR4	0	0	1	0	0	DET2 TIM3	DET2 TIM2	DET2 TIM1	DET2 TIM0	DET1 TIM3	DET1 TIM2	DET1 TIM1	DET1 TIM0	R/W
CR5	0	0	1	0	1	LV1R3	LV1R2	LV1R1	LV1R0	LV1X3	LV1X2	LV1X1	LV1X0	R/W
CR6	0	0	1	1	0	F2_1	F1_1	F0_1	SWC1	BSEL1	E0_1	DET1*	ALM1*	R/W
CR7	0	0	1	1	1	AOUT1 SEL	CH1TG2 TX	CH1TG2 TOUT1	CH1TG2 LV3	CH1TG2 LV2	CH1TG2 LV1	CH1TG2 LV0	CH1TG2 _8	R/W
CR8	0	1	0	0	0	CH1TG2 _7	CH1TG2 _6	CH1TG2 _5	CH1TG2 _4	CH1TG2 _3	CH1TG2 _2	CH1TG2 _1	CH1TG2 _0	R/W
CR9	0	1	0	0	1	CH1TG1 LV6	CH1TG1 LV5	CH1TG1 LV4	CH1TG1 LV3	CH1TG1 LV2	CH1TG1 LV1	CH1TG1 LV0	CH1TG1 _8	R/W
CR10	0	1	0	1	0	CH1TG1 _7	CH1TG1 _6	CH1TG1 _5	CH1TG1 _4	CH1TG1 _3	CH1TG1 _2	CH1TG1 _1	CH1TG1 _0	R/W
CR11	0	1	0	1	1	CH2 RING	CH2TG1 TRP2	CH2TG1 TRP1	CH2TG1 TRP0	CH1 RI NG	CH1TG1 TRP2	CH1TG1 TRP1	CH1TG1 TRP0	R/W
CR12	0	1	1	0	0	LV2R3	LV2R2	LV2R1	LV2R0	LV2X3	LV2X2	LV2X1	LV2X0	R/W
CR13	0	1	1	0	1	F2_2	F1_2	F0_2	SWC2	BSEL2	E0_2	DET2*	ALM2*	R/W
CR14	0	1	1	1	0	AOUT2 SEL	CH2TG TX	CH2TG TOUT2	CH2TG2 LV3	CH2TG2 LV2	CH2TG2 LV1	CH2TG2 LV0	CH2TG2 _8	R/W
CR15	0	1	1	1	1	CH2TG2 _7	CH2TG2 _6	CH2TG2 _5	CH2TG2 _4	CH2TG2 _3	CH2TG2 _2	CH2TG2 _1	CH2TG2 _0	R/W
CR16	1	0	0	0	0	CH2TG1 LV6	CH2TG1 LV5	CH2TG1 LV4	CH2TG1 LV3	CH2TG1 LV2	CH2TG1 LV1	CH2TG1 LV0	CH2TG1 _8	R/W
CR17	1	0	0	0	1	CH2TG1 _7	CH2TG1 _6	CH2TG1 _5	CH2TG1 _4	CH2TG1 _3	CH2TG1 _2	CH2TG1 _1	CH2TG1 _0	R/W
CR18	1	0	0	1	0	CH2 LOOP1	CH2 LOOP0	CH1 LOOP1	CH1 LOOP0	TEST3	TEST2	TEST1	TEST0	R/W
CR19	1	0	0	1	1	TEST11	TEST10	TEST9	TEST8	TEST7	TEST6	TEST5	TEST4	R/W

*: Read only bit

Note: In this datasheet, numbers in names for control register bits are often substituted by “n” (in a small letter). In the case, the “n” does not always refer to a channel number.

Ex) MODE0, MODE1 → MODEn
CH1TG2_7, CH1TG2_6 → CH1TG2_n
PMG2FRQ, PMG1FRQ → PMGnFRQ

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	V_{DDD}, V_{DDA}	–0.3 to +7.0	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage to be fixed; V_{DDD}, V_{DDA}	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	—	–40	—	+85	°C
High Level Input Voltage	V_{IH}	All digital input pins	2.2	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	0.8	V
MCK Frequency	F_{MCK}	MCK = 2.048 MHz MCKSEL (CR0-B5) bit = “0”	–0.01%	2048	+0.01%	kHz
		MCK = 4.096 MHz MCKSEL (CR0-B5) bit = “1”	–0.01%	4096	+0.01%	kHz
BCLK Frequency	F_{BCLK}	BCLK	256	—	4096	kHz
Sync Pulse Frequency	F_{SYNC}	XSYNC, RSYNC	–0.01%	8	+0.01%	kHz
Clock Duty Ratio	D_{CLK}	MCK,BCLK	40	50	60	%
Digital Input Rise Time	t_{IR}	All digital input pins	—	—	50	ns
Digital Input Fall Time	t_{IF}		—	—	50	ns
MCK to BCLK Phase Difference	t_{MB}	MCK, BCLK	—	—	50	ns
Transmit Sync Pulse Setting Time	t_{XS}	BCLK to XSYNC	50	—	—	ns
	t_{SX}	XSYNC to BCLK	50	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLK to RSYNC	50	—	—	ns
	t_{SR}	RSYNC to BCLK	50	—	—	ns
Sync Pulse Width	t_{WS}	XSYNC, RSYNC SHORT (CR0-B4) bit = “0”	1 BCLK	—	125 μs –1BCLK	μs
		XSYNC, RSYNC SHORT (CR0-B4) bit = “0”	210	—	1BCLK	ns
PCMOUT Set-up Time	t_{DS}	PCMOUT	50	—	—	ns
PCMOUT Hold Time	t_{DH}	PCMOUT	50	—	—	ns
Digital Output Load	R_{DL}	Pull-up Resistor, PCMOUT	0.5	—	—	kΩ
	C_{DL1}	PCMOUT	—	—	50	pF
	C_{DL2}	Other output pins	—	—	50	pF
Bypass Capacitor for SGC	C_{SG}	SGC to AG	0.1	—	—	μF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	2CH Operating Mode, No Signal	—	23.0	35.0	mA
	I_{DD2}	1CH Operating Mode, No Signal	—	16.0	22.0	mA
	I_{DD4}	Power-down Mode $\overline{PDN}$ pin = logic "0"	—	25.0	50.0	μA
High Level Input Leakage Current	I_{IH}	All Digital Input Pins $V_I = V_{DD}$	—	0.1	5.0	μA
Low Level Input Leakage Current	I_{IL}	All Digital Input Pins V_I = 0 V	–5.0	–0.1	—	μA
Digital Output Low Voltage	V_{OL1}	$\overline{PCMOUT}$, Pull-up = 0.5 kΩ	0	0.2	0.4	V
	V_{OL2}	Other output pins, I_{OL} = –0.4 mA	0	0.2	0.4	V
Digital Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	2.5	—	—	V
Digital Output Leakage Current	I_O	$\overline{PCMOUT}$ High Impedance State	—	—	10	μA
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SG, SGC Output Voltage	V_{SG}	SGC to AG 0.1 μF	—	2.4	—	V
SG, SGC Rise Time	t_{SGC}	SGC to AG 0.1 μF Rise time to 90% of max. level	—	—	10	ms
SG Output Load Resistance	R_{LSG}	SG	10	—	—	kΩ

Transmit Analog Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AINnN, AINnP		—	10	—	MΩ
Output Load Resistance	R_{LGX}	GSXn		20	—	—	kΩ
Output Load Capacitance	C_{LGX}	(to SGC)		—	—	30	pF
Output Amplitude	V_{OGX}	*1		—	—	2.226	Vpp
Offset Voltage	V_{OSGX}		Gain = 1	–50	—	50	mV

*1 –3.0 dBm (600Ω) = 0 dBm0

Receive Analog Interface Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Load Resistance	R_{LAO}	AOUTnN, AOUTnP (to SGC)	20	—	—	kΩ
	R_{LTO}	TOUTn (to SGC)	10	—	—	kΩ
Output Load Capacitance	C_{LAO}	AOUTnN, AOUTnP, TOUTn	—	—	50	pF
Output Amplitude	V_{OAO}	AOUTnN, AOUTnP, TOUTn R_{LAO} = 20 kΩ (to SGC)	—	—	3.4*	Vpp
Offset Voltage	V_{OSAO}	AOUTnN, AOUTnP, TOUTn R_{LAO} = 20 kΩ (to SGC)	–100	—	100	mV

* 0.658 dBm (600Ω) = 0 dBm0

AC Characteristics

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)					
Transmit Frequency Response	Loss T1	60	0	GSXn to PCMOUT (Attenuation)	25	45	—	dB
	Loss T2	300			–0.15	0.15	0.20	
	Loss T3	1020			Reference			
	Loss T4	3000			–0.15	0.02	0.20	
	Loss T5	3300			–0.15	0.1	0.80	
	Loss T6	3400			0	0.6	0.80	
Receive Frequency Response	Loss R1	100	0	PCMIN to AOUTn (Attenuation)	–0.15	0.04	0.2	dB
	Loss R2	1020			Reference			
	Loss R3	3000			–0.15	0.07	0.2	
	Loss R4	3300			–0.15	0.2	0.8	
	Loss R5	3400			0	0.6	0.8	
Transmit Signal to Distortion Ratio	SDT1	1020	3	GSXn to PCMOUT *1	36	43	—	dB
	SDT2		0		36	40	—	
	SDT3		–30		36	38	—	
	SDT4		–40		30	32	—	
	SDT5		–45		25	29	—	
Receive Signal to Distortion Ratio	SDR1	1020	3	PCMIN to AOUTn *1	36	42	—	dB
	SDR2		0		36	39	—	
	SDR3		–30		36	39	—	
	SDR4		–40		30	33	—	
	SDR5		–45		25	30	—	
Transmit Gain Tracking	GTT1	1020	3	GSXn to PCMOUT	–0.2	0.02	0.2	dB
	GTT2		–10		Reference			
	GTT3		–40		–0.2	0.06	0.2	
	GTT4		–50		–0.6	0.4	0.6	
	GTT5		–55		–1.2	0.4	1.2	
Receive Gain Tracking	GTR1	1020	3	PCMIN to AOUTn	–0.2	0	0.2	dB
	GTR2		–10		Reference			
	GTR3		–40		–0.2	–0.02	0.2	
	GTR4		–50		–0.6	–0.1	0.6	
	GTR5		–55		–1.2	–0.2	1.2	

*1 C-message filter used

AC Characteristics (Continued)

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)					
Idle Channel Noise	$NIDLE_T$	—	—	Analog input = SGC[*1] AINn to PCMOUT Gain = 1 (μ-law)	—	9	15	dBm0
	$NIDLE_R$	—	—	PCMIN = 'FF'h (μ-law) PCMIN = 'D5'h (A-law) PCMIN = all '0' (linear)[*1] PCMIN to AOUTn	—	4	10	
Absolute Level (Initial Difference)	AV_T/AV_R	1020	0	GSXn to PCMOUT V_{DD} = 5 V, Ta = 25°C	0.511	0.548	0.587	Vrms
				PCMIN to AOUTn (Single-ended) V_{DD} = 5 V, Ta = 25°C	0.806	0.835	0.864	
Absolute Level (Deviation of Temperature and Power)	AV_{TT}			V_{DD} = 4.75 to 5.25 V Ta = –40 to 85°C	–0.3	—	0.3	dB
	AV_{RT}				–0.3	—	0.3	
Absolute Delay	T_D	1020	0	A to A Mode BCLK = 2048 kHz	—	0.58	0.6	ms
Transmit Group Delay	T_{GD} T1	500	0	*2	—	0.26	0.75	ms
	T_{GD} T2	600			—	0.16	0.35	
	T_{GD} T3	1000			—	0.02	0.125	
	T_{GD} T4	2600			—	0.05	0.125	
	T_{GD} T5	2800			—	0.07	0.75	
Receive Group Delay	T_{GD} R1	500	0	*2	—	0.00	0.75	ms
	T_{GD} R2	600			—	0.00	0.35	
	T_{GD} R3	1000			—	0.00	0.125	
	T_{GD} R4	2600			—	0.09	0.125	
	T_{GD} R5	2800			—	0.12	0.75	
Cross Talk Attenuation	CR_T	1020	0	Trans to Receive	75	83	—	dB
	CR_R			Receive to Trans	75	80	—	
	CR_{CH}			Channel to Channel	75	78	—	
Discrimination	DIS	4.6 to 72k	0	0 to 4 kHz	30	32	—	dB
Out of Band Spurious	OBS	300 to 3.4K	0	4.6 to 1000 kHz	—	–37.5	–35	dB
Signal Frequency Distortion	SFD_T	1020	0	0 to 4 kHz	—	–50	–40	dBm0
	SFD_R				—	–48	–40	
Intermodulation Distortion	IMD_T	fa = 470 fb = 320	–4	2 fa – fb	—	–50	–40	dBm0
	IMD_R				—	–54	–40	
Power Supply Noise Rejection Ratio	PSR_{T1}	0 to 4k	100 mVrms	*3	40	44	—	dB
	PSR_{T2}	4 to 50k			50	55	—	
	PSR_{R1}	0 to 4k			40	45	—	
	PSR_{R2}	4 to 50k			50	56	—	

*1 C-message filter used
*2 Minimum value of the group delay distortion
*3 Under idle channel noise

AC Characteristics (Continued)

(V_{DD} = 4.75 to 5.25 V, Ta = –40 to +85°C)

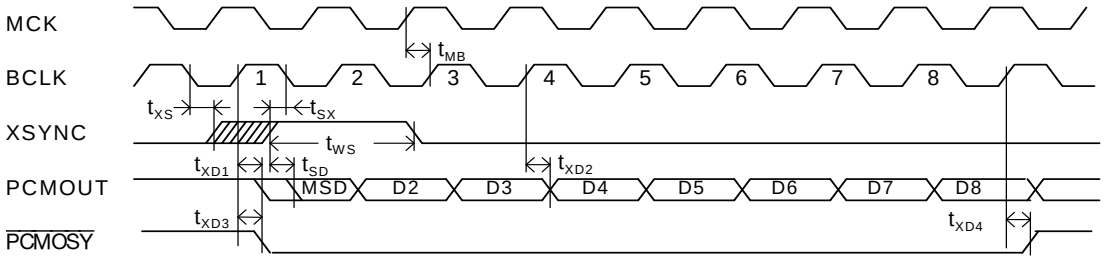
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SD}	PCMOUT Pull-up resister = 0.5 kΩ C_L = 50 pF and 1 LSTTL	—	—	100	ns
	t_{XD1}		—	—	100	
	t_{XD2}		—	—	100	
	t_{XD3}	$\overline{PCMOSY}$, C_L = 50 pF	—	—	100	ns
	t_{XD4}		—	—	100	
PCMOUT Operation Delay Time	t_{DDO}	Time to operation after Power-down release	—	4	—	ms
AOUTn/TOUTn Signal Output Delay Time	t_{DAO}	Time to baseband signal output after power-on	—	4	—	ms
Serial Port I/O Setting Time	t_1	C_{LOAD} = 50 pF	50	—	—	ns
	t_2		50	—	—	ns
	t_3		50	—	—	ns
	t_4		50	—	—	ns
	t_5		100	—	—	ns
	t_6		50	—	—	ns
	t_7		50	—	—	ns
	t_8		—	—	50	ns
	t_9		20	—	—	ns
	t_{10}		20	—	—	ns
	t_{11}		—	—	50	ns
	t_{12}		—	—	3.5(*4)	ns
			5.0(*4)	—	—	
EXCK Clock Frequency	f_{EXCK}	EXCK	0.5	—	10	MHz
SLIC Interface Delay Time	t_{20}		—	—	200	ns
	t_{21}		—	20	—	µs
	t_{22}		—	—	200	ns
	t_{23}		—	—	200	ns
	t_{24}		—	—	225	ms

*4 Don't raise the DEN in the range (3.5ns to 5.0ns) delayed from falling edge of the 12th EXCK.

TIMING DIAGRAM

Transmit Timing - 8-bit PCM Mode with LIN (CR0-B3) bit = "0"

Long Frame Sync Mode with SHORT (CR0-B4) bit = "0"



Short Frame Sync Mode with SHORT (CR0-B4) bit = "1"

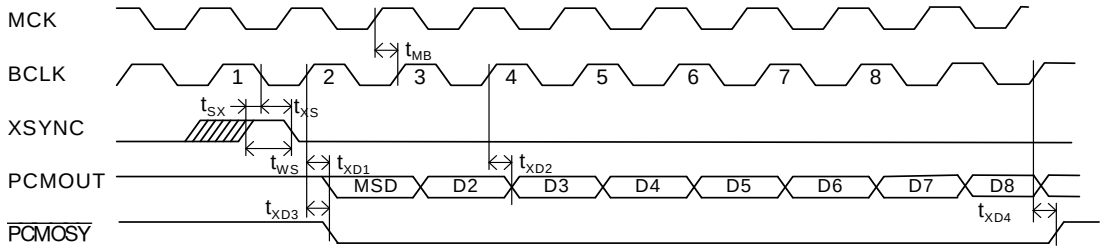
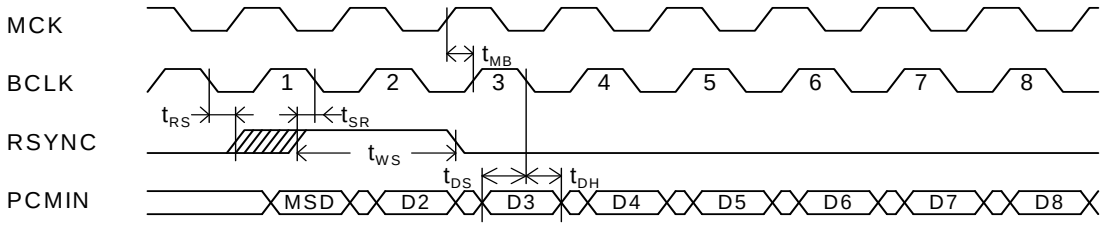


Figure 1 Transmit Side Timing Diagram

Receive Timing - 8-bit PCM Mode with LIN (CR0-B3) bit = "0"

Long Frame Sync Mode with SHORT (CR0-B4) bit = "0"



Short Frame Sync Mode with SHORT (CR0-B4) bit = "1"

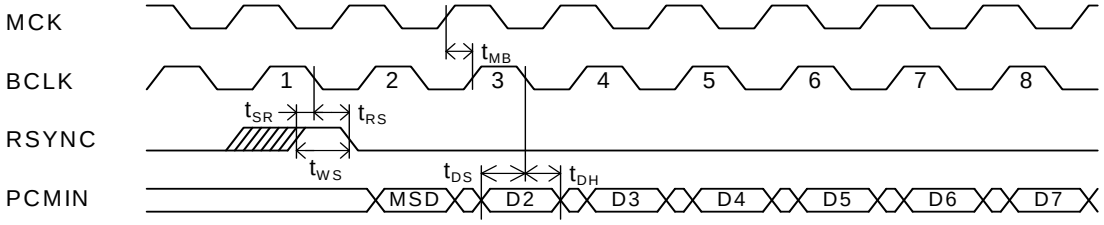
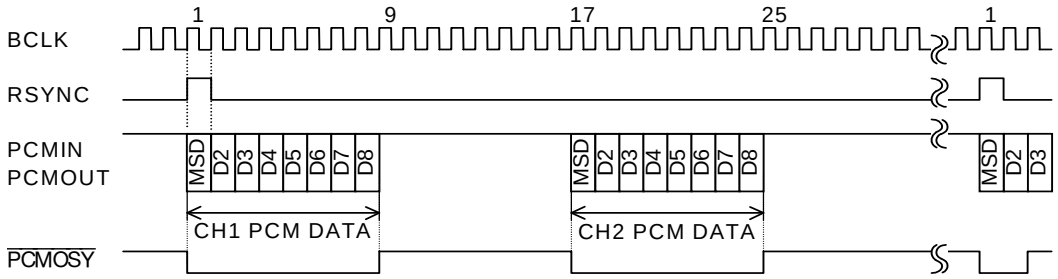


Figure 2 Receive Side Timing Diagram

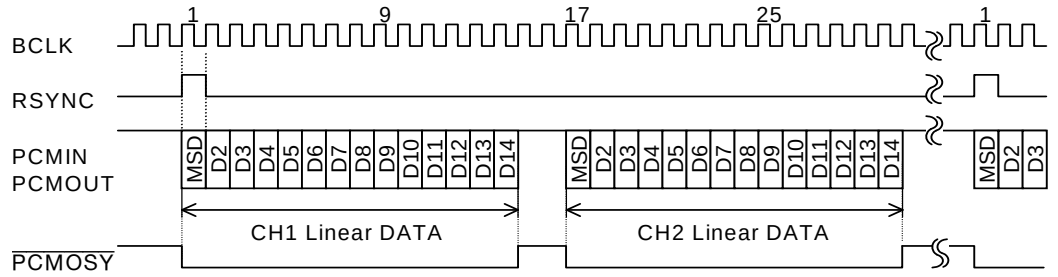
Note: The above timings are also valid in 14-bit linear PCM Mode with the LIN (CR0-B3) bit = "1", except that the number of data bits on the PCMIN and PCMOUT signals changes from 8 to 14.

PCM Interface Bit Configuration

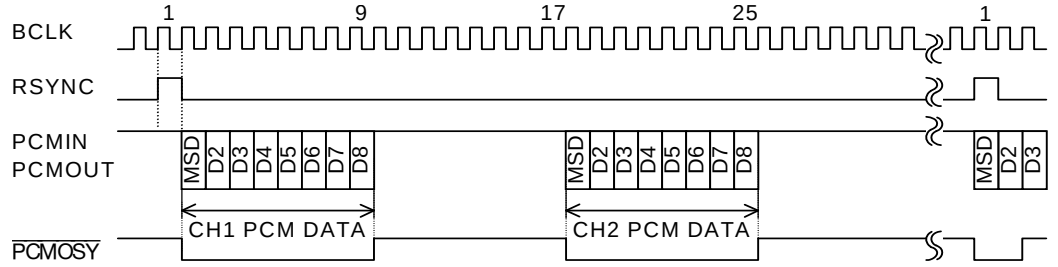
8-bit PCM Mode with LIN (CR0-B3) bit =”0” & Long Frame Sync Mode with SHORT (CR0-B4) bit = “0”



14-bit Linear PCM Mode with LIN (CR0-B3) bit = ”1” & Long Frame Sync Mode with SHORT (CR0-B4) bit = “0”



8-bit PCM Mode with LIN (CR0-B3) bit = “0” & Short Frame Sync Mode with SHORT (CR0-B4) bit = “1”



14-bit Linear PCM Mode with LIN (CR0-B3) bit = “1” & Short Frame Sync Mode with SHORT (CR0-B4) bit = “1”

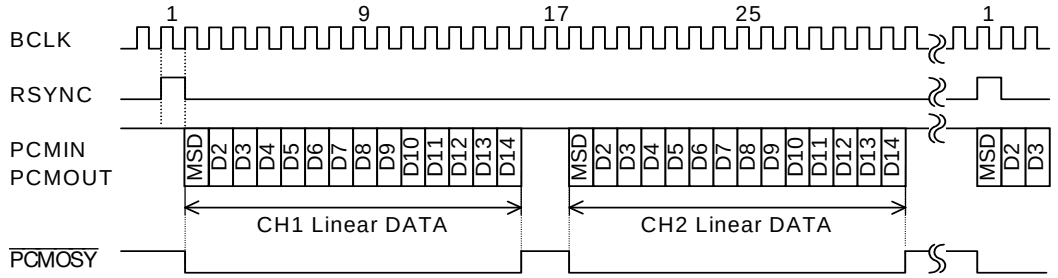


Figure 3 PCM Interface Bit Configuration

SGC, PCMOUT, and AOUT Output Timing

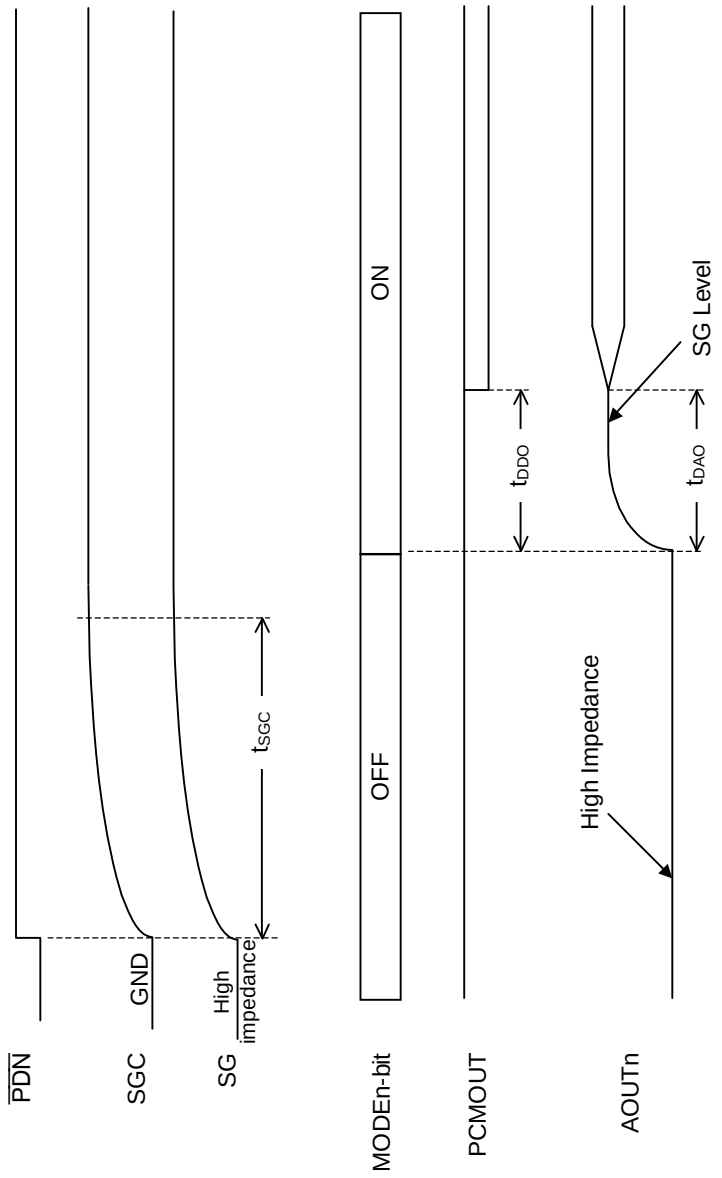


Figure 4 SGC, PCMOUT, and AOUT Output Timing

MCU Serial Interface

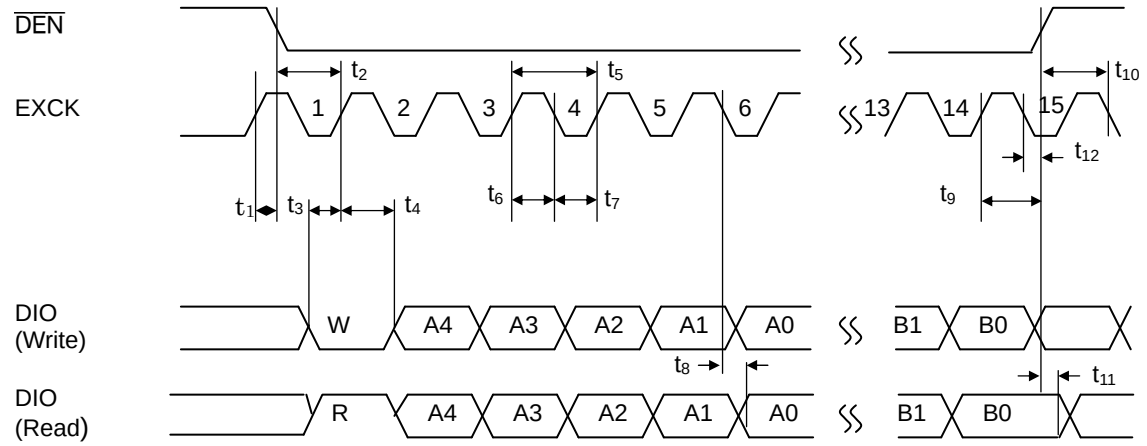
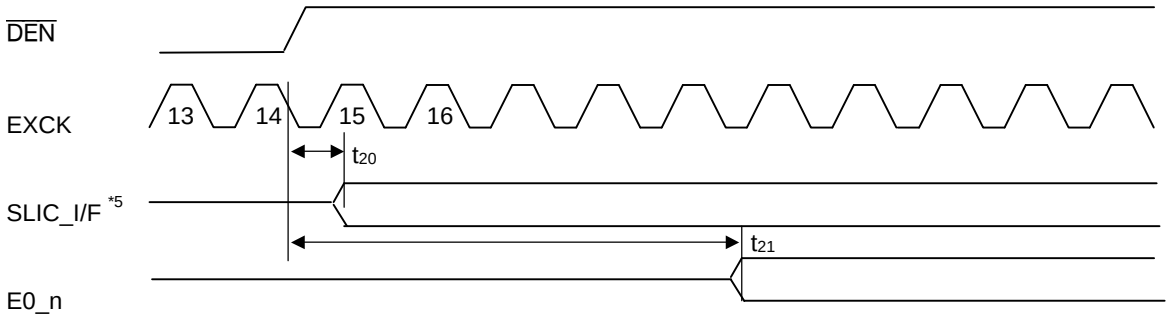


Figure 5 MCU Serial Interface

SLIC Interface



*5 SLIC_I/F = F2_n pin, F1_n pin, F0_n, SWCn pin, BSELn pin

Figure 6 SLIC Interface 1 (to SLIC)

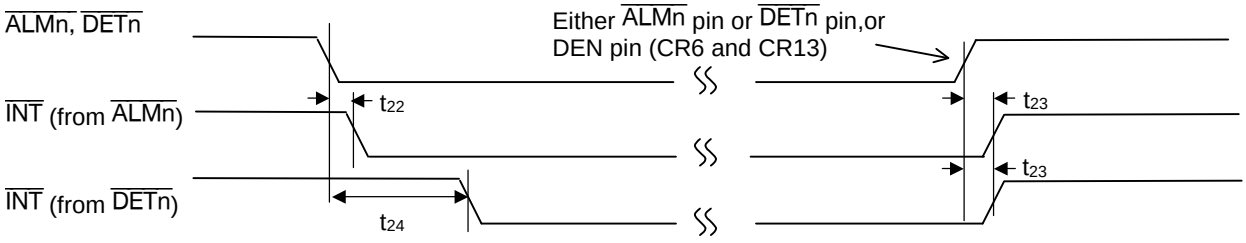


Figure 7 SLIC Interface 2 (from SLIC)

* The INT pin driven to a logic “1” in either of the following cases;

(1) ($\overline{PDN}$ pin = logic “1”) Any of the $\overline{ALMn}$ or $\overline{DETn}$ pins (maximum 4 pins concerned) in a logic “0” state go to logic “1”.
(2) ($\overline{PDN}$ pin = logic “0”) All of the $\overline{ALMn}$ or $\overline{DETn}$ pins (maximum 4 pins concerned) in a logic “0” state go to logic “1”.
(3) Both SLIC 1 control (CR6) and SLIC 2 control (CR13) are read by the MCU.

FUNCTIONAL DESCRIPTION

Pin Functional Description

AIN1N, AIN1P, AIN2N, AIN2P, GSX1, GSX2

The AINnN and AINnP pins are the transmit path analog inputs for Channel-n, where n equals channel 1 or channel 2. The AINnN pin is the inverting input, and the AINnP pin is the non-inverting input for the op-amp.

The GSXn pin functions as the transmit path level adjustment for Channel-n and is connected to the output of the op-amp. It is used to adjust the output level as shown in Figure 8 below.

When the AINnN or AINInP pins are not in use, connect the AINnN pin to the GSXn pin and the AINnP pin to the SGC pin. During power-down mode, the GSXn output is in a high impedance state.

In the case of the analog input 2.226 Vpp at the GSXn pin, the digital output will be +3.00 dBm0.

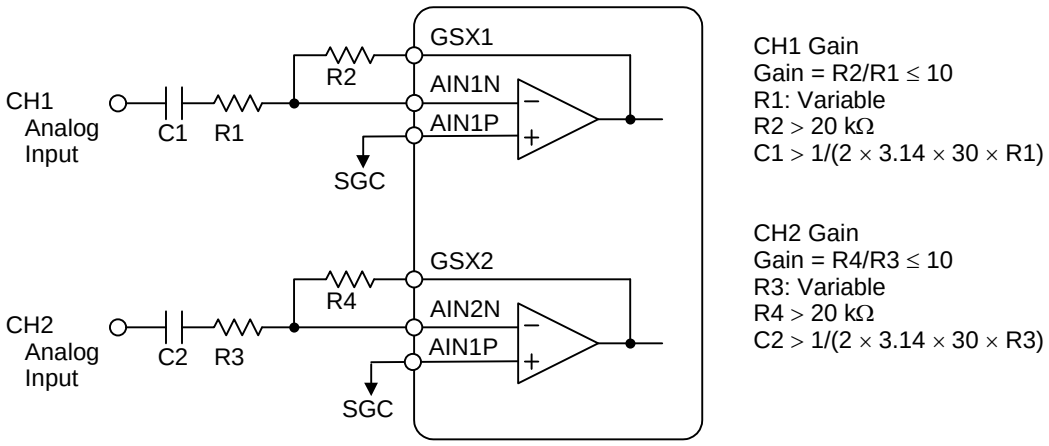


Figure 8 Example of Analog Input Setting Schematic

AOUT1P, AOUT1N, AOUT2P, AOUT2N

The AOUTnN and AOUTnP pins are the receive path analog outputs from Channel-n, where n equals channel 1 or channel 2. These pins can drive a load of 20 kΩ or more. When the AOUTnSEL register bit (CR7-B7/CR14-B7) is cleared (0), the AOUTnP pin is a single-ended output from Channel-n and the AOUTnN pin is at high impedance. When the AOUTnSEL bit is set (1), the AOUTnN and AOUTnP pins are differentials outputs from the corresponding channel.

The output signal from each of these pins has an amplitude of 3.4 Vpp above and below the signal ground voltage (SG). Hence, when the maximum PCM code (+3.00 dBm0) is input to the PCMIN pin, the maximum amplitude between the AOUTnN pin and the AOUTnP pin will be 6.8 Vpp.

While the device is in power-down mode, or the corresponding channel (1 or 2) is in power saving mode, the related outputs are high impedance. Refer to Table 5 for more information.

TOUT1, TOUT2

TOUTn is the tone analog output for the corresponding channel. The output signal has an amplitude of 2.5 Vpp above and below the signal ground voltage (SG). While the device is in power-down mode, or the corresponding channel is in power-save mode, the related outputs are high impedance.

V_{DDA}, V_{DDD}

+5 V power supply for analog and digital circuits. The V_{DDA} pin is the power pin for the analog circuits. The V_{DDD} pin is the power pin for the digital circuits. If these signals are connected together externally, The V_{DDA} pin must be connected to the V_{DDD} pin in the shortest distance on the printed circuit board. Internal to the ML7033, the V_{DDA} plane is separate from the V_{DDD} plane.

To minimize power supply noise, a 0.1 μF bypass capacitor (with excellent high frequency characteristics) and a 10 μF electrolytic capacitor should be connected between the V_{DDA} pin and the AG pin. In addition, the same capacitive network should also be connected between the V_{DDD} pin and the DG pin. If the AG and DG pins are connected together externally, only one capacitive network is required.

AG, DG

The AG pin is a ground for the analog circuits. The DG pin is a ground for the digital circuits.
The analog ground and the digital ground are separated internally within the device. The AG pin and DG pins must be connected in the shortest distance on the printed circuit board, and then to system ground with a low impedance.

SGC

The SGC pin used is to internally generate the signal ground voltage level by connecting a bypass capacitor. The output impedance is approximately 50 kΩ. Connect a 0.1 μF bypass capacitor with excellent high frequency characteristics between the SGC pin and the AG pin. During power-down mode, the SGC output is at the voltage level of the AG pin.

SG

The SG pin is the signal ground level output for the system circuits. The output voltage is 2.4 V, the as same as the SGC pin in a normal operating state. During power-down mode, this output is high impedance.

MCK

Master clock input. Input either 2.048 or 4.096 MHz clock. After turning on the power, the appropriate value must be written into the MCKSEL bit (CR0-B5) depending upon the desired master clock frequency.

If the supplied master clock frequency and the value of the MCKSEL bit (CR0-B5) do not match, the power-down control circuit and the MCU interface circuit will continue to operate properly. Access to the control registers can also occur. However, other circuits may not operate properly.

As for the power-on sequence, please refer to “Power-On Sequence” in the later page.

BCLK

Shift clock signal input for the PCMIN and the PCMOUT signals. The clock frequency, equal to the data rate, is 256 kHz to 4096 kHz. This signal must be generated from the same clock source as the master clock and synchronized in phase with the master clock. Please refer to Figures 1 and 2 for more information about the phase difference between MCK and BCLK.

RSYNC

Receive synchronizing clock input. The PCMIN signals are received in synchronization with this clock. The 8 kHz input clock is generated from the identical clock source as MCK and must be synchronized in phase with the master clock.

XSYNC

Transmit synchronizing clock input. The PCMOUT signals are transmitted in synchronization with this clock. The 8 kHz input clock is generated from the identical clock source as MCK and must be synchronized in phase with the master clock.

PCMIN

Serial PCM data input. The serial PCM data input on the PCMIN pin is converted to analog signals and output from the AOUTnP pin (or from the AOUTnN pin and the AOUTnP pin) in synchronization with the RSYNC clock and the BCLK clock.

When in Long Frame Sync Mode (CR0-B4 = “0”), the first bit of the serial PCM data (MSD of channel 1) is identified at the rising edge of the RSYNC clock.

When in Short Frame Sync Mode (CR0-B4 = “1”), the first bit of the serial PCM data (MSD of channel 1) is identified at the falling edge of the RSYNC clock.

PCMOUT

Serial PCM data output. Channel 1 data is output in sequential order, from most significant data (MSD) to least significant data (LSD). Data is synchronized with the rising edge of BCLK.

When in Long Frame Sync Mode (CR0-B4 = “0”), the first bit of PCM data may be output at the rising edge of the XSYNC signal, depending on the timing between BCLK and XSYNC.

When in Short Frame Sync Mode (CR0-B4 = “1”), the first bit of PCM data may be output at the falling edge of the XSYNC signal, depending on the timing between BCLK and XSYNC.

This pin is in a high impedance state during power-down. A pull-up resistor must be connected to this pin since it is an open drain output.

$\overline{\text{PCMOSY}}$

$\overline{\text{PCMOSY}}$ is asserted to a logic 0 when PCM data is valid on the PCMOUT pin. This includes both normal mode and power-save mode.

When PCM data is not being output from the PCMOUT pin (including during power-down mode), this pin goes a logic “1”.

This signal is used to control the TRI-STATE Enable of a backplane line-driver.

Table 1 PCM Codes in 8-bit PCM Mode with the LIN (CR0-B3) bit = "0"

INPUT/OUTPUT Level	PCMIN/PCMOUT															
	ALAW (CR0-B2) bit = "0" (μ-law)								ALAW (CR0-B2) bit = "1" (A-law)							
	MSD	D2	D3	D4	D5	D6	D7	D8	MSD	D2	D3	D4	D5	D6	D7	D8
+Full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
+0	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
–0	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
–Full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Table 2 PCM Codes in 14-bit Linear PCM Mode with the LIN (CR0-B3) bit = "1"

INPUT/OUTPUT Level	PCMIN/PCMOUT													
	MSD	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
+Full scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1
+1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
–1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
–Full scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0

$\overline{\text{PDN}}$

Power-down control signal. When $\overline{\text{PDN}}$ is a asserted (logic "0"), both the channel 1 and channel 2 circuits enter the power-down state. However, even in power-down mode, the state of the control registers is maintained. Reads and writes to the registers are also possible, and the state of the $\overline{\text{INT}}$ pin also changes in accordance with inputs from the SLIC devices. This pin is deasserted (logic "1") by external logic during normal operation.

This power-down function is available even in power saving mode by the MODEn (CR0-B1/CR0-B0) bit.

RESET

An input to reset control registers. By asserting the $\overline{\text{RESET}}$ pin (applying a logic "0"), all control registers are initialized. During a normal operation mode, set this pin logic "1".

Table 3 State of PCMOUT in 8-bit PCM Mode with LIN (CR0-B3) bit = "0"

$\overline{\text{PDN}}$ pin	MODE1 bit	MODE0 bit	ALAW bit	CH2 PCM Data	CH1 PCM Data
0	0/1	0/1	0/1	Hi-Z *1	Hi-Z *1
1	0	0	0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
			1	1 1 0 1 0 1 0 1	1 1 0 1 0 1 0 1
1	0	1	0	1 1 1 1 1 1 1 1	Operate
			1	1 1 0 1 0 1 0 1	Operate
1	1	0	0	Operate	1 1 1 1 1 1 1 1
			1	Operate	1 1 0 1 0 1 0 1
1	1	1	0	Operate	Operate
			1	Operate	Operate

Table 4 State of PCMOUT in 14-bit Linear PCM Mode with LIN (CR0-B3) bit = "1"

$\overline{PDN}$ pin	MODE1 bit	MODE0 bit	ALAW bit	CH2 PCM Data	CH1 PCM Data
0	0/1	0/1	0/1	Hi-Z *1	Hi-Z *1
1	0	0		ALL "0"	ALL "0"
1	0	1		ALL "0"	Operate
1	1	0		Operate	ALL "0"
1	1	1		Operate	Operate

Table 5 State of Analog Output Pins

$\overline{PDN}$ pin	MODE1 bit	MODE0 bit	GSX1 pin	GSX2 pin	AOUT1 pin	AOUT2 pin	SG pin	SGC pin	MCU Interface
0	0/1	0/1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	AG level *2	Operate
1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	AG level *2	Operate
1	0	1	Operate	Hi-Z	Operate	Hi-Z	Operate	Operate	Operate
1	1	0	Hi-Z	Operate	Hi-Z	Operate	Operate	Operate	Operate
1	1	1	Operate	Operate	Operate	Operate	Operate	Operate	Operate

*1 The data will be 'H' by an external pull-up resistor.
*2 Output impedance = about 50 kΩ

F2_1, F1_1, F0_1, F2_2, F1_2, F0_2

The F2_n, F1_n and F0_n pins are data outputs used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series device. The output levels from the F2_n, the F1_n and F0_n pins are determined by the F2_n, F1_n, and F0_n register bits (CR6-B7 to B5 and CR13-B7 to B5). By inputting these outputs directly into the corresponding input pin of the SLIC device, the SLIC operating mode selection is possible.

Even in the power-down state with the $\overline{PDN}$ pin is asserted, these pins remain functional.

E0_1, E0_2

The E0_n pins are the detector mode selection data outputs. These pins are used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series device. Though the output level from the E0_n pin is determined by the E0_n bit (CR6-B2/CR13-B2), the output level changes in 20 μs (= hold timer) in the power-on mode with the $\overline{PDN}$ pin = logic "1" and in 200 ns in the power-down mode with the $\overline{PDN}$ pin = logic "0" after the change of E0_n bit (CR6-B2 /CR13-B2). Refer to Figure 6 for information.

What event is actually detected by the SLIC is determined by the combination of the F2_n, F1_n, F0_n and E0_n pins. Refer to Table 6 for more information. By connecting the output directly into the corresponding input pin of the SLIC device, detector mode selection in the SLIC is possible. Even in the power-down state with the $\overline{PDN}$ pin = logic "0", this pin remains functional. However, the hold timer is ignored in this state.

Table 6 SLIC Device Operation Mode and Detector Mode

Operating Mode	F2_n	F1_n	F0_n	E0_n = 1	E0_n = 0	Description
Low Power Standby	0	0	0	SHD	GKD	Standby mode
Forward Active	0	0	1	SHD	GKD	Forward battery loop feed
Unbalanced Ringing	0	1	0	RTD	RTD	Unbalanced ringing mode
Reverse Active	0	1	1	SHD	GKD	Reverse battery loop feed
Ringing	1	0	0	RTD	RTD	Balanced ringing mode
Forward Loop Back	1	0	1	SHD	GKD	Test mode
Tip Open	1	1	0	SHD	GKD	For PBX type application
Power Denial	1	1	1	n/a	n/a	Device shutdown

SHD: Switch Hook Detection RTD: Ring Trip Detection GKD:Ground Key Detection

BSEL1, BSEL2

The BSELn pin is the battery mode selection data output. This pin is used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series SLIC device. A logic “0” on this pin selects the low battery mode, and the logic “1” selects the high battery mode within the SLIC device. The output levels from the BSELn pins are determined by the BSELn register bits (CR6-B3/CR13-B3).

By connecting these outputs directly to the corresponding SLIC device input pins, battery mode selection of the SLIC is possible. This pin remains functional even in power-down mode.

$\overline{\text{SWC1}}$, $\overline{\text{SWC2}}$

The $\overline{\text{SWCn}}$ pin is the uncommitted switch control data output. This pin is used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series SLIC device. By connecting this pin directly to the corresponding input pin of the SLIC device, the uncommitted switch control can be made. The uncommitted switch is located between the SW+ pin and the SW- pin. A logic “0” on this pin enables the SLIC internal switch on, and a logic “1” disables the switch.

The output levels from the $\overline{\text{SWC1}}$ and $\overline{\text{SWC2}}$ pins are determined by the $\overline{\text{SWCn}}$ register bits (CR6-B4/CR13-B4). This pin remains functional even in power-down mode with the $\overline{\text{PDN}}$ pin is a logic “0”.

$\overline{\text{DET1}}$, $\overline{\text{DET2}}$

The $\overline{\text{DETn}}$ pins are the SLIC’s detection signal (switch hook, ring trip or ground key detection) inputs. These pins are used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series device. A logic “0” on this pin clears the corresponding $\overline{\text{DETn}}$ register bit (CR6-B1/CR13-B1). A logic ‘1’ on this pin input sets the register bit.

The Intersil RSLIC™ series SLIC device is equipped with a function to switch the output on its $\overline{\text{DET}}$ pin from a logic “1” state to a logic “0” state when it detects an assigned event of either off-hook, ring trip or ground key. Therefore, by connecting these pins to the corresponding pins on the SLIC device and reading the $\overline{\text{DETn}}$ register bit (CR6-B1/CR13-B1), the occurrence of an assigned event can be detected.

The event detected by the SLIC is determined by the F2_n, F1_n, and F0_n register bits (CR6-B7 to B5/CR13-B7 to B5), and the E0_n register bits (CR6-B2 /CR13-B2). To avoid the unintended detection of these conditions due to glitches on the $\overline{\text{DETn}}$ signal of the SLIC, the ML7033 is equipped with a debounce timer to hold the DET register bit (CR6-B1/CR13-B1) and the output of the $\overline{\text{INT}}$ pin for a set period, even when an input to the $\overline{\text{DETn}}$ pin changes from a logic "1" to a logic "0". For more information on the debounce timer, refer to the DETnTIM3 through DETnTIM0 register bit descriptions (CR4-B7 to B0).

This pin remains functional in power-down mode ($\overline{\text{PDN}}$ pin low). However, while in the power-down state, the debounce timer is disabled.

When this pin is not used, it should be tied to V_{DDD}.

$\overline{\text{ALM1}}$, $\overline{\text{ALM2}}$

The $\overline{\text{ALMn}}$ pins are the thermal shut down alarm signals. These pins are used when the SLIC connected to the corresponding channel is an Intersil RSLIC™ series device. A logic "0" on the $\overline{\text{ALMn}}$ input pin clears the corresponding ALM register bit (CR6-B0/CR13-B0). A logic "1" on this pin sets the bit.

The Intersil RSLIC™ series device is equipped with a function that allows it to automatically enter power-down mode and toggle its $\overline{\text{ALMn}}$ pin from a logic "1" to a logic "0" state when the SLIC die temperature exceeds a safe operating temperature. Hence, by connecting the corresponding pin of the SLIC device to the $\overline{\text{ALM1}}$ and $\overline{\text{ALM2}}$ pins and reading the ALM register bit (CR6-B0/CR13-B0), it is possible to know whether the concerned SLIC device is operating normally, or is in a thermal shutdown state.

This pin remains functional in power-down mode. However, while in the power-down state, the debounce timer is disabled.

When this pin is not used, it should be tied to V_{DDD}.

$\overline{\text{INT}}$

The ML7033 asserts the $\overline{\text{INT}}$ interrupt pin when either the $\overline{\text{DETn}}$ pin or the $\overline{\text{ALMn}}$ pin are asserted by the SLIC device when the device is an Intersil RSLIC™ series SLIC device. The Intersil RSLIC™ series device is equipped with detector and thermal shut down alarm functions to notify a change of SLIC state by driving a logic 0 onto the output pins connected to $\overline{\text{DETn}}$ and $\overline{\text{ALMn}}$. Refer to the $\overline{\text{DETn}}$ and $\overline{\text{ALMn}}$ pin descriptions above. By monitoring the state of the $\overline{\text{INT}}$ pin and reading the DETn (CR6-B0/CR13-B0) and ALMn (CR6-B0/CR13-B0) register bits, it is possible to know that a change of a state occurred within the SLIC device.

The $\overline{\text{INT}}$ pin transitions from a logic "1" to a logic "0" in the following cases;

(1) ($\overline{\text{PDN}}$ pin = logic "0") Any of the $\overline{\text{ALMn}}$ or $\overline{\text{DETn}}$ pins in the logic "1" state transition to the logic "0" state.
(2) ($\overline{\text{PDN}}$ pin = logic "1") Any of the $\overline{\text{ALMn}}$ or $\overline{\text{DETn}}$ pins transition from the logic "1" state to the logic "0" state when all the four pins ($\overline{\text{ALM1}}$, $\overline{\text{ALM2}}$, $\overline{\text{DET1}}$, and $\overline{\text{DET2}}$) have been in the logic "1" state.

Note that the debounce timer with the $\overline{\text{DETn}}$ pin is not valid while in power-down mode ($\overline{\text{PDN}}$ pin = logic "0").

The $\overline{INT}$ pin is released to the logic "1" state in either of the following cases;

(1) ($\overline{PDN}$ pin = logic "1") Any one of the $\overline{ALMn}$ or $\overline{DETn}$ pins in the logic "0" state transition to the logic "1" state.
(2) ($\overline{PDN}$ pin = logic "0") All of the $\overline{ALMn}$ or $\overline{DETn}$ pins in the logic "0" state transition to the logic "1" state.
(3) Both SLIC 1 control (CR6 register) and SLIC 2 control (CR13 register) are read by the MCU.

Note that the debounce timer, which works when the $\overline{DETn}$ pin changes from a logic "1" state to a to logic "0" state, does not work when the pin changes from logic "0" to logic "1".

$\overline{DEN}$, EXCK, DIO

Serial control ports for the MCU interface. These pins are used by an external MCU to access the internal control registers of the ML7033. The $\overline{DEN}$ pin is the data enable input. The EXCK pin is the data shift clock input. The DIO pin is the address and data input/output. Figure 9 shows the MCU interface input/output timing diagram. Note that EXCK must be a continuous clock of at least 15 pulses or more.

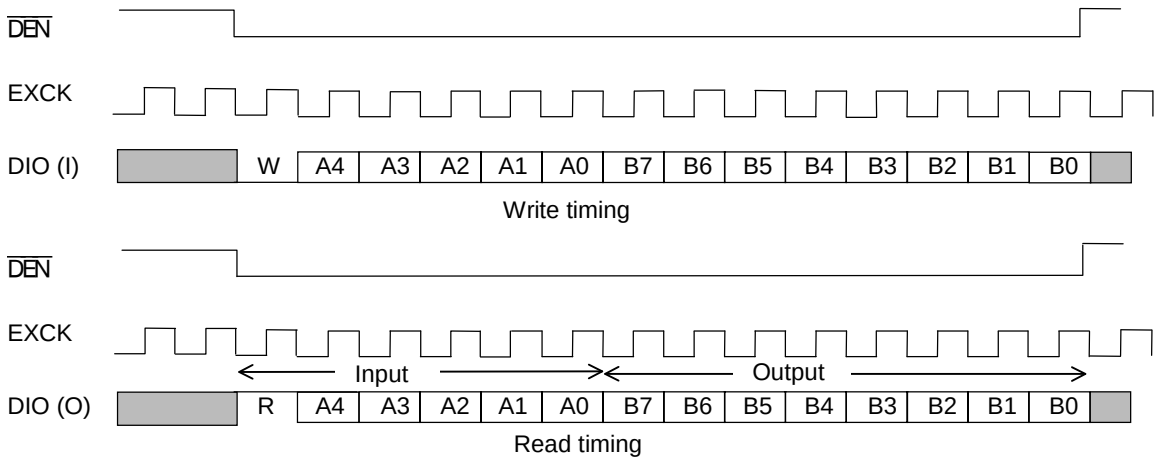


Figure 9 MCU Interface Timing Diagram

CIDATA1, CIDATA2

The CIDATA1 and CDATA2 data inputs are used for Caller ID generation. While in a Caller ID tone generation mode with the CIDCHnON register bit set, (CR1-B1/CR1-B0), signals on the CIDATAn pins are modulated in either the ITU-T V.23 or Bell 202 schemes. The scheme is determined by the CIDFMT register bit (CR1-B2), and output from the analog output pin(s).

The analog output pins for modulated Caller ID data can be selected by the CHnTG2TX (CR7-B6/CR14-B6), the CHnTGTOUTn (CR7-B5/CR14-B5), and the AOUTnSEL (CR7-B7/CR14-B7) register bits.

The output level for the modulated Caller ID data can be tuned by the CHnTG1LVn (CR9-B7 to B1/CR16-B7 to B1) register bits.

TEST

The TEST input is used for testing purposes only during the manufacturing process and has no function once the testing process is completed. This pin is not used during normal operation of the device and should be kept at a logic "0" state.

Power-On Sequence

While in the power-on state, the following chart is recommended.

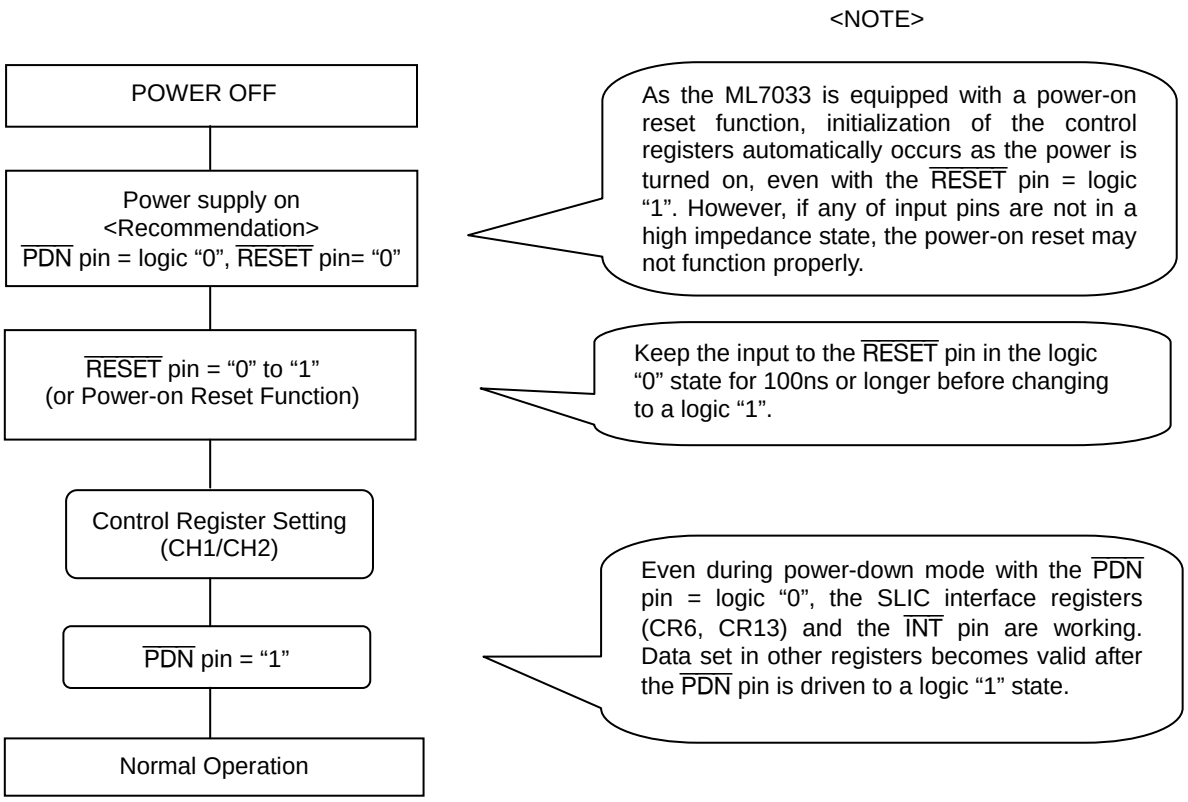


Figure 10 Power-on Sequence Flow Chart

Control Registers Functional Description

CR0 (Basic operating mode)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	FILTER1SEL	FILTER2SEL	MCKSEL	SHORT	LIN	ALAW	MODE1	MODE0
default	0	0	0	0	0	0	0	0

B7 … Transmit and receive filter select for CH1
0 : ITU-T G.714 filter 1 : wideband filter for V.90 data modem application

B6 … Transmit and receive filter select for CH2
0 : ITU-T G.714 filter 1 : wideband filter for V.90 data modem application

B5 … MCK frequency select 0 : 2.048 MHz 1 : 4.096 MHz

B4 … Frame synchronizing scheme select 0 : Long frame SYNC 1 : Short frame SYNC
Refer to Figure 3.

B3 … PCM companding law select
0 : 8-bit PCM mode 1 : 14-bit linear PCM (2's complement) mode
"1" is selected, a setting with the ALAW (CR0-B2) bit is ignored.

B2 … PCM companding law select 0 : μ-law 1 : A-law
When the LIN (CR0-B3) is "1", a setting with this bit is ignored.

B1, B0 … Power saving control 0 : Power saving mode 1 : Normal operation
The MODE1 (CR0-B1) bit is for channel 2, and the MODE0 (CR0-B0) bit is for channel 1. In power saving mode, power for the corresponding channel is turned off except for the last output stage of the PCMOUT pin. The power saving mode differs from the power-down mode controlled by the $\overline{PDN}$ pin in the following aspects;

- Possible to control a state for an individual channel independently
- The last stage of the PCMOUT pin is operational, and outputs 'positive zero' PCM code in the 8-bit PCM mode or 'zero' PCM code in the 14-bit Linear PCM mode during the assigned time slot.
- Debounce timer and hold timer are valid.

As in power-down mode, the power saving mode does not initialize control registers and read and write of control registers are possible in the power saving mode. The power-down mode setting by the $\overline{PDN}$ pin takes precedence over the power saving mode.

Table 7 Mode Settings for CH1 and CH2

MODE1 bit	MODE0 bit	$\overline{PDN}$ pin	$\overline{RESET}$ pin	Power of Channel		Register
				CH2	CH1	
0*1	0*1	0	0	OFF	OFF	Initialized to default
0*1	0*1	1	0	OFF*2	OFF*2	Initialized to default
0/1	0/1	0	1	OFF	OFF	Read/Write possible
0	0	1	1	OFF*2	OFF*2	Read/Write possible
0	1	1	1	OFF*2	ON	Read/Write possible
1	0	1	1	ON	OFF*2	Read/Write possible
1	1	1	1	ON	ON	Read/Write possible

*1 forced to be default by the $\overline{RESET}$ pin = logic "0". *2 The last output stage is powered.

CR1 (Tone generator and Call ID tone control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	CH2TG ON	CH1TG ON				CIDFMT	CID CH2ON	CID CH1ON
default	0	0	0	0	0	0	0	0

B7 … State control for a tone generator on CHl 0 : disabled 1 : enabled

B6 … State control for a tone generator on CH2 0 : disabled 1 : enabled

B5, B4, B3 … Reserved (The default alternation is prohibited.)
When a write action is executed for CR1, set these bits to “0”.

B2 … Caller ID generator modulation scheme select
0 : ITU-T V.23 scheme (1: 1300 Hz, 0: 2100 Hz)
1 : Bell 202 format (1: 1200 Hz, 0: 2200 Hz)

B1 … State control for Caller ID generator on CH2 0 : OFF 1 : ON
Regardless of how the CH2TGON bit (CR1-B7) is set, signals input into the CIDATA2 pin are modulated and output as Caller ID tones. When this bit is set, the level setting by the CH2TG1LVn (CR16-B7 to B1) bits is valid, but the CH2TG1_n (CR16-B0/CR17-B7 to B0) bits, CH2RING (CR11-B7) bit, and CH2TG1TRPn (CR11-B6 to B4) bits are invalid.

B0 … State control for Caller ID generator on CH1 0 : OFF 1 : ON
Regardless of how the CH1TGON bit (CR1-B6) is set, signals input into the CIDATA1 pin are modulated and output as Caller ID tones. When this bit is set, the level set by the CH1TG1LVn (CR9-B7 to B1) bits is valid, but the CH1TG1_n (CR9-B0/CR11-B7 to B0) bits, the CH1RING (CR11-B3) bit, and the CH1TG1TRPn (CR11-B2 to B0) bits are invalid.

CR2 (Pulse metering tone generator control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	PMG2 FRQ	PMG2 LV1	PMG2 LV0	PMG2 TOUT2	PMG1 FRQ	PMG1 LV1	PMG1 LV0	PMG1 TOUT1
default	0	0	0	0	0	0	0	0

B7 … Pulse metering tone frequency select for CH2 0 : 12 kHz 1 : 16 kHz

B6, B5 … Pulse metering tone level setting for CH2
(B6, B5) (0, 0) = OFF
(0, 1) = 0.5 Vpp
(1, 0) = 1.0 Vpp
(1, 1) = 1.5 Vpp
The level of the pulse metering tone, as shown in Figure 11, reaches the assigned level in 10 ms and gradually fades out over 10 ms.

The ramp-up and ramp-down times also apply when a tone is cancelled by writing (0,0) into these register bits. Once the register bits are set, the tone begins to fade out and completely fades out after 10 ms. In addition, subsequent writes to these bits are prohibited for 10 ms.

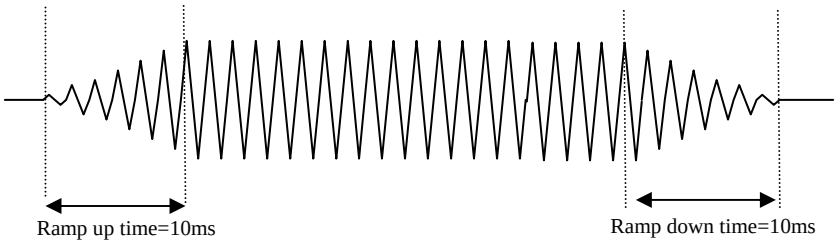


Figure 11 Pulse Metering Tone Waveform

B4 … Pulse metering tone output pin select for CH2
0 : AOUT2 pin (added to voice signals) 1 : TOUT2 pin

B3 … Pulse metering tone frequency select for CH2 0 : 12 kHz 1 : 16 kHz

B2, B1 … Pulse metering tone level setting for CH1
(B2, B1) (0,0) = OFF
(0, 1) = 0.5 Vpp
(1, 0) = 1.0 Vpp
(1, 1) = 1.5 Vpp
The level of the pulse metering tone, as shown in Figure 11, reaches the assigned level in 10 ms and gradually fades over 10 ms.

The ramp-up and ramp-down times also apply when a tone is cancelled by writing (0,0) into these register bits. In this case the tone fades out after 10 ms. In addition, subsequent writes to these bits are prohibited for 10 ms.

B0 … Pulse metering tone frequency select for CH1 0 : 12 kHz 1 : 16 kHz

CR3 (Time slot assignment control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	TSAE	TSAC	TSA5	TSA4	TSA3	TSA2	TSA1	TSA0
default	0	0	0	0	0	0	0	0

* CR3 is a write only register.

B7 … Time slot assignment customization enable
0 : Default time slot assignment 1 : Customized time slot assignment
The default time slot assignment is CH1 for Slot 0 and CH2 for Slot 2.

B6 … Time slot assignment channel select 0 : CH1 1 : CH2
This bit is used to specify the channel for which the accompanied TSAn (CR3-B5 to B0) bits are going to assign a time slot. Hence, when a customized time slot assignment is enabled, CR3 should be written twice; once for CH1 and another for CH2.

B5 to B0 … Assigned time slot select
Each time slot consists of 8 BCLK cycles. The number of time slots available for time slot assignment depends upon the applied BCLK frequency, and can be calculated in the following equations;

Number of time slots available for time slot assignment
= (BCLK frequency)/(SYNC frequency)/8
= (BCLK frequency)/64k

For instance, when the BCLK frequency is 4096 kHz, time slots that can be assigned are from 0 (000000) to 63 (111111). The specification of a time slot beyond 63 is prohibited. Note that in 14-bit linear PCM (2's complement) mode, specified when the LIN bit (CR0-B3) is set, only even numbered time slots (0, 2, 4, … 62) can be assigned.

In any mode, the assigned time slot for a channel is common both for transmit and receive, and different time slots cannot be assigned for transmit and receive. When the TSAE bit (CR3-B7) is cleared, the time slot assignment specified by these bits is ignored, and the default time slots are assigned (CH1 for Time Slot 0 and CH2 for Time Slot 2). Figure 12 shows an example of how CH1 is assigned for Time Slot 0 (000000) and CH2 is assigned for Time Slot 3 (000011) in 8-bit PCM mode.

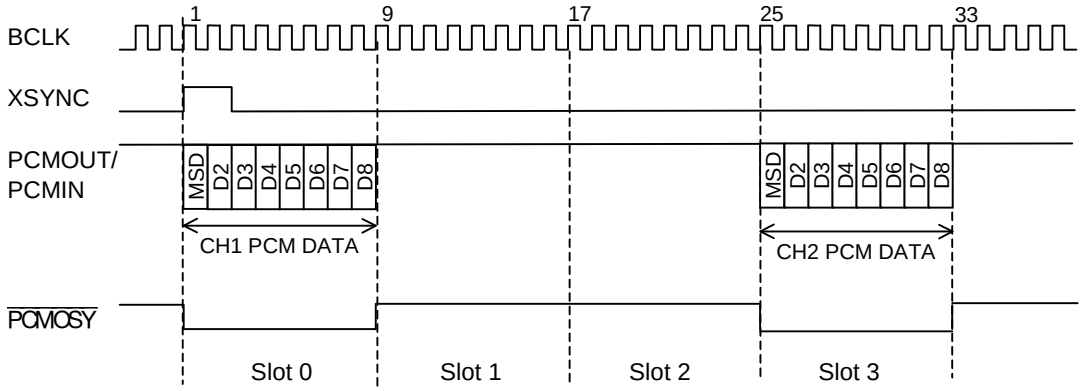


Figure 12 Example of Time Slot Assignment: CH1 = Slot 0, CH2 = Slot 3

CR4 (Debounced timer setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	DET2 TIM3	DET2 TIM2	DET2 TIM1	DET2 TIM0	DET1 TIM3	DET1 TIM2	DET1 TIM1	DET1 TIM0
default	0	0	0	0	0	0	0	0

B7 to B4 … Debounce timer setting for CH2
B3 to B0 … Debounce timer setting for CH1

To avoid the unintended detection of glitches on the $\overline{\text{DETn}}$ signal, the ML7033 is equipped with a debounce timer to hold the $\overline{\text{DETn}}$ (CR6-B1/CR13-B1) bit and the $\overline{\text{INT}}$ output state for a set period, even when the state of the $\overline{\text{DETn}}$ pin changes from logic "1" to logic "0". Bits B7 to B4 determine the debounce timer setting for CH2. Bits B3 to B0 determine the debounce timer setting CH1.

The debounce timer is operational only in the power-on state when the $\overline{\text{PDN}}$ pin = logic "1", and remains operational in the power-saving mode with the MODEn (CR0-B1, B0) bits = "0" as long as the device is in the power-on state.

The debounce timer holding time ranges from 0 ms to 225 ms at 15 ms intervals for each individual channel. The values written into B7 to B4 (channel 2) or B3 to B0 (channel 1) determine the holding time for each channel.

The timer value is calculated by the equation of [Decimal(B7,B6,B5,B4) * 15] or [Decimal(B3,B2,B1,B0) * 15]. Refer to Table 8.

Table 8 Debounce Timer Setting

B7/B3	B6/B2	B5/B1	B4/B0	Timer (ms)
0	0	0	0	0
0	0	0	1	15
0	0	1	0	30
0	0	1	1	45
0	1	0	0	60
:	:	:	:	:
0	1	1	1	105
1	0	0	0	120
1	0	0	1	135
:	:	:	:	:
1	1	1	1	225

CR5 (CH1 transmit/receive level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	LV1R3	LV1R2	LV1R1	LV1R0	LV1X3	LV1X2	LV1X1	LV1X0
default	0	0	0	0	0	0	0	0

B7 to B4 … Level setting for CH1 on its receive side
The LV1R3 to LV1R0 bits determine the level for the CH1 receive side as shown in Table 9.

B3 to B0 … Level setting for CH1 on its transmit side
The LV1X3 to LV1X0 bits determine the level for the CH1 transmit side as shown in Table 9.

Table 9 Receive and Transmit Level Setting

LV1R3/LV1X3	LV1R2/ LV1X2	LV1R1/LV1X1	LV1R0/LV1X0	Level (dBm0)
0	0	0	0	0.0
0	0	0	1	–1.0
0	0	1	0	–2.0
0	0	1	1	–3.0
0	1	0	0	–4.0
0	1	0	1	–5.0
0	1	1	0	–6.0
0	1	1	1	–7.0
1	0	0	0	–8.0
1	0	0	1	–9.0
1	0	1	0	–10.0
1	0	1	1	–11.0
1	1	0	0	–12.0
1	1	0	1	–13.0
1	1	1	0	–14.0
1	1	1	1	OFF

CR6 (SLIC 1 control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR6	F2_1	F1_1	F0_1	SWC1	BSEL1	E0_1	DET1	ALM1
default	0	0	0	0	0	0	—	—

* CR6-B1 and B0 are read-only bits. Though either of "0" or "1" will do for these registers when a byte-wide write action is made, the written values are ignored.
* The $\overline{INT}$ pin which stays at logic "0" will be released to logic "1" when both of this control register (CR6) and SLIC 2 control register (CR13) are read.

B7 to B5 … Operation mode setting for SLIC1

The F2_1 to F0_1 bits determine the output level for the Fn_1 pins. For more details, refer to Table 6. When each bit is cleared ("0"), the corresponding Fn_1 pin outputs a logic "0". When each bit is set ("1"), the corresponding Fn_1 pin outputs a logic "1".

B4 … Uncommitted switch control for SLIC1 0 : switch on 1 : switch off

This bit determines the output level for the $\overline{SWC1}$ pin. When this bit is cleared, the $\overline{SWC1}$ pin outputs a logic "0". When this bit is set, the pin outputs a logic "1".

When the SLIC connected to CH1 is the Intersil RSLIC™ series, the SLIC's internal uncommitted switch, located between the SW+ pin and the SW- pin, can be controlled by inputting the output from the SWC1 pin directly into the corresponding input pin of the SLIC device.

B3 … Battery mode select for SLIC1 0 : low battery mode 1 : high battery mode

This bit determines the output level for the BSEL1 pin. When this bit is cleared, the BSEL1 pin outputs a logic "0". When this bit is set, the pin outputs a logic "1".

When the SLIC connected to CH1 is from the Intersil RSLIC™ series, the SLIC's battery mode selection is possible by inputting the output from the BSEL1 pin directly into the corresponding input pin of the SLIC device.

B2 … Detector mode selection for SLIC1

This bit determines the output level for the E0_1 pin. When this bit is cleared, the E0_1 pin outputs a logic "0". When this bit is set, the pin outputs a logic "1".

When a SLIC connected to CH1 is Intersil RSLIC™ series, the SLIC's detector mode selection is possible by connecting the E0_1 pin directly to the corresponding input pin of the SLIC device. The event detected by the SLIC is determined by the combination of the F2_1, the F1_1, the F0_1 and the E0_1 pins as shown in Table 6.

The output level of the E0_1 pin changes 20μs later (hold timer) in the power-on mode with the $\overline{PDN}$ pin = logic "1", and 200ns later in the power-down mode with the PDN pin = logic "0" than a change of this bit value. Refer to Figure 6.

B1 … Event detection indicator for SLIC1 (Read-only bit) 0 : detected 1 : not detected
By reading the state of this bit, the input level to the $\overline{DET1}$ pin can be known. If this bit is cleared it indicates that the $\overline{DET1}$ pin is in the logic “0” state. If this bit is set it indicates that the $\overline{DET1}$ pin is in the logic “1” state.

When the SLIC connected to channel 1 is from the Intersil RSLIC™ series, the $\overline{DET1}$ pin can be connected directly to the corresponding output pin of the SLIC device. This allows an assigned event such as off-hook, ring trip, or ground key to be detected. The event detected by the SLIC detects is determined by the F2_1, F1_1, F0_1 (CR6-B7 to B5), and E0_1 (CR6-B2) bits.

When the debounce timer is enabled by setting the DET1TIM3 through DET1TIM0 bits (CR4-B3 to B0), the DET1 (CR6-B1) bit is held unchanged for a set period, even when the DET1 input pin changes from logic “1” to logic “0”.

B0 … Thermal Shutdown Alarm indicator for SLIC1 (Read-only bit) 0 : detect 1 : not detect

By reading this bit, the input level to the $\overline{ALM1}$ pin can be known. When this bit is cleared, the $\overline{ALM1}$ pin is a logic “0”. When this bit is set, the pin is a logic “1”.

When the SLIC connected to channel 1 is from the Intersil RSLIC™ series, the ALM1 pin can be connected directly to the corresponding output pin of the SLIC device. This allows the user to know whether the SLIC1 is in the normal operating state, or in the thermal shutdown state.

CR7 (CH1 Tone generator 2 control 1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR7	AOUT1 SEL	CH1TG 2 TX	CH1TG 2 TOUT1	CH1TG2 LV3	CH1TG2 LV2	CH1TG2 LV1	CH1TG2 LV0	CH1TG2 _8
default	0	0	0	0	0	0	0	0

CR8 (CH1 Tone generator 2 control 2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR8	CH1TG2 _7	CH1TG2 _6	CH1TG2 _5	CH1TG2 _4	CH1TG2 _3	CH1TG2 _2	CH1TG2 _1	CH1TG2 _0

CR7-B7 … AOUT1P, AOUT1N output select
0 : Single-ended output with the AOUT1P pin with the AOUT1N pin at high impedance
1 : Differential output with the AOUT1P and the AOUT1N pins

B6 … CH1 tone generator output select 0 : to Rx side 1 : to Tx side

B5 … CH1 tone generator Rx side output pin select 0 : AOUT1 pin 1 : TOUT1 pin

B4 to B1 … CH1 Tone Generator 2 (TG2) output level setting
This 4-bit field defines the output level for TG2 on CH1 as shown in Table 10.

Table 10 TG2 Level Setting

B4 (TG2LV3)	B3 (TG2LV2)	B2 (TG2LV1)	B1 (TG2LV0)	Level (dBm0)
0	0	0	0	OFF
0	0	0	1	–12.0
0	0	1	0	–11.0
0	0	1	1	–10.0
0	1	0	0	–9.0
0	1	0	1	–8.0
0	1	1	0	–7.0
0	1	1	1	–6.0
1	0	0	0	–5.0
1	0	0	1	–4.0
1	0	1	0	–3.0
1	0	1	1	–2.0
1	1	0	0	–1.0
1	1	0	1	0.0
1	1	1	0	+1.0
1	1	1	1	+2.0

CR7-B0, CR8-B7 to B0 … CH1 Tone Generator 2 (TG2) Frequency Select

These bits define the output frequency from TG2 on CH1. The frequency is between 300 and 3400Hz at 10Hz intervals. The values written to these bits determine the frequency as shown in the following equation. Refer to Table 11.

Binary data for CR7-B0, CR8-B7 to B0
= (Output Frequency [Hz])/10

Below is an example of how these bits are programmed when the intended frequency is 1500Hz;

Ex) (Output Frequency [Hz])/10 = 1500/10 = 150d = 10010110b
Bits to set in CR7-B0, CR8-B7 to B0 = (0,1,0,0,1,0,1,1,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 300 and 3400 Hz.

Table 11 Tone Generator Frequency Setting

Frequency (Hz)	decimal	hex	CR7	CR8							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

CR9 (CH1 tone generator 1 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR9	CH1TG1 LV6	CH1TG1 LV5	CH1TG1 LV4	CH1TG1 LV3	CH1TG1 LV2	CH1TG1 LV1	CH1TG1 LV0	CH1TG1 _8
default	0	0	0	0	0	0	0	0

CR10 (CH1 tone generator 1 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR10	CH1TG1 _7	CH1TG1 _6	CH1TG1 _5	CH1TG1 _4	CH1TG1 _3	CH1TG1 _2	CH1TG1 _1	CH1TG1 _0
default	0	0	0	0	0	0	0	0

CR9-B7 to B1 … CH1 Tone Generator 1 (TG1) Output Level Setting

This 7-bit field defines the output level of TG1 on CH1. The output level can be turned OFF or ON. When turned on, the level is between –12.1 dBm0 and +0.5 dBm0 at 0.1 dBm0 intervals as shown in Table 12.

The value written to this field is calculated based on the desired output level as shown in the following equation.

Binary data for CR9- B7 to B1
= [(Output Level [dBm0]) + 12.2]*10

The following is an example of how to program this field when the intended output level is –5.8 dBm0;

Ex) [(Output Level [dBm0]) + 12.2]*10 = (-5.8 + 12.2)*10 = 64d = 1000000b
Bits to set in CR9-B7 to B1 = (1,0,0,0,0,0,0)

Table 12 Tone Generator 1 Level Setting

B7 TG1LV6	B6 TG1LV5	B5 TG1LV4	B4 TG1LV3	B3 TG1LV2	B2 TG1LV1	B1 TG1LV0	Level (dBm0)
0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	–12.1
0	0	0	0	0	1	0	–12.0
0	0	0	0	0	1	1	–11.9
0	0	0	0	1	0	0	–11.8
:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	–5.9
1	0	0	0	0	0	0	–5.8
1	0	0	0	0	0	1	–5.7
:	:	:	:	:	:	:	:
1	1	1	1	0	1	0	0.0
1	1	1	1	0	1	1	0.1
1	1	1	1	1	0	0	0.2
1	1	1	1	1	0	1	0.3
1	1	1	1	1	1	0	0.4
1	1	1	1	1	1	1	0.5 (= 1.25 V_{op})

CR9-B0, CR10-B7 to B0 …CH1 Tone Generator 1 Output Frequency Select

When the CH1RING (CR11-B3) bit is cleared (“0”), these 9 bits determine the output frequency of tone generator 1 on channel 1 to a value between 300 and 3400 Hz at 10Hz intervals. A sample list of frequencies is shown in Table 13. The value programmed into this field is calculated based on the desired frequency using the following equation.

Binary data for CR9-B0, CR10-B7 to B0
= (Output Frequency [Hz])/10

The following is an example of how to program this field when the intended frequency is 1500 Hz;

Ex) (Output Frequency [Hz])/10 = 1500/10 = 150d = 10010110b
Bits to set in CR9-B0, CR10-B7 to B0 = (0,1,0,0,1,0,1,1,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 300 and 3400 Hz.

Table 13 Tone Generator Frequency Setting (CH1RING bit = “0”)

Frequency (Hz)	decimal	hex	CR9	CR10							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

When the CH1RING (CR11-B3) bit is set ("1"), the CH1TG1_8 (CR9-B0) bit and the CH1TG1_7 to CH1TG1_6 (CR10-B7 to B6) bits are ignored and the CH1TG1_5 to CH1TG1_0 (CR10-B5 to B0) bits are used to define the ringing tone frequency.

When the CH1RING (CR11-B3) bit is set, the frequency can be set to a value between 15 Hz and 50 Hz at 1 Hz intervals. The value programmed into this field is calculated based on the desired frequency using the following equation. A partial list of frequencies is shown in Table 14.

Binary data for CR10-B5 to B0
= (Output Frequency [Hz])

The following is an example of how to program this field when the intended frequency is 20Hz;

Ex) Output Frequency [Hz] = 20d = 010100b
Bits to set in CR10-B5 to B0 = (0,1,0,1,0,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 15 and 50Hz.

Table 14 Tone Generator Frequency Setting (CH1RING bit = "1")

Frequency (Hz)	decimal	hex	CR9	CR10							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
15	15	0Fh	—	—	—	0	0	1	1	1	1
16	16	10h	—	—	—	0	1	0	0	0	0
17	17	11h	—	—	—	0	1	0	0	0	1
18	18	12h	—	—	—	0	1	0	0	1	0
19	19	13h	—	—	—	0	1	0	0	1	1
20	20	14h	—	—	—	0	1	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
48	48	30h	—	—	—	1	1	0	0	0	0
49	49	31h	—	—	—	1	1	0	0	0	1
50	50	32h	—	—	—	1	1	0	0	1	0

CR11 (Ringing_ON and Trapezoid crest factors control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR11	CH2 RING	CH2TG1 TRP2	CH2TG1 TRP1	CH2TG1 TRP0	CH1 RING	CH1TG1 TRP2	CH1TG1 TRP1	CH1TG1 TRP0
default	0	0	0	0	0	0	0	0

B7 … CH2 Tone Generator 1 (TG1) function select
0 : CH2TG1 works as a non-ringing tone generator (300 to 3400 Hz)
1 : CH2TG1 works as a ringing tone generator (15 to 50 Hz)
The frequency and level of CH2TG1 are set by CR16 to CR17.

B6 to B4 … CH2 ringing tone waveform setting
This 3-bit field determines the type of ringing tone waveform for TG1 on CH2. A sinusoidal waveform, or a trapezoidal waveform with a crest factor between 1.225 V and 1.375 V at 0.025 V intervals, can be selected as shown in Table 15. For a definition of 'crest factor', refer to Figure 13. These bits are valid when the CH2RING (CR11-B7) bit is set.

B3 … CH1 TG1 function select
0 : CH1TG1 works as a non-ringing tone generator (300 to 3400 Hz)
1 : CH1TG1 works as a ringing tone generator (15 to 50 Hz)
The frequency and level of CH1TG1 are set by CR9 to CR10.

B2 to B0 … CH1 ringing tone waveform setting
This 3-bit field determines the type of ringing tone waveform for TG1 on CH1. A sinusoidal waveform, or a trapezoidal waveform with a crest factor between 1.225 V and 1.375 V at 0.025 V intervals, can be selected as shown in Table 15. For a definition of 'crest factor', refer to Figure 13. These bits are valid when the CH1RING (CR11-B3) bit is set.

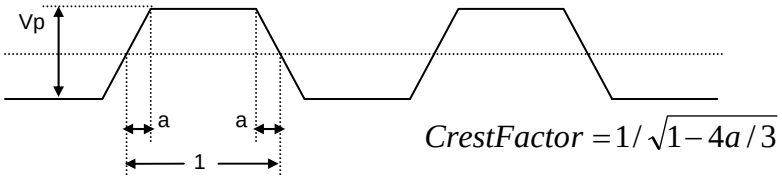


Figure 13 Ringing Tone Waveform

Table 15 Crest Factor Setting

B6/B2 TG1 TRP2	B5/B1 TG1 TRP1	B4/B0 TG1 TRP0	Crest Factor
0	0	0	OFF
0	0	1	1.225
0	1	0	1.250
0	1	1	1.275
1	0	0	1.300
1	0	1	1.325
1	1	0	1.350
1	1	1	1.375

CR12 (CH2 transmit/receive level control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR12	LV2R3	LV2R2	LV2R1	LV2R0	LV2X3	LV2X2	LV2X1	LV2X0
default	0	0	0	0	0	0	0	0

B7 to B4 … Level setting for CH2 on its receive side
This 4-bit field determines the level setting for the CH2 receive side. The settings range from 0 to –14 dBm0 as shown in Table 16.

B3 to B0 … Level setting for CH2 on its transmit side
This 4-bit field determines the level setting for the CH2 transmit side. The settings range from 0 to –14 dBm0 as shown in Table 16.

Table 16 Receive and Transmit Level Setting

LV2R3/ LV2X3	LV2R2/ LV2X2	LV2R1/ LV2X1	LV2R0/ LV2X0	Level (dBm0)
0	0	0	0	0.0
0	0	0	1	–1.0
0	0	1	0	–2.0
0	0	1	1	–3.0
0	1	0	0	–4.0
0	1	0	1	–5.0
0	1	1	0	–6.0
0	1	1	1	–7.0
1	0	0	0	–8.0
1	0	0	1	–9.0
1	0	1	0	–10.0
1	0	1	1	–11.0
1	1	0	0	–12.0
1	1	0	1	–13.0
1	1	1	0	–14.0
1	1	1	1	OFF

CR13 (SLIC 2 control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR13	F2_2	F1_2	F0_2	SWC2	BSEL2	E0_2	DET2	ALM2
default	0	0	0	0	0	0	-	-

* CR13-B1 and B0 are read-only bits. Though either of "0" or "1" will do for these registers when a byte-wide write action is made, the written values are ignored.
* The $\overline{INT}$ pin which stays at logic "0" will be released to logic "1" when both of this control register (CR13) and SLIC 1 control register (CR6) are read.

B7 to B5 … Operation mode setting for SLIC2
This 3-bit field determines the output level of the Fn_2 pins. For more detail, refer to Table 6. When any of these bits are cleared, the corresponding Fn_2 pin outputs a logic "0". When any of these bits are set, the corresponding Fn_2 pin outputs a logic "1".

B4 … Uncommitted switch control for SLIC2 0 : switch on 1 : switch off
This bit determines the output level of the $\overline{SWC2}$ pin. When this bit is cleared, the SWC2 pin outputs a logic "0". When this bit is set, the $\overline{SWC2}$ pin outputs a logic "1".

When the SLIC connected to channel 2 is an Intersil RSLIC™ series device, the internal uncommitted switch of the SLIC, located between the SW+ and the SW- pins, can be controlled by connecting the $\overline{SWC2}$ pin directly to the corresponding input pin of the SLIC device.

B3 … Battery mode select for SLIC2 0 : low battery mode 1 : high battery mode
This bit determines the output level for the BSEL2 pin. When this bit is cleared, the BSEL2 pin outputs a logic "0". When this bit is set, the BSEL2 pin outputs a logic "1".

When the SLIC connected to CH2 is an Intersil RSLIC™ series device, the battery mode selection of the SLIC is possible by connecting the BSEL2 pin directly to the corresponding input pin of the SLIC device.

B2 … Detector mode selection for SLIC2
This bit determines the output level of the E0_2 pin. When this bit is cleared, the E0_2 pin outputs a logic "0". When this bit is set, the E0_2 pin outputs a logic "1".

When the SLIC connected to channel 2 is an Intersil RSLIC™ series device, the detector mode selection of the SLIC is possible by connecting the E0_2 pin directly to the corresponding input pin of the SLIC device. The event detected by the SLIC is determined by the F2_2, F1_2, F0_2 and E0_2 output pins as shown in Table 6.

The output level from the E0_2 pin changes 20 μs later (hold timer) in the power-on mode with the $\overline{PDN}$ pin = logic "1", and 200 ns later in the power-down mode with the $\overline{PDN}$ pin = logic "0" than a change of this bit value. Refer to Figure 6 for more information.

B1 … Event detection indicator for SLIC2 (Read-only bit) 0 : detected 1 : not detected
By reading the state of this bit, the input level to the $\overline{DET2}$ pin can be determined.
If this bit is cleared, the $\overline{DET2}$ pin is a logic “0”. If this bit is set, the $\overline{DET2}$ pin is a logic “1”.

When the SLIC connected to channel 2 is an Intersil RSLIC™ series device, an assigned event of off-hook, ring trip or ground key can be detected by connecting the $\overline{DET2}$ pin of the ML7033 directly to the corresponding output pin of the SLIC device.

The event detected by the the SLIC is determined by the F2_2, F1_2, F0_2 (CR13-B7 to B5), and E0_2 (CR13-B2) bits.

When a debounce timer is enabled by a setting with the DET2TIM3 through DET2TIM0 bits (CR4-B7 to B4), the DET2 (CR13-B1) bit is held unchanged for a set period, even when the DET2 pin changes from a logic “1” to a logic “0”.

B0 … Thermal Shutdown Alarm indicator for SLIC2 (Read-only bit) 0 : detect 1 : not detect

By reading the state of this bit, the input level to the ALM2 pin can be determined.
If this bit is cleared, the $\overline{ALM2}$ pin is a logic “0”. If this bit is set, the $\overline{ALM2}$ pin is a logic “1”.

When the SLIC connected to channel 2 is an Intersil RSLIC™ series device, connecting the $\overline{ALM2}$ pin directly to the corresponding output pin of the SLIC device allows the ML7033 to know whether the SLIC is in the normal operating mode, or in a thermal shutdown state.

CR14 (CH2 tone generator 2 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR14	AOUT2 SEL	CH2TG2 TX	CH2TG2 TOUT2	CH2TG2 LV3	CH2TG2 LV2	CH2TG2 LV1	CH2TG2 LV0	CH2TG2 _8
default	0	0	0	0	0	0	0	0

CR15 (CH2 tone generator 2 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR15	CH2TG2 _7	CH2TG2 _6	CH2TG2 _5	CH2TG2 _4	CH2TG2 _3	CH2TG2 _2	CH2TG2 _1	CH2TG2 _0
default	0	0	0	0	0	0	0	0

CR14-B7 … AOUT2P, AOUT2N output select
0 : Single-ended output with the AOUT2P pin with the AOUT2N pin at high impedance.
1 : Differential output with the AOUT2P and the AOUT2N pins.

B6 … CH2 tone generator output select 0 : to Rx side 1 : to Tx side

B5 … CH2 tone generator Rx side output pin select 0 : AOUT2 pin 1 : TOUT2 pin

B4 to B1 … CH2 TG2 output level setting
This 4-bit field determines the output level of TG2 on CH2. The output level ranges from –12 to +2 dBmO as shown in Table 17.

Table 17 Tone Generator 2 Level Setting

B4 TG2LV3	B3 TG2LV2	B2 TG2LV1	B1 TG2LV0	Level (dBm0)
0	0	0	0	OFF
0	0	0	1	–12.0
0	0	1	0	–11.0
0	0	1	1	–10.0
0	1	0	0	–9.0
0	1	0	1	–8.0
0	1	1	0	–7.0
0	1	1	1	–6.0
1	0	0	0	–5.0
1	0	0	1	–4.0
1	0	1	0	–3.0
1	0	1	1	–2.0
1	1	0	0	–1.0
1	1	0	1	0.0
1	1	1	0	+1.0
1	1	1	1	+2.0

CR14-B0, CR15-B7 to B0… CH2 TG2 frequency select

These 9 bits define the output frequency for TG2 on CH2. The frequency range is between 300 and 3400 Hz in 10 Hz intervals as shown in Table 18.

The output frequency is calculated using the following formula:

Binary data for CR14-B0, CR15-B7 to B0
= (Output Frequency [Hz])/10

The following example shows how to program the output frequency when the intended frequency is 1500 Hz;

Ex) (Output Frequency [Hz]) / 10 = 1500/10 = 150d = 10010110b
Bits to set in CR14-B0, CR15-B7 to B0 = (0,1,0,0,1,0,1,1,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 300 and 3400 Hz.

Table 18 Tone Generator Frequency Setting

Frequency (Hz)	decimal	hex	CR14	CR15							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

CR16 (CH2 tone generator 1 control1)

	B7	B6	B5	B4	B3	B2	B1	B0
CR16	CH2TG1 LV6	CH2TG1 LV5	CH2TG1 LV4	CH2TG1 LV3	CH2TG1 LV2	CH2TG1 LV1	CH2TG1 LV0	CH2TG1 _8
default	0	0	0	0	0	0	0	0

CR17 (CH2 tone generator 1 control2)

	B7	B6	B5	B4	B3	B2	B1	B0
CR17	CH2TG1 _7	CH2TG1 _6	CH2TG1 _5	CH2TG1 _4	CH2TG1 _3	CH2TG1 _2	CH2TG1 _1	CH2TG1 _0
default	0	0	0	0	0	0	0	0

CR16-B7 to B1 … CH2 TG1 output level setting

This 7-bit field defines the output level of tone generator 1 on channel 2. The output level ranges from –12.1 to +0.5 dBm0 in 0.1 dBm0 intervals as shown in Table 19. A value of 0 in this field disables the tone generator.

The output level is calculated using the following formula.

Binary data for CR16- B7 to B1
= [(Output Level [dBm0]) + 12.2]*10

The following example shows how to program this field when the intended output level is –5.8 dBm0;

Ex) [(Output Level [dBm0]) + 12.2]*10 = (–5.8 + 12.2)*10 = 64d = 1000000b
Bits to set in CR9-B7 to B1 = (1,0,0,0,0,0,0)

Table 19 Tone Generator 1 Level Setting

B7 TG1LV6	B6 TG1LV5	B5 TG1LV4	B4 TG1LV3	B3 TG1LV2	B2 TG1LV1	B1 TG1LV0	Level (dBm0)
0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	1	–12.1
0	0	0	0	0	1	0	–12.0
0	0	0	0	0	1	1	–11.9
0	0	0	0	1	0	0	–11.8
:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	–5.9
1	0	0	0	0	0	0	–5.8
1	0	0	0	0	0	1	–5.7
:	:	:	:	:	:	:	:
1	1	1	1	0	1	0	0.0
1	1	1	1	0	1	1	0.1
1	1	1	1	1	0	0	0.2
1	1	1	1	1	0	1	0.3
1	1	1	1	1	1	0	0.4
1	1	1	1	1	1	1	0.5 (= 1.25 V_{op})

CR16-B0, CR17-B7 to B0 … CH2 TG1 frequency select

When the CH2RING (CR11-B7) bit is cleared, this 9-bit field is valid and determines the output frequency from tone generator 1 on channel 2. The frequency range is between 300 and 3400 Hz at 10 Hz intervals as shown in Table 20.

The output level is calculated using the following formula.

Binary data for CR16-B0, CR17-B7 to B0
= (Output Frequency [Hz])/10

The following is an example of how to program this register field when the intended frequency is 1500 Hz;

Ex) (Output Frequency [Hz]) / 10 = 1500/10 = 150d = 10010110b
Bits to set in CR16-B0, CR17-B7 to B0 = (0,1,0,0,1,0,1,1,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 300 and 3400 Hz.

Table 20 Tone Generator Frequency Setting (CH2RING bit = "0")

Frequency (Hz)	decimal	hex	CR16	CR17							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
300	30	01Eh	0	0	0	0	1	1	1	1	0
310	31	01Fh	0	0	0	0	1	1	1	1	1
320	32	020h	0	0	0	1	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
400	40	028h	0	0	0	1	0	1	0	0	0
410	41	029h	0	0	0	1	0	1	0	0	1
:	:	:	:	:	:	:	:	:	:	:	:
1000	100	064h	0	0	1	1	0	0	1	0	0
1010	101	065h	0	0	1	1	0	0	1	0	1
:	:	:	:	:	:	:	:	:	:	:	:
2000	200	0C8h	0	1	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3000	300	12Ch	1	0	0	1	0	1	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
3390	339	153h	1	0	1	0	1	0	0	1	1
3400	340	154h	1	0	1	0	1	0	1	0	0

When the CH2RING (CR11-B7) bit is set, the setting of the CH2TG1_8 (CR16-B0) bit and the CH2TG1_7 to CH2TG1_6 (CR16-B7 to B6) bits are ignored, and the CH2TG1_5 to CH2TG1_0 (CR16-B5 to B0) field defines the ringing tone frequency.

When the CH2RING (CR11-B7) bit is set, the frequency range is between 15 and 50 at 1 Hz intervals as shown in Table 21.

The output frequency is calculated using the following formula.

Binary data for CR17-B5 to B0
= (Output Frequency [Hz])

The following example shows how to program this register field when the intended frequency is 20 Hz;

Ex) Output Frequency [Hz] = 20d = 010100b
Bits to set in CR17-B5 to B0 = (0,1,0,1,0,0)

Note that the operations are not guaranteed when these bits define a frequency out of a band between 15 and 50 Hz.

Table 21 Tone Generator Frequency Setting (CH2RING bit = "1")

Frequency (Hz)	decimal	hex	CR16	CR17							
			B0	B7	B6	B5	B4	B3	B2	B1	B0
15	15	0Fh	—	—	—	0	0	1	1	1	1
16	16	10h	—	—	—	0	1	0	0	0	0
17	17	11h	—	—	—	0	1	0	0	0	1
18	18	12h	—	—	—	0	1	0	0	1	0
19	19	13h	—	—	—	0	1	0	0	1	1
20	20	14h	—	—	—	0	1	0	1	0	0
:	:	:	:	:	:	:	:	:	:	:	:
48	48	30h	—	—	—	1	1	0	0	0	0
49	49	31h	—	—	—	1	1	0	0	0	1
50	50	32h	—	—	—	1	1	0	0	1	0

CR18 (Test control)

	B7	B6	B5	B4	B3	B2	B1	B0
CR18	CH2 LOOP1	CH2 LOOP0	CH1 LOOP1	CH1 LOOP0	TEST3	TEST2	TEST1	TEST0
default	0	0	0	0	0	0	0	0

B7, B6 … CH2 loop-back test mode select
(B7, B6):
(0, 0) = Loop-back OFF
(0, 1) = Loop-back OFF
(1, 0) = Channel 2 digital loop-back test. PCM data output on the PCMOUT pin during normal operation is internally looped back through the Receive path via the PCMIN pin. In digital loop-back test mode, input data on PCMIN pin is ignored, but PCM data continues to be output on the PCMOUT pin.
(1, 1) = Channel 2 analog loop-back test. Analog signals output on the AOUT2P pin (or the AOUT2P and AOUT2N pins) are internally looped back to the transmit path behind a built-in feedback amplifier located after the AIN2P, AIN2N and GSX2 pins. In this mode, the AIN2P and AIN2N input pins are ignored. However, analog signals continue to be output on the AOUT2P pin (or the AOUT2P and the AOUT2N pins).

A loop-back test is functional only if XSYNC and RSYNC are from the same clock source.

B5, B4 … CH1 loop-back test mode select
(B5, B4):
(0, 0) = Loop-back OFF
(0, 1) = Loop-back OFF
(1, 0) = Channel 1 digital loop-back test. PCM data is output on the PCMOUT pin in normal operation is internally looped back through the Receive path via the PCMIN pin. In loop-back test mode, input data on PCMIN pin is ignored. However, PCM data can be output on the PCMOUT pin.
(1, 1) = Channel 1 analog loop-back test. Analog signals output on the AOUT1P pin (or from the AOUT1P and the AOUT1N pins) are internally looped back to the transmit path via a built-in feedback amplifier located after the AIN1P, AIN1N and GSX1 pins. In this mode, the AIN1P and AIN1N input pins are ignored. However, analog signals can be output from the AOUT1P pin (or from the AOUT1P and the AOUT1N pins).

A loop-back test is functional if XSYNC and RSYNC are from the same clock source.

B3 to B0 … LSI test registers for an LSI manufacturer
The default alternation is prohibited. When a write action is executed for CR18, set all of these bits to “0”.

CR19 (LSI manufacturer's test control)

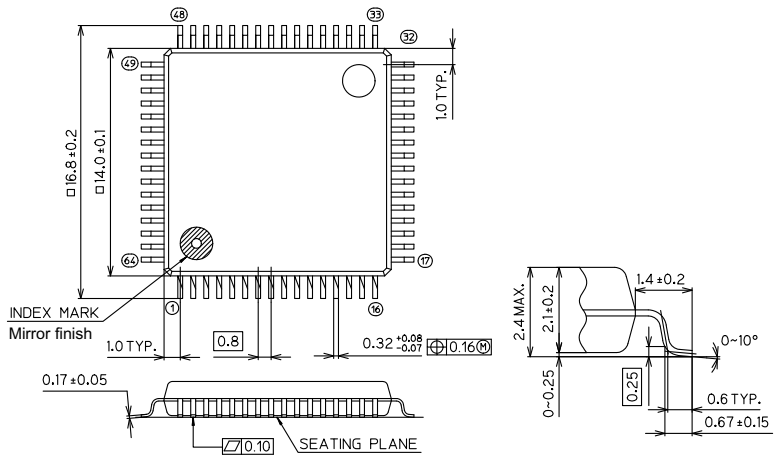
	B7	B6	B5	B4	B3	B2	B1	B0
CR19	TEST11	TEST10	TEST9	TEST8	TEST7	TEST6	TEST5	TEST4
default	0	0	0	0	0	0	0	0

B7 to B0 … LSI test registers for an LSI manufacturer
For manufacturing use only. Both reads and writes to this register are prohibited.

PACKAGE DIMENSIONS

(Unit: mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7033-02	Dec. 2001	–	–	Final edition 2
FEDL7033-03	Jun. 8, 2007	12	12	Added t_{12} Corrected values of Serial Port I/O Setting Time
		16	16	Added t_{12} Corrected Figure 5 Serial Interface
		–	51	Added “Revision History”
FEDL7033-04	Oct. 13, 2011	–	–	Company Name Change

NOTES

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