

CMOS 16-bit Single Chip Microcomputer

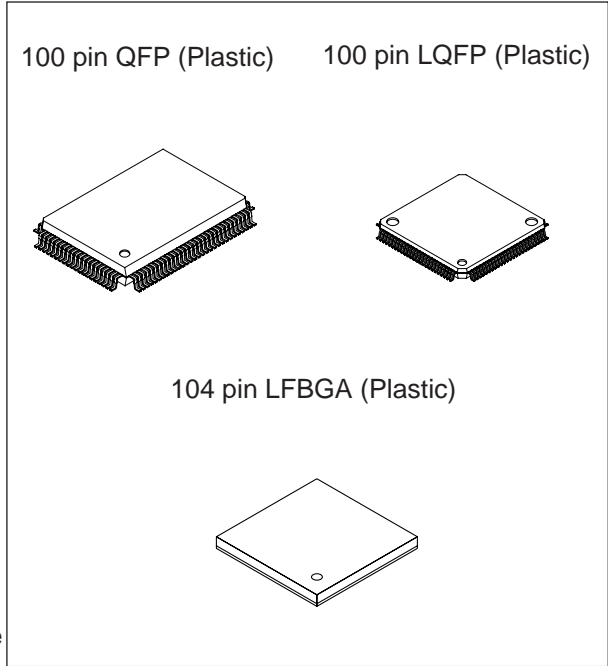
Description

The CXP912032 is a CMOS 16-bit micro-computer integrating on a single chip an A/D converter, serial interface with an incorporated buffer RAM, high-precision timing pattern generation function, pulse cycle measurement circuit, PWM generator, general-purpose prescaler, vertical sync separation circuit, and a measurement circuit which measures the signals of capstan FG, drum FG/PG, reel FG and other servo systems with high precision, as well as basic configurations like a 16-bit CPU, ROM, RAM, and I/O port.

This LSI also provides sleep/stop modes that enable lower power consumption.

Features

- An efficient instruction set as a controller
 - Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
 - Highly quadratic instruction system, general-purpose register of 16-bit × 8-pin × 16-bank configuration
- Minimum instruction cycle time 100ns at 20MHz operation
- Incorporated ROM capacity 128K bytes
- Incorporated RAM capacity 6144 bytes
- Peripheral functions
 - A/D converter
 - Serial interface
 - Timers
 - High-precision timing pattern generator
 - PWM/DA gate output
 - Servo input control
 - VSYNC separator
 - FRC capture unit
 - PWM output
 - General-purpose prescaler
 - Pulse cycle measurement circuit
- General-purpose I/O
- Interruption
- Standby mode
- Package
- Piggyback/evaluation chip



Structure

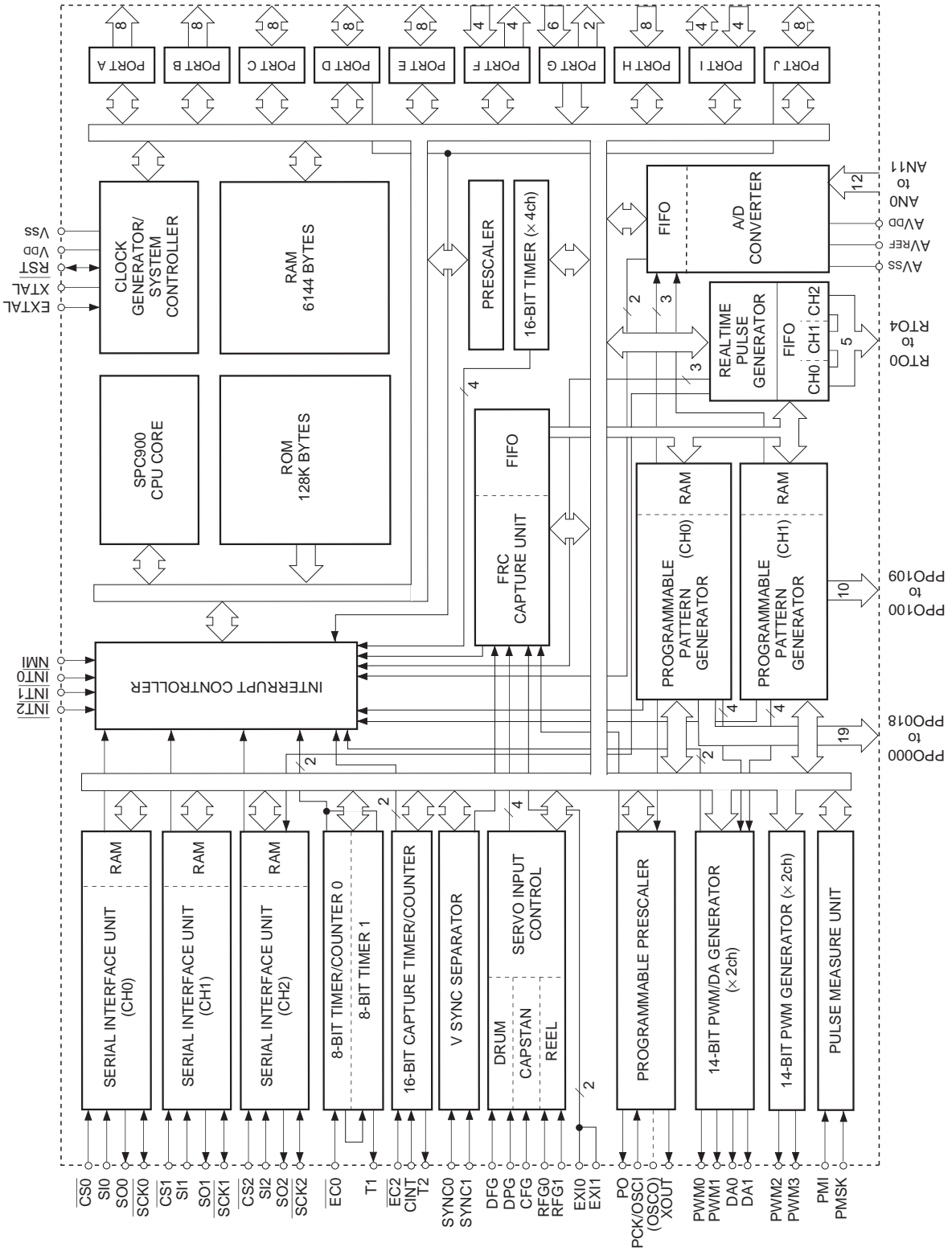
Silicon gate CMOS IC

8-bit 12-channel successive approximation system, automatic scanning function, 8-stage (soft) + 4-stage (hard) FIFO for conversion results (Conversion time: 20µs at 20MHz)
 Buffer RAM (128 bytes, supports high-speed transfer mode), 3 channels
 8-bit timer/counter + 8-bit timer (with timing output), 1 channel
 16-bit capture timer/counter (with timing output), 1 channel
 16-bit timer, 4 channels
 PPG for 27 pins, 42 stages (max.)
 PPG for 16 pins, 16 stages (max.)
 RTG for 5 pins, 3 channels
 PWM for 14 bits, 2 channels
 (Repetitive frequency of 39.1kHz, 20MHz)
 DA gate pulse for 14 bits, 2 channels
 Capstan FG, drum FG/PG, reel FG

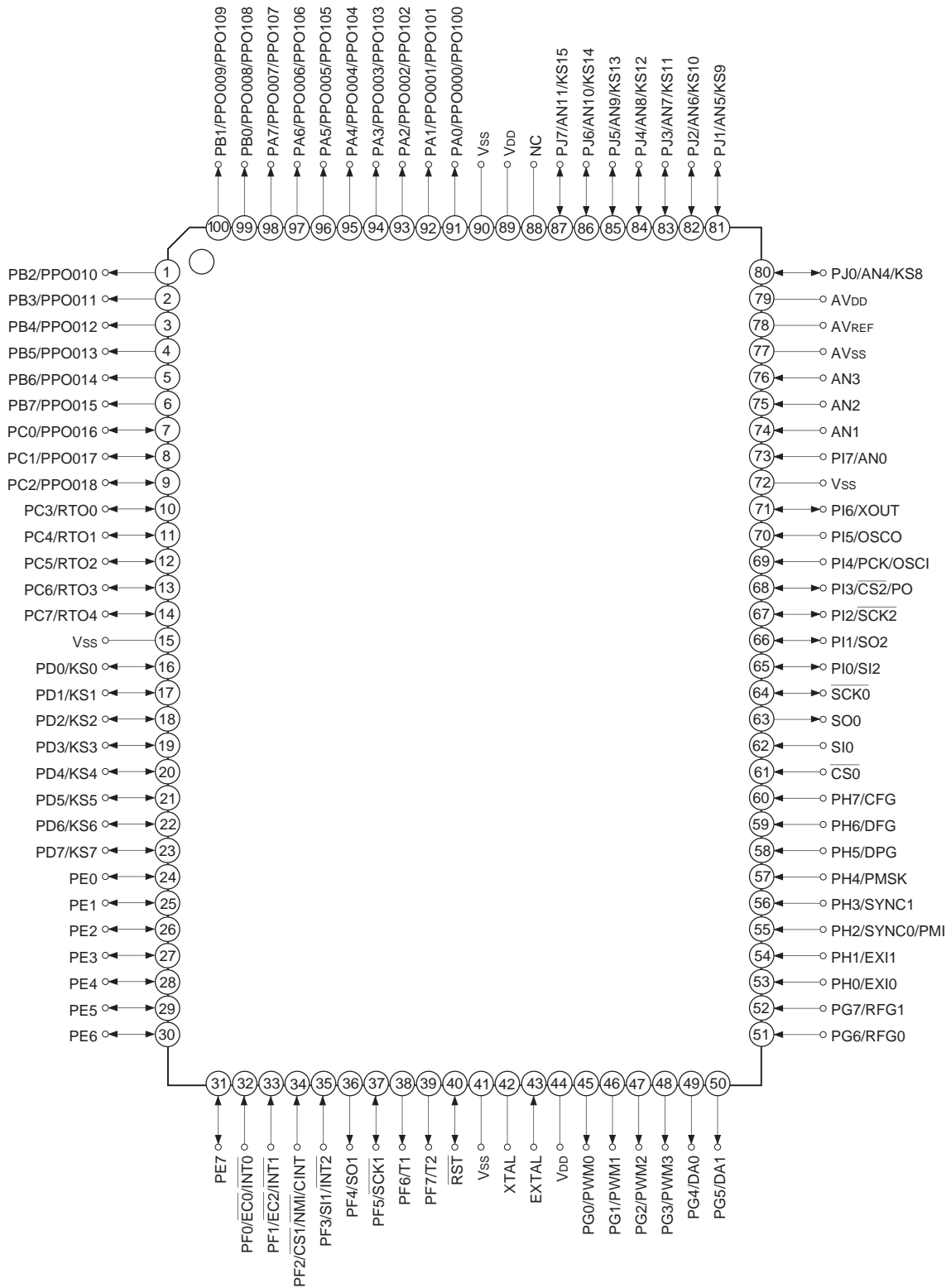
24-bit and 8-stage FIFO
 14 bits, 2 channels
 10 bits, 1 channel
 1 channel with mask input
 80 pins
 (max.; when all multi-purpose pins are used as general-purpose I/O.)
 28 factors, 28 vectors, multi-interruption and priority selection possible
 Sleep/stop
 100-pin plastic QFP/LQFP, 104-pin plastic LFBGA
 CXP912000 100-pin ceramic QFP/LQFP

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram

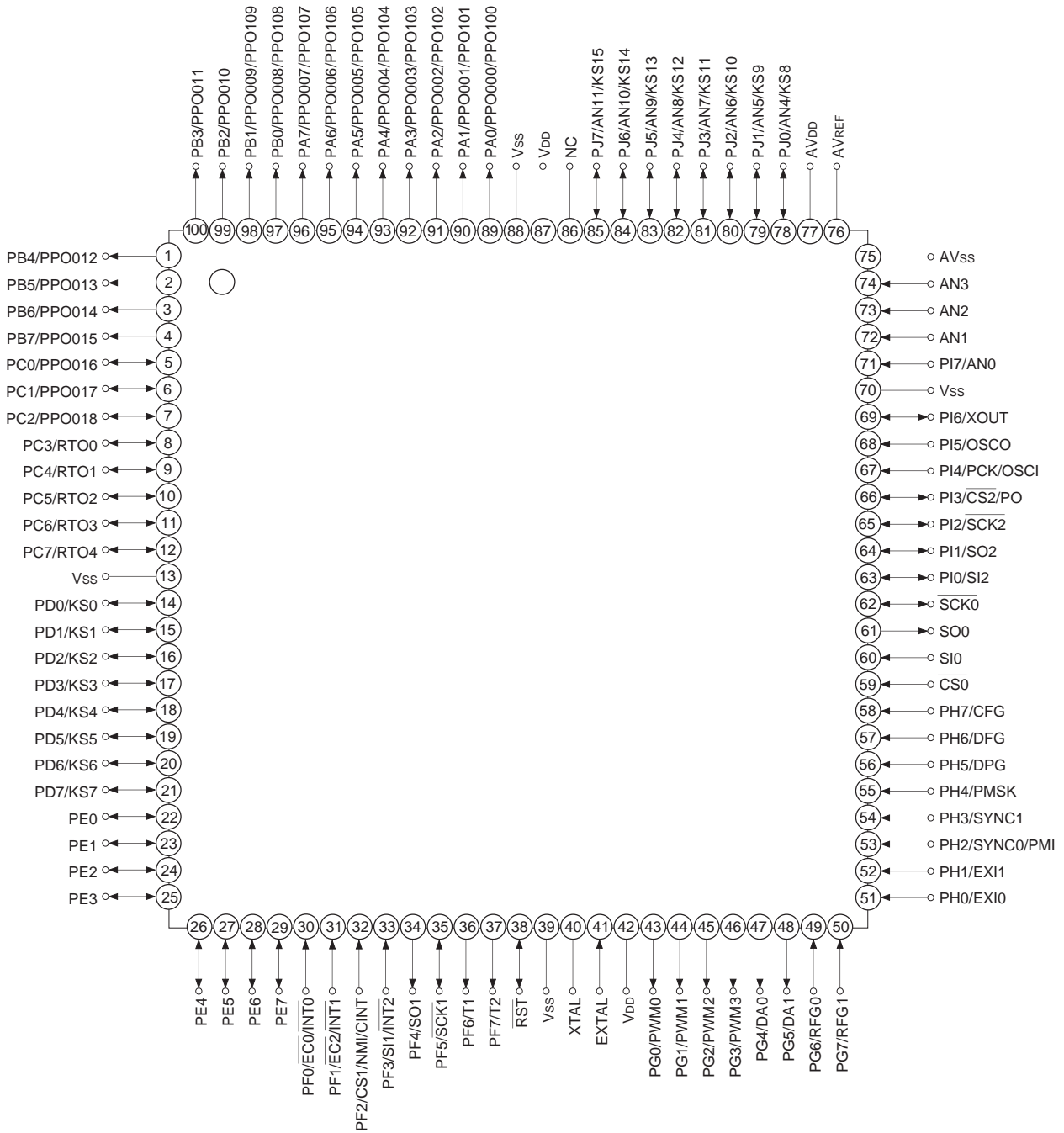


Pin Configuration 1 (Top View) 100-pin QFP Package



- Note**
1. Vss (Pins 15, 41, 72 and 90) must be connected to GND.
 2. VDD (Pins 44 and 89) must be connected to VDD.
 3. NC (Pin 88) is left open.

Pin Configuration 2 (Top View) 100-pin LQFP Package



- Note)** 1. Vss (Pins 13, 39, 70 and 88) must be connected to GND.
 2. VDD (Pins 42 and 87) must be connected to VDD.
 3. NC (Pin 86) is left open.

Pin Configuration 3 (Top View) 104-pin LFBGA Package

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	(A1) NC		(A3) PB1	(A4) PA7	(A5) PA4	(A6) PA1	(A7) Vss	(A8) NC	(A9) PJ5	(A10) PJ2	(A11) PJ0		(A13) NC
B			(B3) PB2	(B4) PB0	(B5) PA5	(B6) PA2	(B7) VDD	(B8) PJ7	(B9) PJ4	(B10) PJ1	(B11) AVDD		
C	(C1) PB6	(C2) PB5		(C4) PB3	(C5) PA6	(C6) PA3	(C7) PA0	(C8) PJ6	(C9) PJ3	(C10) AVREF		(C12) AN3	(C13) AN2
D	(D1) PC0	(D2) PB7	(D3) PB4								(D11) AVss	(D12) AN1	(D13) PI7
E	(E1) PC3	(E2) PC2	(E3) PC1								(E11) Vss	(E12) PI6	(E13) PI5
F	(F1) PC6	(F2) PC5	(F3) PC4								(F11) PI4	(F12) PI3	(F13) PI2
G	(G1) Vss	(G2) PC7	(G3) PD0								(G11) PI1	(G12) SCK0	(G13) PI0
H	(H1) PD1	(H2) PD2	(H3) PD3								(H11) CS0	(H12) SI0	(H13) SO0
J	(J1) PD4	(J2) PD5	(J3) PD6								(J11) PH5	(J12) PH6	(J13) PH7
K	(K1) PD7	(K2) PE0	(K3) PE3								(K11) PH0	(K12) PH3	(K13) PH4
L	(L1) PE1	(L2) PE2		(L4) PE4	(L5) PF1	(L6) PF4	(L7) Vss	(L8) VDD	(L9) PG2	(L10) PG7		(L12) PH1	(L13) PH2
M			(M3) PE5	(M4) PE7	(M5) PF2	(M6) PF5	(M7) PF7	(M8) EXTAL	(M9) PG1	(M10) PG4	(M11) PG6		
N	(N1) NC		(N3) PE6	(N4) PF0	(N5) PF3	(N6) PF6	(N7) RST	(N8) XTAL	(N9) PG0	(N10) PG3	(N11) PG5		(N13) NC

- Note)**
1. Vss (Pins A7, E11, G1 and L7) must be connected to GND.
 2. VDD (Pins B7 and L8) must be connected to VDD.
 3. NC (Pins A1, A13, N1, N13 and A8) are left open.
 4. A1, A13, N1 and N13 pins are reinforced balls.

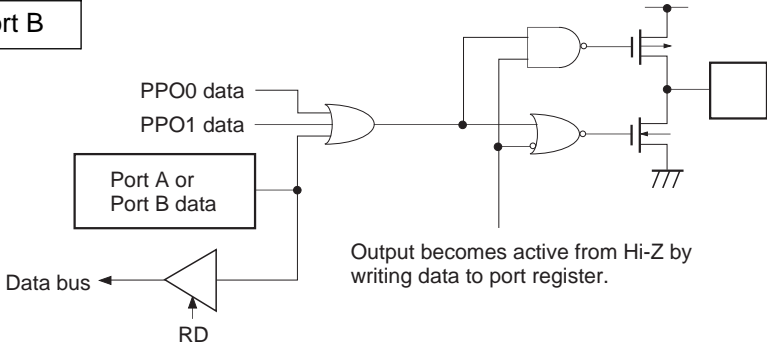
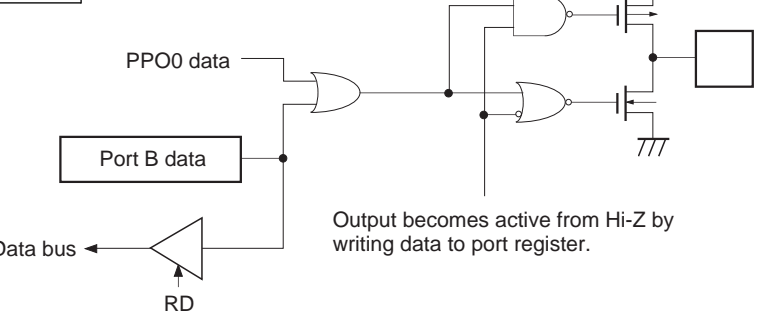
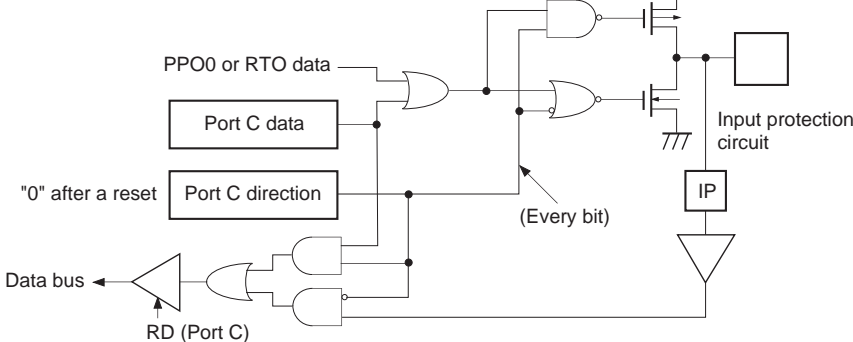
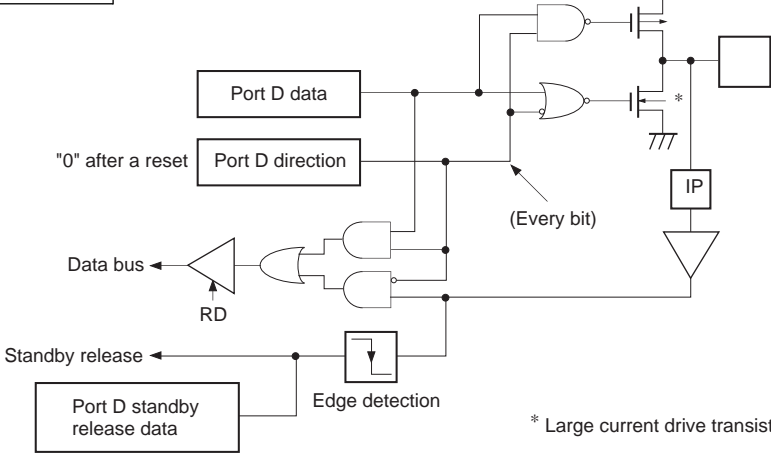
Pin Description

Symbol	I/O	Functions			
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107	Output / Real time output / Real time output	(Port A) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG0, PPG1) output. Functions as high-precision real-time pulse output port. (PPG0 19 pins, PPG1 10 pins)		
PB0/PPO008 /PPO108 PB1/PPO009 /PPO109	Output / Real time output / Real time output	(Port B) 8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output. (8 pins)			
PB2/PPO010 to PB7/PPO015	Output / Real time output				
PC0/PPO016 to PC2/PPO018	Output / Real time output	(Port C) 8-bit I/O port. I/O can be specified by bit unit. Data is gated with PPO0 or RTO contents by OR-gate and they are output. (8 pins)			Real-time pulse generator (RTG) output. Functions as high-precision real-time pulse output port. (5 pins)
PC3/RTO0 to PC7/RTO4	Output / Real time output				
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be specified by bit unit. Standby release input function can also be specified by bit unit. Can drive 12mA sync current when V _{DD} = 5V. (8 pins)			
PE0 to PE7	I/O	(Port E) 8-bit I/O port. I/O can be specified by bit unit. Can drive 12mA sync current when V _{DD} = 5V. (8 pins)			
PF0/ $\overline{\text{EC0}}$ / INT0	Input / Input / Input	(Port F) 8-bit port. Lower 4 bits are for input; upper 4 bits are for output. (8 pins)	External event input for timer/counter. (2 pins)	Input to request external interruption. Active at the falling edge. (2 pins)	
PF1/ $\overline{\text{EC2}}$ / INT1	Input / Input / Input		Serial chip select (CH1) input.	Input to request non-maskable interruption. Active at the falling edge.	External capture input for 16-bit timer/counter.
PF2/ $\overline{\text{CS1}}$ / $\overline{\text{NMI}}$ / $\overline{\text{CINT}}$	Input / Input / Input / Input		Serial data (CH1) input.	Input to request external interruption. Active at the falling edge.	
PF3/SI1/ $\overline{\text{INT2}}$	Input / Input / Input		Serial data (CH1) output.		
PF4/SO1	Output / Output		Serial data (CH1) I/O.		
PF5/ $\overline{\text{SCK1}}$	Output / I/O		8-bit timer/counter output.		
PF6/T1	Output / Output		16-bit capture timer/counter output.		
PF7/T2	Output / Output				

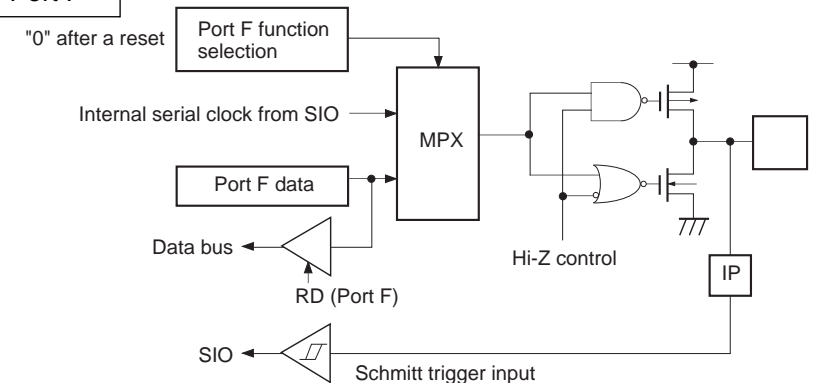
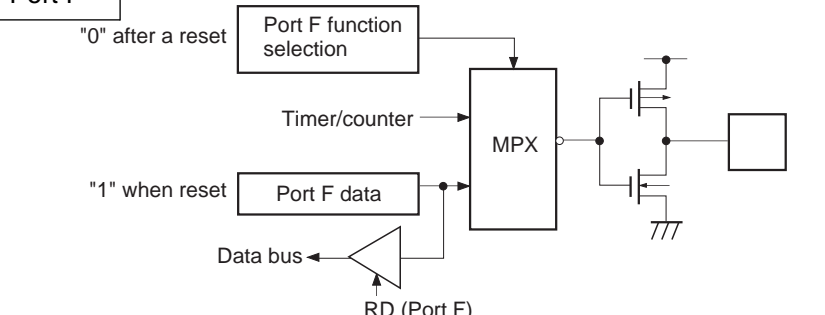
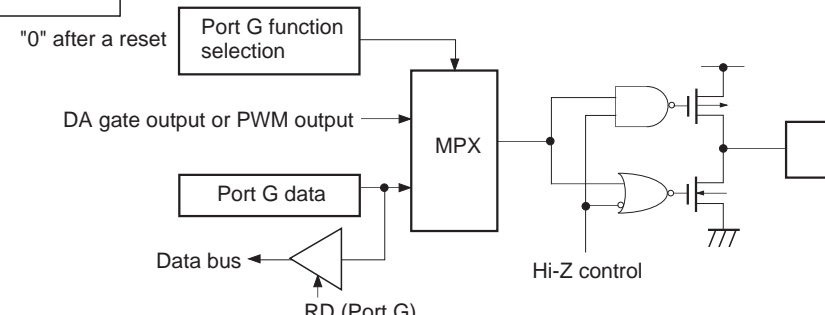
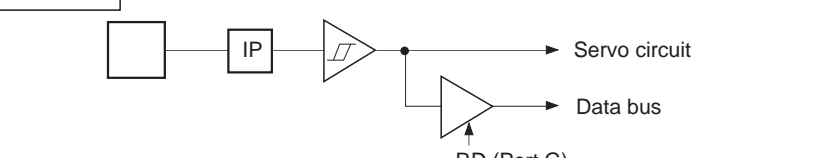
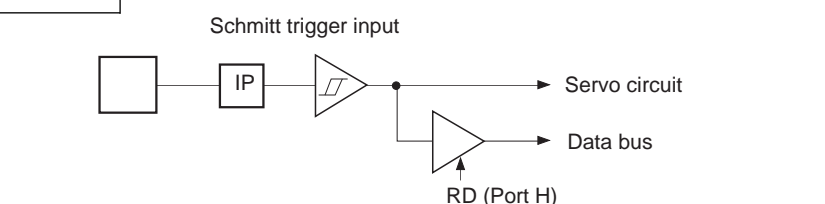
Symbol	I/O	Functions		
PG0/PWM0	Output / Output	(Port G) 8-bit port. Lower 6 bits are for output; upper 2 bits are for input. (8 pins)	14-bit PWM output. (4 pins)	
PG1/PWM1	Output / Output			
PG2/PWM2	Output / Output			
PG3/PWM3	Output / Output			
PG4/DA0	Output / Output		DA gate pulse output. (2 pins)	
PG5/DA1	Output / Output			
PG6/RFG0	Input / Input		Reel FG input. (2 pins)	
PG7/RFG1	Input / Input			
PH0/EXI0	Input / Input	(Port H) 8-bit input port. (8 pins)	External input for FRC capture unit. (2 pins)	
PH1/EXI1	Input / Input			
PH2/ SYNC0/PMI	Input / Input / Input		Composite sync signal input. (2 pins)	Pulse input for pulse cycle measurement circuit.
PH3/SYNC1	Input / Input		Mask input for pulse cycle measurement circuit.	
PH4/PMSK	Input / Input		Drum PG input.	
PH5/DPG	Input / Input		Drum FG input.	
PH6/DFG	Input / Input		Capstan FG input.	
PH7/CFG	Input / Input			
SCK0	I/O	Serial clock (CH0) I/O.		
SO0	Output	Serial data (CH0) output.		
SI0	Input	Serial data (CH0) input.		
CS0	Input	Serial chip select (CH0) input.		
PI0/SI2	I/O / Input	(Port I) 8-bit port. Lower 4 bits are for I/O; upper 4 bits are for input. Lower 4 bits can be specified by bit unit. (8 pins)	Serial data (CH2) input.	
PI1/SO2	I/O / Output		Serial data (CH2) output.	
PI2/SCK2	I/O / I/O		Serial clock (CH2) I/O.	
PI3/CS2/PO	I/O / Input / Output		Serial chip select (CH2) input.	General-purpose prescaler output.
PI4/PCK/ OSCI	Input / Input / Input		General-purpose prescaler external clock input.	Connects a crystal for general-purpose prescaler clock oscillation. (Mask option)
PI5/OSCO	Input / Output			
PI6/XOUT	Input / Output		Clock output from clock generator or general-purpose prescaler.	
PI7/AN0	Input / Input			
AN1 to AN3	Input			
PJ0/AN4 to PJ7/AN11	I/O / Input	(Port J) 8-bit I/O port. I/O can be specified by bit unit. Standby release input function can also be specified by bit unit. (8 pins)	Analog input for A/D converter. (12 pins)	

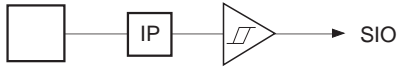
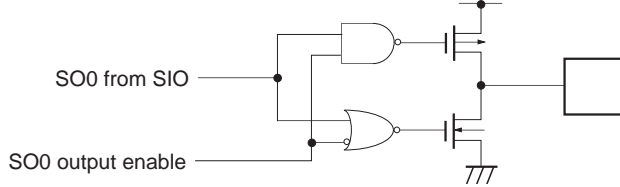
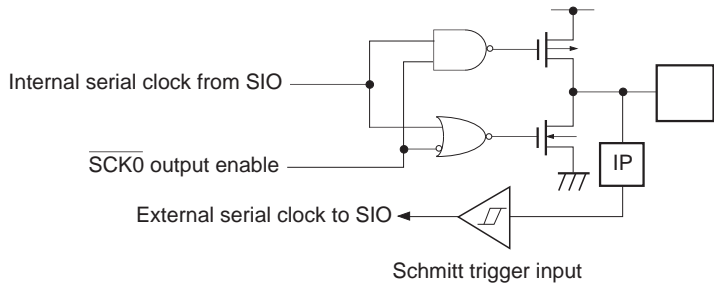
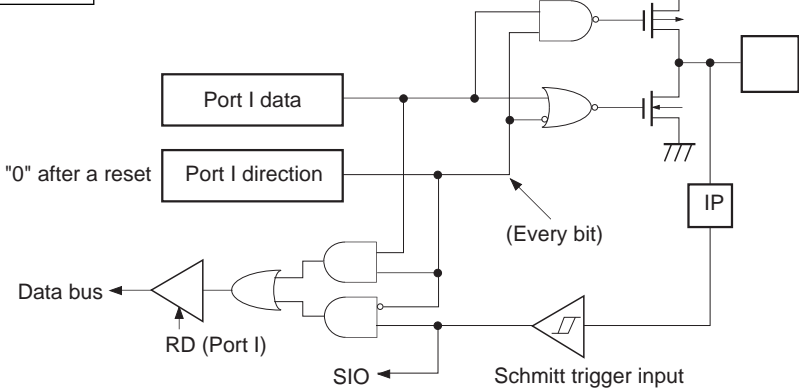
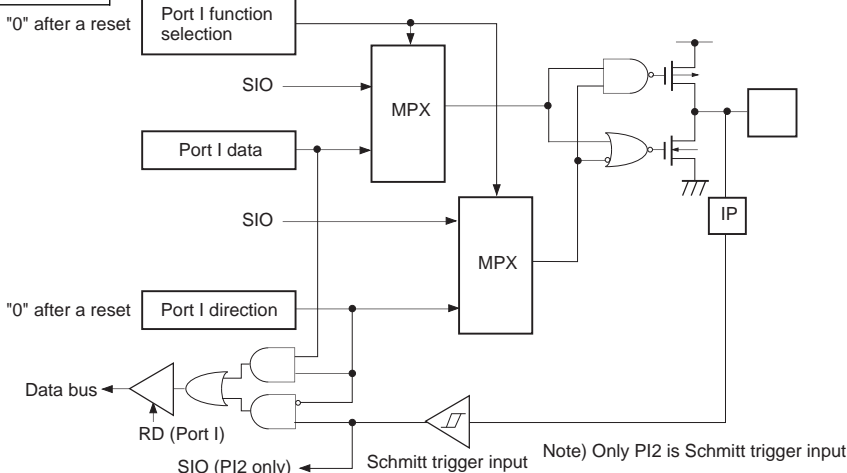
Symbol	I/O	Functions
EXTAL	Input	Connects a crystal for system clock oscillation. When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.
XTAL	Output	
$\overline{\text{RST}}$	I/O	System reset. Active at "L" level.
AV _{DD}		Positive power supply for A/D converter.
AV _{REF}	Input	Reference voltage input for A/D converter.
AV _{SS}		A/D converter GND.
V _{DD}		Positive power supply. All three V _{DD} pins must be connected to the positive power supply.
V _{SS}		GND. All four V _{SS} pins must be connected to GND.

I/O Circuit Format for Pins

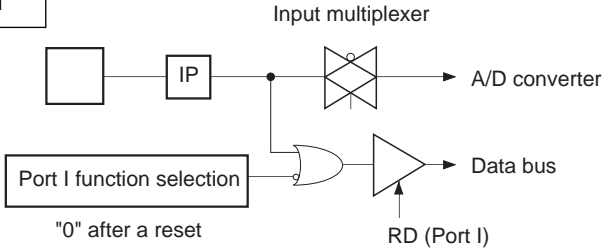
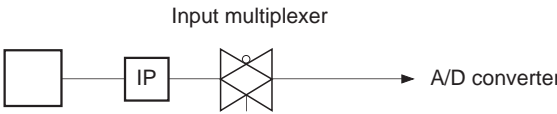
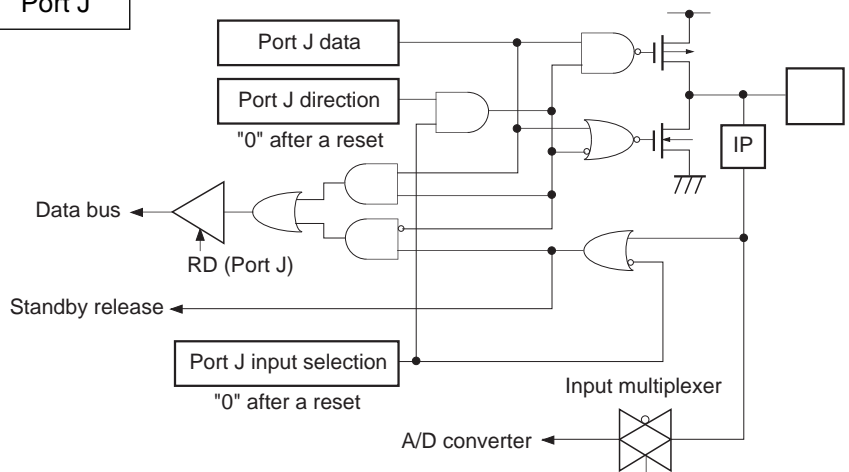
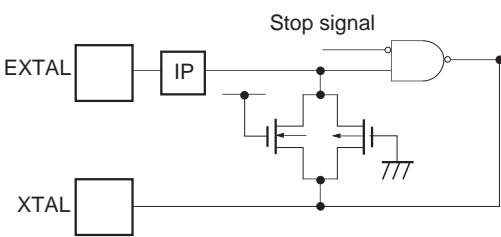
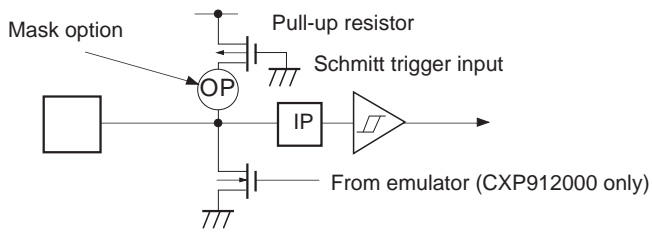
Pin	Circuit format	After a reset
<p>PA0/PPO000/ PPO100 to PA7/PPO007/ PPO107</p> <p>PB0/PPO008/ PPO108 to PB1/PPO009/ PPO109</p> <p>10 pins</p>	<p>Port A</p> <p>Port B</p>  <p>Output becomes active from Hi-Z by writing data to port register.</p>	<p>Hi-Z</p>
<p>PB2/PPO010 to PB7/PPO015</p> <p>6 pins</p>	<p>Port B</p>  <p>Output becomes active from Hi-Z by writing data to port register.</p>	<p>Hi-Z</p>
<p>PC0/PPO016 to PC2/PPO018</p> <p>PC3/RTO0 to PC7/RTO4</p> <p>8 pins</p>	<p>Port C</p>  <p>Input protection circuit</p> <p>"0" after a reset</p> <p>(Every bit)</p> <p>RD (Port C)</p>	<p>Hi-Z</p>
<p>PD0/KS0 to PD7/KS7</p> <p>8 pins</p>	<p>Port D</p>  <p>"0" after a reset</p> <p>(Every bit)</p> <p>RD</p> <p>Standby release</p> <p>Edge detection</p> <p>* Large current drive transistor</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PE0 to PE7</p> <p>8 pins</p>	<p>Port E</p> <p>Port E data</p> <p>"0" after a reset Port E direction</p> <p>(Every bit)</p> <p>Data bus</p> <p>RD</p> <p>* Large current drive transistor</p>	<p>Hi-Z</p>
<p>PF0/$\overline{\text{EC0}}$/INT0 PF1/$\overline{\text{EC2}}$/INT1 PF3/SI1/INT2</p> <p>3 pins</p>	<p>Port F</p> <p>Schmitt trigger input</p> <p>Interrupt circuit and timer/counter or SIO</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>Hi-Z</p>
<p>PF2/$\overline{\text{CS1}}$/ NMI/CINT</p> <p>1 pin</p>	<p>Port F</p> <p>"0" after a reset Port F function selection</p> <p>Schmitt trigger input</p> <p>Interrupt circuit</p> <p>Timer/counter or SIO</p> <p>Data bus</p> <p>RD (Port F)</p>	<p>Hi-Z</p>
<p>PF4/SO1</p> <p>1 pin</p>	<p>Port F</p> <p>"0" after a reset Port F function selection</p> <p>SO1 from SIO</p> <p>MPX</p> <p>Port F data</p> <p>Data bus</p> <p>RD (Port F)</p> <p>Hi-Z control</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PF5/SCK1</p> <p>1 pin</p>	<p>Port F</p> <p>"0" after a reset</p> 	<p>Hi-Z</p>
<p>PF6/T1 PF7/T2</p> <p>2 pins</p>	<p>Port F</p> <p>"0" after a reset</p> 	<p>"H" level</p>
<p>PG0/PWM0 PG1/PWM1 PG2/PWM2 PG3/PWM3 PG4/DA0 PG5/DA1</p> <p>6 pins</p>	<p>Port G</p> <p>"0" after a reset</p> 	<p>Hi-Z</p>
<p>PG6/RFG0 PG7/RFG1</p> <p>2 pins</p>	<p>Port G</p> <p>Schmitt trigger input</p> 	<p>Hi-Z</p>
<p>PH0/EXI0 PH1/EXI1 PH2/SYNC0/PMI PH3/SYNC1 PH4/PMSK PH5/DPG PH6/DFG PH7/CFG</p> <p>8 pins</p>	<p>Port H</p> <p>Schmitt trigger input</p>  <p>Note) PH2/SYNC0/PMI and PH3/SYNC1 can select CMOS Schmitt trigger input or TTL Schmitt trigger input with the mask option.</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>$\overline{\text{CS0}}$ SIO</p> <p>2 pins</p>	<p>Schmitt trigger input</p> 	<p>Hi-Z</p>
<p>SO0</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>Port I</p> <p>PI0/SI2</p> <p>1 pin</p>		<p>Hi-Z</p>
<p>Port I</p> <p>PI1/SO2 PI2/SCK2</p> <p>2 pins</p>	 <p>Note) Only PI2 is Schmitt trigger input.</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PI3/$\overline{\text{CS2}}$/PO</p> <p>1 pin</p>	<p>Port I</p> <p>"0" after a reset</p> <p>Port I function selection</p> <p>General-purpose prescaler</p> <p>MPX</p> <p>Port I data</p> <p>"0" after a reset</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>SIO</p> <p>Schmitt trigger input</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI4/PCK/OSCI</p> <p>PI5/OSCO</p> <p>2 pins</p>	<p>Port I</p> <p>"0" after a reset</p> <p>Port I function selection</p> <p>OSCI</p> <p>IP</p> <p>General-purpose prescaler</p> <p>OSCO</p> <p>Fig. 1.</p> <p>PI4/PCK or PI5</p> <p>IP</p> <p>General-purpose prescaler</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Fig. 2.</p> <p>Note) The circuit format in Fig. 1 or Fig. 2 can be selected with the mask option.</p>	<p>Oscillation</p> <p>Hi-Z</p>
<p>PI6/XOUT</p> <p>1 pin</p>	<p>Port I</p> <p>"0" after a reset</p> <p>Port I function selection</p> <p>Clock generator</p> <p>General-purpose prescaler</p> <p>MPX</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PI7/AN0</p> <p>1 pin</p>	<p>Port I</p>  <p>Input multiplexer</p> <p>A/D converter</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Port I function selection</p> <p>"0" after a reset</p>	<p>Hi-Z</p>
<p>AN1 to AN3</p> <p>3 pins</p>	 <p>Input multiplexer</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>PJ0/AN4/KS8 to PJ7/AN11/KS15</p> <p>8 pins</p>	<p>Port J</p>  <p>Port J data</p> <p>Port J direction</p> <p>"0" after a reset</p> <p>Data bus</p> <p>RD (Port J)</p> <p>Standby release</p> <p>Port J input selection</p> <p>"0" after a reset</p> <p>Input multiplexer</p> <p>A/D converter</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <p>EXTAL</p> <p>XTAL</p> <p>Stop signal</p> <p>IP</p> <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop mode. 	<p>Osillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt trigger input</p> <p>IP</p> <p>From emulator (CXP912000 only)</p>	<p>"L" level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	All pins excluding large current output pins
	I _{OLC}	20	mA	Large current output pins* ³
Low level total output current	∑I _{OL}	130	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package
		380		LQFP package
		500		LFPGA package

*1 AV_{DD} and V_{DD} must be the same voltage.

*2 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*3 Nch transistors of PD and PE output ports are the large current drive transistors.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	2.7	5.5	V	Guaranteed operation range for high-speed mode (1/2 frequency dividing clock)
		2.7	5.5	V	Guaranteed operation range for low-speed mode (1/16 frequency dividing clock)
		2.5	5.5	V	Guaranteed data hold range during stop mode
Analog voltage	AV _{DD}	2.7	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt trigger input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL Schmitt trigger input*4, *7
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*5
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
			0.2V _{DD}	V	*2, *6
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt trigger input*3
	V _{ILTS}	0	0.8	V	TTL Schmitt trigger input*4, *7
	V _{ILEX}	-0.3	0.4	V	EXTAL
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} must be the same voltage.

*2 PC, PD, PE, PI1, PI3 to PI7, PJ for normal input port

*3 $\overline{CS0}$, SI0, $\overline{SCK0}$, \overline{RST} , PF0/ $\overline{EC0}$ / $\overline{INT0}$, PF1/ $\overline{EC2}$ / $\overline{INT1}$, PF2/ $\overline{CS1}$ / \overline{NMI} / \overline{CINT} , PF3/SI1/ $\overline{INT2}$, PF5/ $\overline{SCK1}$, PG6/RFG0, PG7/RFG1, PH (PH2 and PH3 when CMOS Schmitt trigger input is selected with the mask option), PI0/SI2, PI2/ $\overline{SCK2}$.

*4 PH2 and PH3 (when TTL Schmitt trigger input is selected with the mask option).

*5 Specified only during external clock input.

*6 When the supply voltage (V_{DD}) is within the range of 2.7 to 3.6V.

*7 When the supply voltage (V_{DD}) is within the range of 4.5 to 5.5V.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PE, PF6 to PF7, PG0 to PG5, PI0, PI3, PI6, PJ	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
			VDD = 2.7V, IOH = -0.15mA	2.4			V
			VDD = 2.7V, IOH = -0.5mA	2.0			V
		PF4, PF5, PI1, PI2, SO0, SCK0	VDD = 4.5V, IOH = -4.0mA	3.6			V
			VDD = 3.0V, IOH = -4.0mA	2.0			V
Low level output voltage	VOL	PA to PC, PF4 to PF7, PG0 to PG5, PI0 to PI3, PI6, PJ, SO0, SCK0, RST*1	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
			VDD = 2.7V, IOL = 1.2mA			0.3	V
			VDD = 2.7V, IOL = 1.6mA			0.5	V
		PD, PE	VDD = 4.5V, IOL = 12.0mA			1.5	V
			VDD = 2.7V, IOL = 5.0mA			1.0	V
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
			VDD = 3.6V, VIH = 3.6V	0.3		20	μA
	IIIE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
			VDD = 3.6V, VIL = 0.3V	-0.3		-20	μA
	IILR	RST*2	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
			VDD = 3.6V, VIL = 0.3V	-0.9		-200	μA
I/O leakage current	IIZ	PA to PJ, AN1 to AN3, CS0, SI0, SO0, SCK0 RST*2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
			VDD = 3.6V, VI = 0, 3.6V			±10	μA
Supply current*3	IDD*4	VDD, VSS	20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 5V ± 10%		40	65	mA
			20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 3.3V ± 0.3V		22	40	mA
	IDDS1*5		20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 5V ± 10%, sleep mode		8	14	mA
			20MHz crystal oscillation (C1 = C2 = 10pF), VDD = 3.3V ± 0.3V, sleep mode		4.5	8	mA
	IDDS2		VDD = 5.5V, stop mode			10	μA
			VDD = 3.6V, stop mode			10	μA
Input capacitance	CIN	Pins other than VDD, VSS, AVDD, AVSS	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

- *1 $\overline{\text{RST}}$ is specified only in evaluation mode.
- *2 In $\overline{\text{RST}}$, the input current is specified when pull-up resistor is selected; the leakage current is specified when no resistor is selected.
- *3 When all output pins are open.
- *4 When the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (1/2 frequency dividing clock).
- *5 When the clock generator output is not selected at PI6.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL, EXTAL	Fig. 1, Fig. 2	VDD = 5.0V ± 10%	1	20	MHz
				VDD = 3.0V ± 10%	1	20	MHz
System clock input pulse width	t _{xH} , t _{xL}	EXTAL	Fig. 1, Fig. 2 External clock drive	VDD = 5.0V ± 10%	20		ns
				VDD = 3.0V ± 10%	20		ns
System clock input rise time, fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive	VDD = 5.0V ± 10%		200	ns
				VDD = 3.0V ± 10%		200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	PF0/ $\overline{\text{EC0}}$, PF1/ $\overline{\text{EC2}}$	Fig. 3	VDD = 5.0V ± 10%	t _{sys} + 50*		ns
				VDD = 3.0V ± 10%	t _{sys} + 100*		ns
Event count input clock rise time, fall time	t _{ER} , t _{EF}	PF0/ $\overline{\text{EC0}}$, PF1/ $\overline{\text{EC2}}$	Fig. 3	VDD = 5.0V ± 10%		20	ms
				VDD = 3.0V ± 10%		20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).
 t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

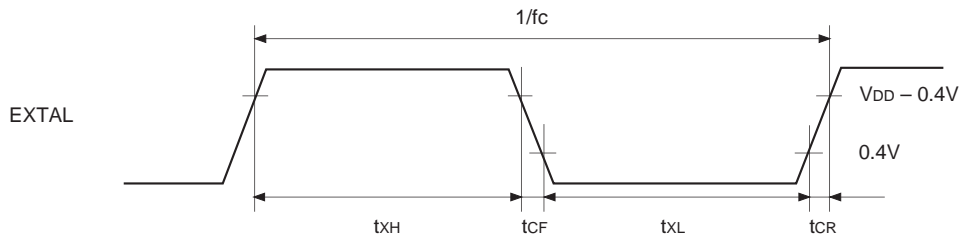


Fig. 1. Clock timing

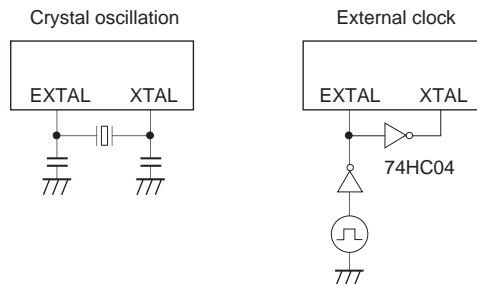


Fig. 2. Clock applied conditions

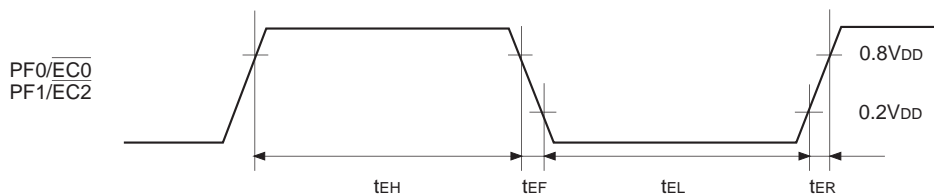


Fig. 3. Event count clock timing

(2) Serial interface (CH0, CH1, CH2)

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min	Max.	Unit
$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}, \overline{\text{SCK1}}, \overline{\text{SCK2}}$	Chip select transfer mode (SCK = output mode)	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}}$ float delay time	t_{DCSKF}	SO0, SO1, SO2	Chip select transfer mode (SCK = output mode)	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \downarrow \rightarrow \text{SO}$ delay time	t_{DCSO}	SO0, SO1, SO2	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}} \uparrow \rightarrow \text{SO}$ float delay time	t_{DCSOF}	$\overline{\text{CS0}}, \overline{\text{CS1}}, \overline{\text{CS2}}$	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 250$	
$\overline{\text{CS}}$ High level width	t_{WHCS}	$\overline{\text{SCK0}}, \overline{\text{SCK1}}, \overline{\text{SCK2}}$	Chip select transfer mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}, \overline{\text{SCK1}}, \overline{\text{SCK2}}$	Input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 200$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 200$	
			Output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	16000/fc	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	16000/fc	
$\overline{\text{SCK}}$ High, Low level width	$t_{\text{KH}}, t_{\text{KL}}$	$\overline{\text{SCK0}}, \overline{\text{SCK1}}, \overline{\text{SCK2}}$	Input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
			Output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	8000/fc - 50	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	8000/fc - 75	
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI0, SI1, SI2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	100	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	100	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$200 - t_{\text{sys}}$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$200 - t_{\text{sys}}$	
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI0, SI1, SI2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO0, SO1, SO2	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$t_{\text{sys}} + 150$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	50	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	100	
Minimum interval time	t_{INT}	$\overline{\text{SCK0}}, \overline{\text{SCK1}}, \overline{\text{SCK2}}$	$\overline{\text{SCK}}$ input mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 100$	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	$2t_{\text{sys}} + 125$	
			$\overline{\text{SCK}}$ output mode	$V_{\text{DD}} = 5.0\text{V} \pm 10\%$	8000/fc - 50	ns
				$V_{\text{DD}} = 3.0\text{V} \pm 10\%$	8000/fc - 75	

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{\text{SCK}}$ output mode, SO output delay time is 150pF when $V_{\text{DD}} = 5.0\text{V} \pm 10\%$ and 100pF when $V_{\text{DD}} = 3.0\text{V} \pm 10\%$.

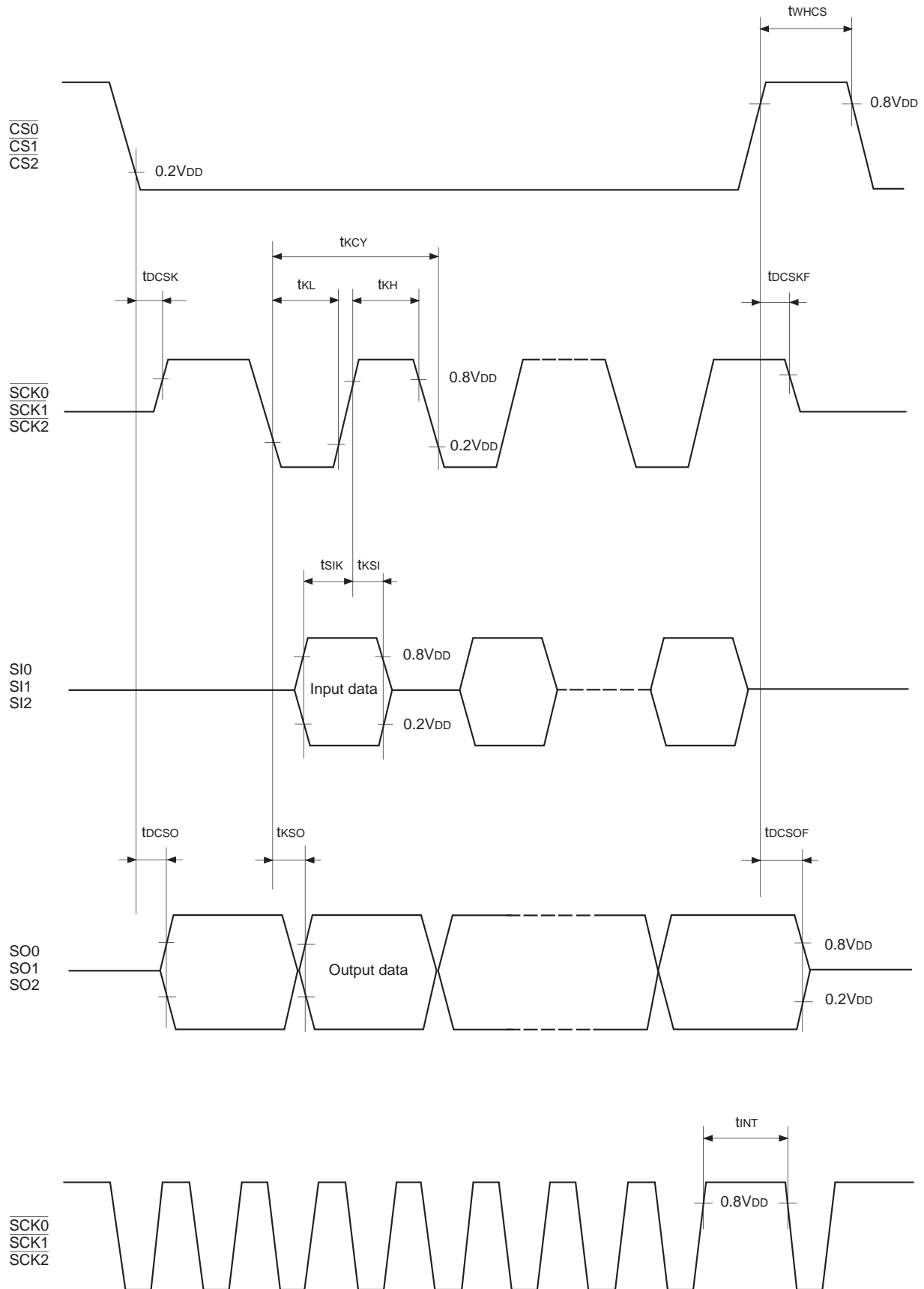


Fig. 4. Serial interface CH0, CH1, CH2 timing

(3) A/D converter characteristics

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = AV_{REF} = 3.0$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
Resolution						8	Bits	
Linearity error			$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$		± 15	LSB	
				$V_{DD} = AV_{DD} = 3.0\text{V}$		± 15		
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$	-10	10	50	mV
				$V_{DD} = AV_{DD} = 3.0\text{V}$	-10	5	35	
Full-scale transition voltage	V_{FT}^{*2}		$T_a = 25^\circ\text{C}$	$V_{DD} = AV_{DD} = 5.0\text{V}$	4935	4975	5015	mV
				$V_{DD} = AV_{DD} = 3.0\text{V}$	2955	2985	3015	
Conversion time	t_{CONV}			$200t_{sys}$			μs	
Sampling time	t_{SAMP}			$14t_{sys}$			μs	
Reference input voltage	V_{REF}	AV_{REF}		$0.9AV_{DD}$		AV_{DD}	V	
Analog input voltage	V_{IAN}	ANO to AN11		0		AV_{REF}	V	
AVREF current	I_{REF}	AV_{REF}	Operation mode	$V_{DD} = 5.5\text{V}$		0.65	1.2	mA
				$V_{DD} = 3.6\text{V}$		0.45	0.8	
	I_{REFS}	AV_{REF}	Sleep mode Stop mode	$V_{DD} = 5.5\text{V}$			10	μA
				$V_{DD} = 3.6\text{V}$			10	

*1 V_{ZT} : Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FEh to FFh and vice versa.

Note) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).

t_{sys} [ns] = 2000/ f_c (upper two bits = "00"), 4000/ f_c (upper two bits = "01"), 16000/ f_c (upper two bits = "11")

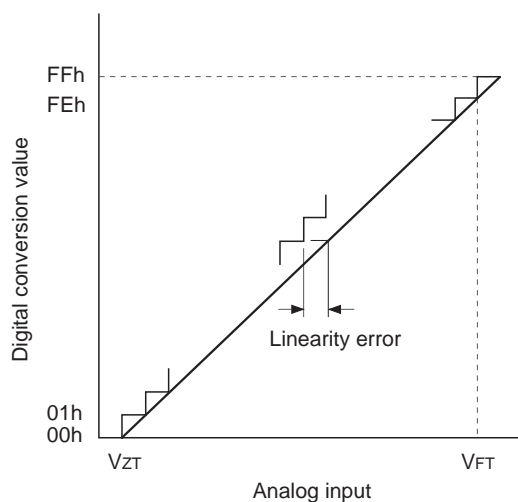


Fig. 5. Definition of A/D converter terms

(4) Interruption and reset input (Ta = -20 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t _{IH} , t _{IL}	$\overline{\text{NMI}}$ $\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ PD0 to PD7		1		μs
Reset input Low level width	t _{RSL}	$\overline{\text{RST}}$		6t _{sys} *		μs

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

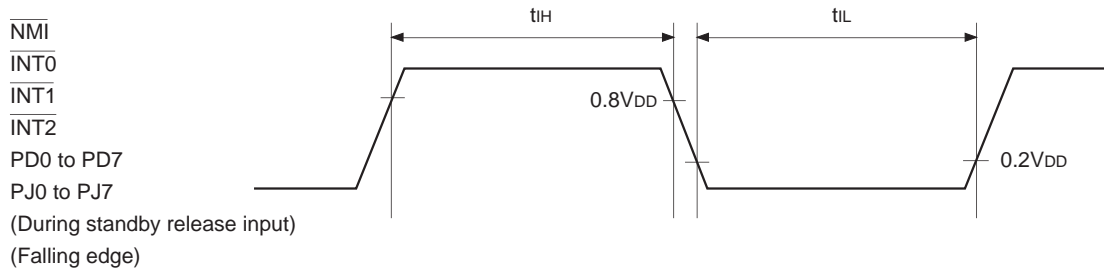


Fig. 6. Interruption input timing

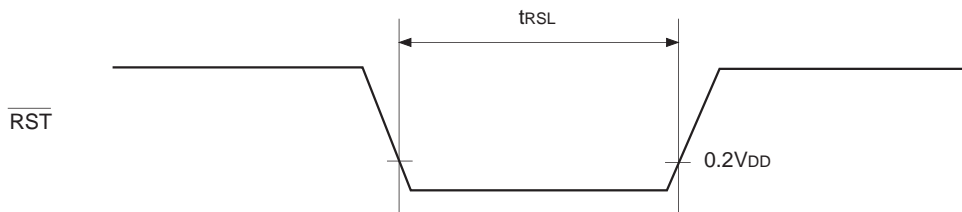


Fig. 7. $\overline{\text{RST}}$ input timing

(5) General-purpose prescaler

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK		$V_{DD} = 5.0V \pm 10\%$		12	MHz
				$V_{DD} = 3.0V \pm 10\%$		12	
External clock input pulse width	t_{WH}, t_{WL}	PCK		$V_{DD} = 5.0V \pm 10\%$	33		ns
				$V_{DD} = 3.0V \pm 10\%$	33		
External clock input rise time, fall time	t_R, t_F	PCK		$V_{DD} = 5.0V \pm 10\%$		200	ns
				$V_{DD} = 3.0V \pm 10\%$		200	
Prescaler output delay time (for PCK ↑)	t_{PLH}	PO	External clock input PCK $t_R = t_F = 6ns$	$V_{DD} = 5.0V \pm 10\%$	80	130	ns
				$V_{DD} = 3.0V \pm 10\%$	130	220	
	t_{PHL}			$V_{DD} = 5.0V \pm 10\%$	60	100	ns
				$V_{DD} = 3.0V \pm 10\%$	90	150	
Prescaler output rise time, fall time	t_{TLH}	PO	External clock input PCK $t_R = t_F = 6ns$	$V_{DD} = 5.0V \pm 10\%$	50	100	ns
				$V_{DD} = 3.0V \pm 10\%$	100	280	
	t_{THL}			$V_{DD} = 5.0V \pm 10\%$	20	40	ns
				$V_{DD} = 3.0V \pm 10\%$	40	80	

Note) PO pin load condition: 50pF

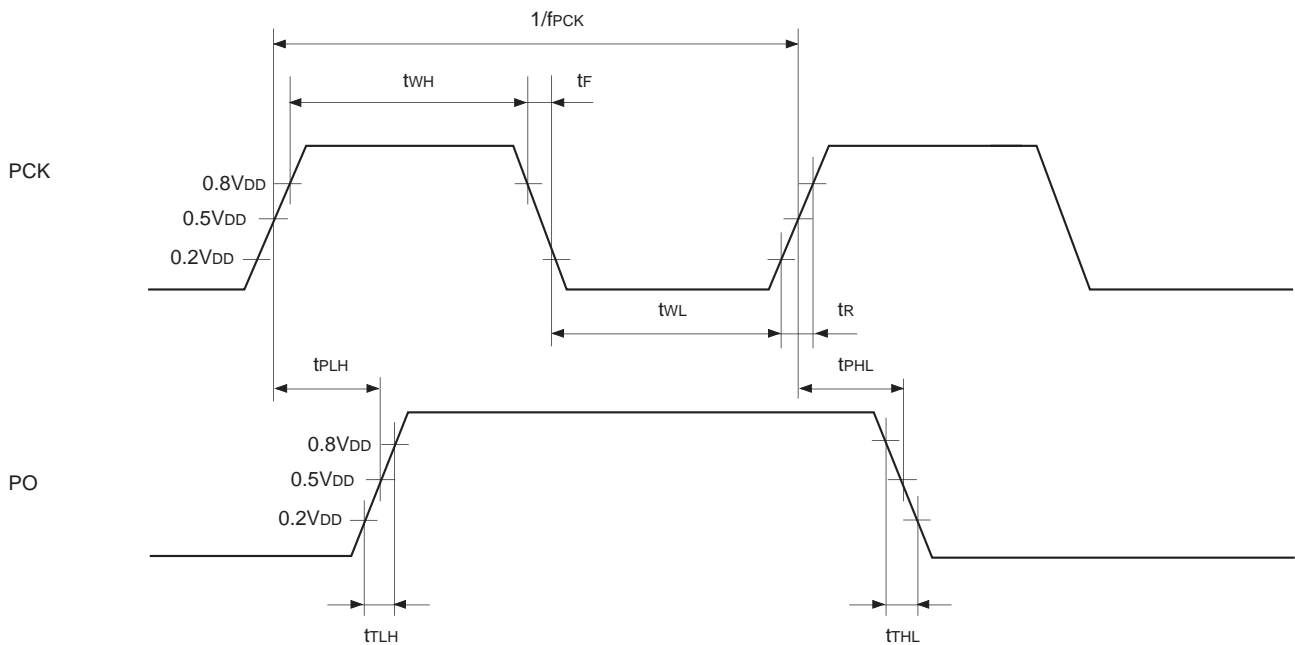


Fig. 8. General-purpose prescaler timing

(6) Other

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit	
CFG input High, Low level width	t _{CFH} , t _{CFL}	CFG	V _{DD} = 5.0V ± 10%	t _{sys} + 200			ns	
			V _{DD} = 3.0V ± 10%	t _{sys} + 200				
DFG input High, Low level width	t _{DFH} , t _{DFL}	DFG	V _{DD} = 5.0V ± 10%	1000/fc + 200			ns	
			V _{DD} = 3.0V ± 10%	1000/fc + 200				
DPG minimum pulse width	t _{DPW}	DPG	V _{DD} = 5.0V ± 10%	50			ns	
			V _{DD} = 3.0V ± 10%	50				
DPG minimum removal time	t _{DPR}	DPG	V _{DD} = 5.0V ± 10%	50			ns	
			V _{DD} = 3.0V ± 10%	50				
RFG input High, Low level width	t _{RFH} , t _{RFL}	RFG0 RFG1	V _{DD} = 5.0V ± 10%	t _{sys} + 200			ns	
			V _{DD} = 3.0V ± 10%	t _{sys} + 200				
EXI input High, Low level width	t _{EIH} , t _{EIL}	EXI0 EXI1	When t _{sys} = 2000/fc	V _{DD} = 5.0V ± 10%	t _{sys} + 200		ns	
				V _{DD} = 3.0V ± 10%	t _{sys} + 200			
PMI input High, Low level width	t _{PIH} , t _{PIL}	PMI	V _{DD} = 5.0V ± 10%	t _{sys} + 200			ns	
			V _{DD} = 3.0V ± 10%	t _{sys} + 200				
PMSK minimum pulse width	t _{PMW}	PMSK	V _{DD} = 5.0V ± 10%	t _{sys} + 200			ns	
			V _{DD} = 3.0V ± 10%	t _{sys} + 200				
PMSK minimum removal time	t _{PMR}	PMSK	V _{DD} = 5.0V ± 10%	t _{sys} + 200			ns	
			V _{DD} = 3.0V ± 10%	t _{sys} + 200				
XOUT output rise time, fall time	t _{TLH}	XOUT	When the load is 50pF	V _{DD} = 5.0V ± 10%		50	100	ns
				V _{DD} = 3.0V ± 10%		100	280	
	V _{DD} = 5.0V ± 10%				20	40		
	V _{DD} = 3.0V ± 10%				40	80		

Note) t_{sys} indicates the three values below according to the upper two bits (CPU clock selected) of the clock control register CLC (address: 0002FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

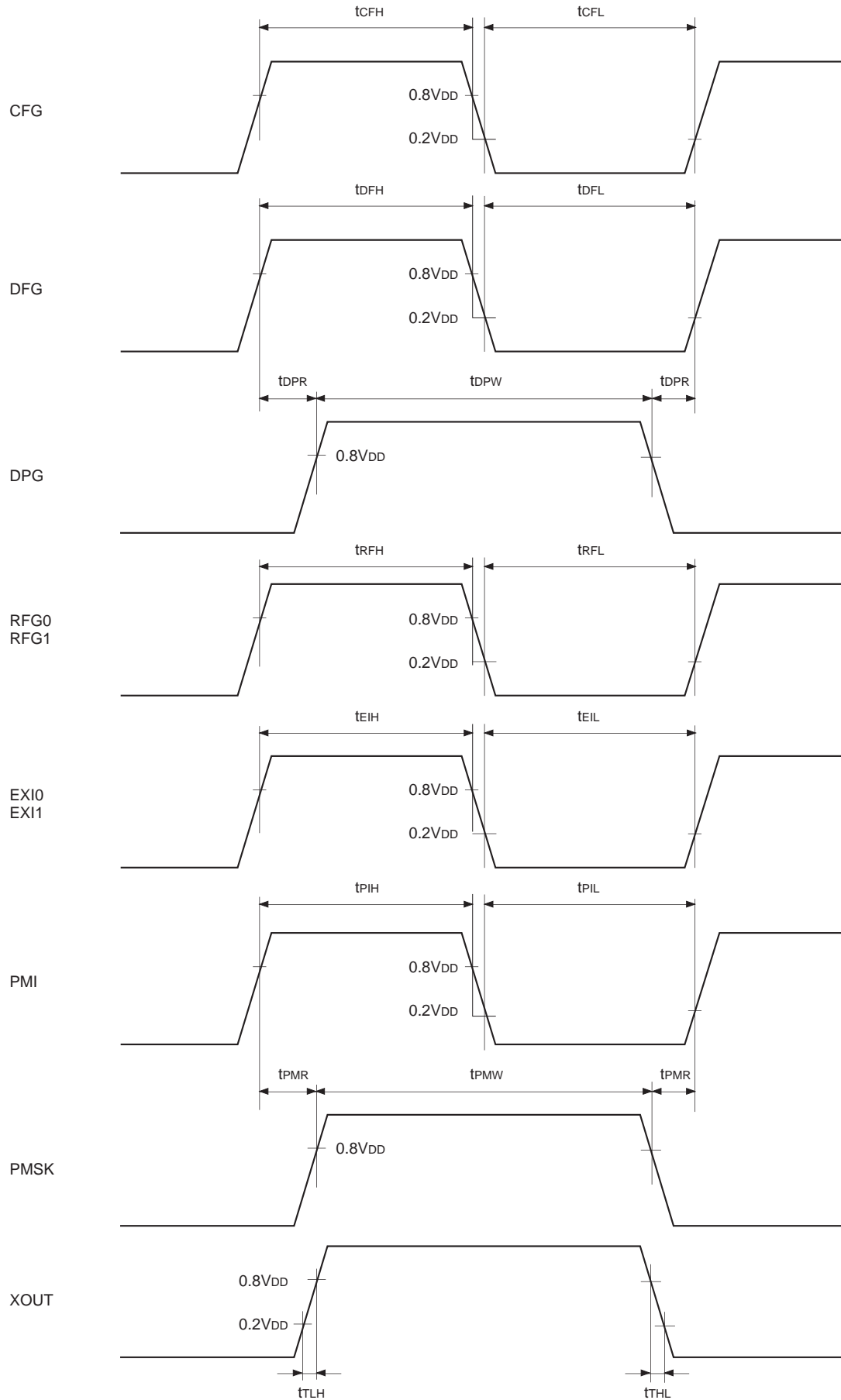


Fig. 9. Other timing

Appendix

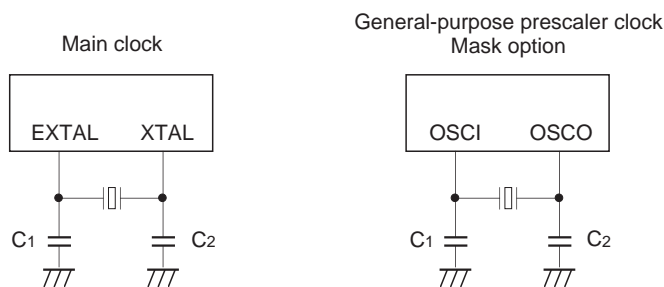


Fig. 10. Recommended oscillation circuit

Manufacturer	Model	fc (MHz)	Main clock		General-purpose prescaler clock	
			C1 (pF)	C2 (pF)	C1 (pF)	C2 (pF)
RIVER ELETEC CO., LTD.	HC-49/U03	12	10	10	4	4
		16			/	
		20			/	
KINSEKI LTD.	HC-49/U (-S)	12	10	10	4	4
		16			/	
		20			/	

Note 1) Use the general-purpose prescaler clock at 12MHz or less.

Note 2) Crystals and capacitors should be placed near the LSI and wiring should be as short as possible.

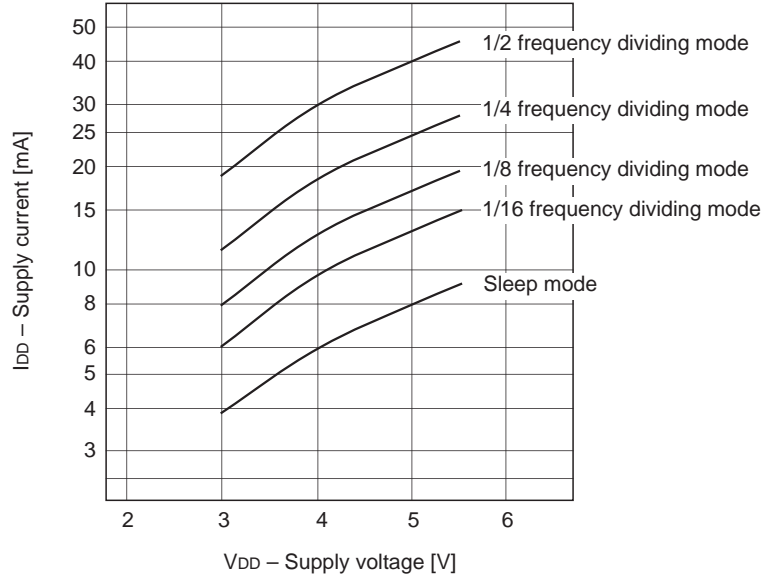
Mask option table

Item	Selection	
EXTAL system operating voltage*	2.7 to 5.5V	4.5 to 5.5V
Reset pin pull-up resistor	Non-existent	Existent
PH2 input circuit	CMOS Schmitt trigger	TTL Schmitt trigger
PH3 input circuit	CMOS Schmitt trigger	TTL Schmitt trigger
PI4/PI5 pin circuit	Oscillation circuit	Input pin

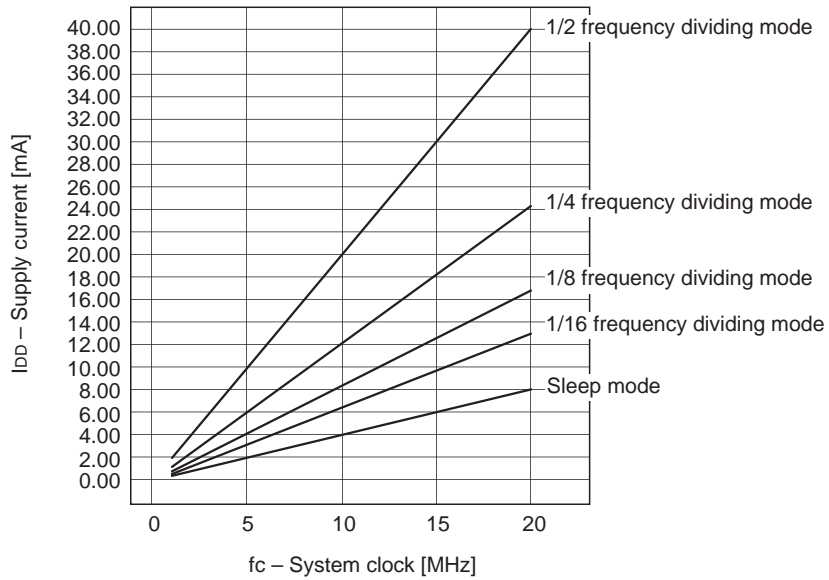
* Select 4.5V to 5.5V when this LSI is used with a supply voltage range of 4.5V to 5.5V.

Example of Representative Characteristics

I_{DD} vs. V_{DD}
 (f_c = 20MHz, T_a = 25°C, Typical)



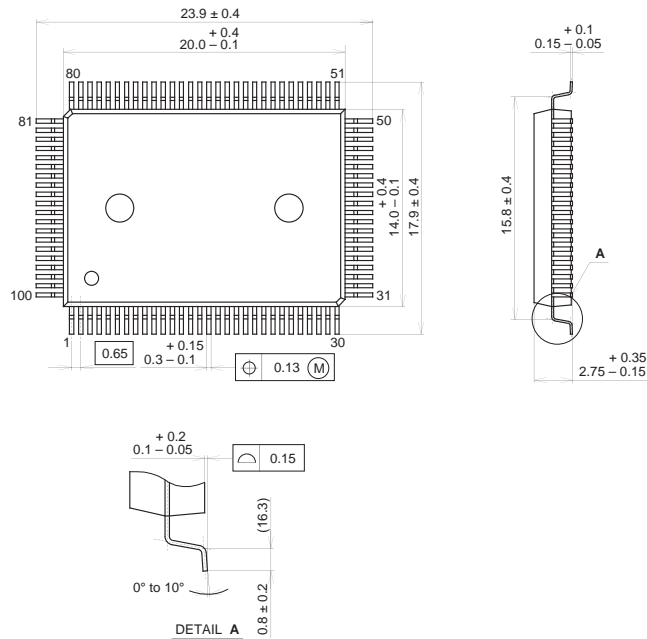
I_{DD} vs. f_c
 (V_{DD} = 5V, T_a = 25°C, Typical)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

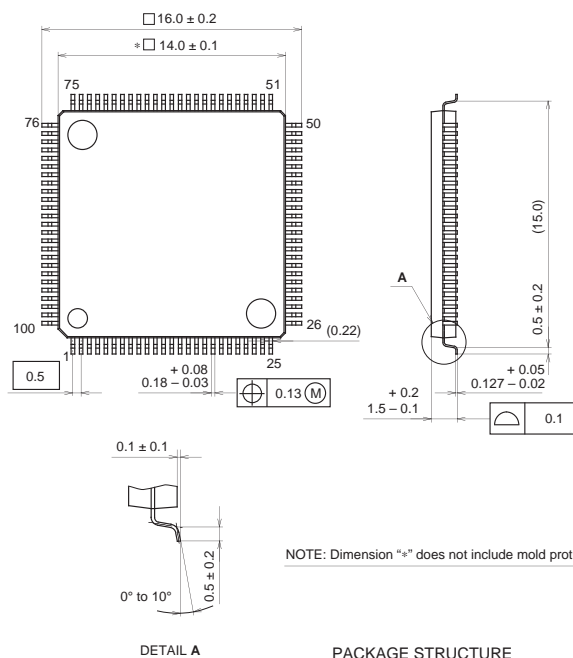


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

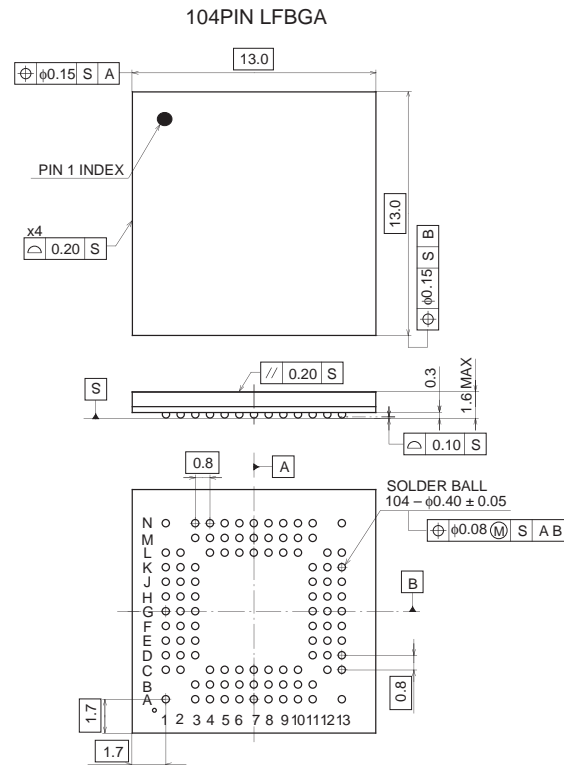
SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g

Package Outline

Unit: mm



PACKAGE STRUCTURE

SONY CODE	LFBGA-104P-01
EIAJ CODE	LFBGA104-P-1313
JEDEC CODE	

PACKAGE MATERIAL	ORGANIC SUBSTRATE
BOARD TREATMENT	COPPER-CLAP RAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE MASS	0.5g