BLF2425M7L250P; BLF2425M7LS250P

Power LDMOS transistor

Rev. 4 — 12 July 2013 Product data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M7L250P and BLF2425M7LS250P are designed for high-power CW applications and are assembled in high performance ceramic packages, available in eared and earless versions

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	28	250	15	51

1.2 Features and benefits

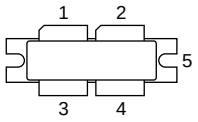
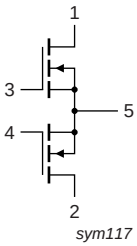
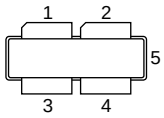
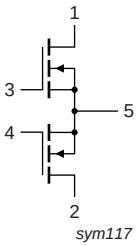
- High efficiency
- Easy power control
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM and industrial heating.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF2425M7L250P (SOT539A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF2425M7LS250P (SOT539B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M7L250P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF2425M7LS250P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 250 W	0.19	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 220 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	3	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	39	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	300	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 11 A	-	16	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.7 A	-	0.08	-	Ω

Table 7. RF characteristics

Test signal: CW at 2450 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 20 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 250 W	14	15	-	dB
RL_{in}	input return loss	P_L = 250 W	-	–18	–10	dB
η_D	drain efficiency	P_L = 250 W	46	51	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF2425M7L250P and BLF2425M7LS250P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 20 mA; P_L = 250 W (CW); f = 2450 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data half device. Typical values unless otherwise specified. I_{Dq} = 20 mA; V_{DS} = 28 V.
Z_S and Z_L defined in Figure 1.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
2400	2.3 – 6.3j	3.8 – 2.7j
2450	3.3 – 6.0j	2.5 – 2.9j
2500	4.1 – 6.0j	3.3 – 2.3j

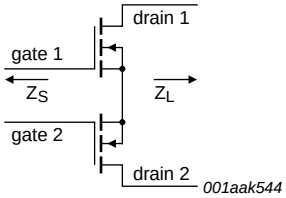
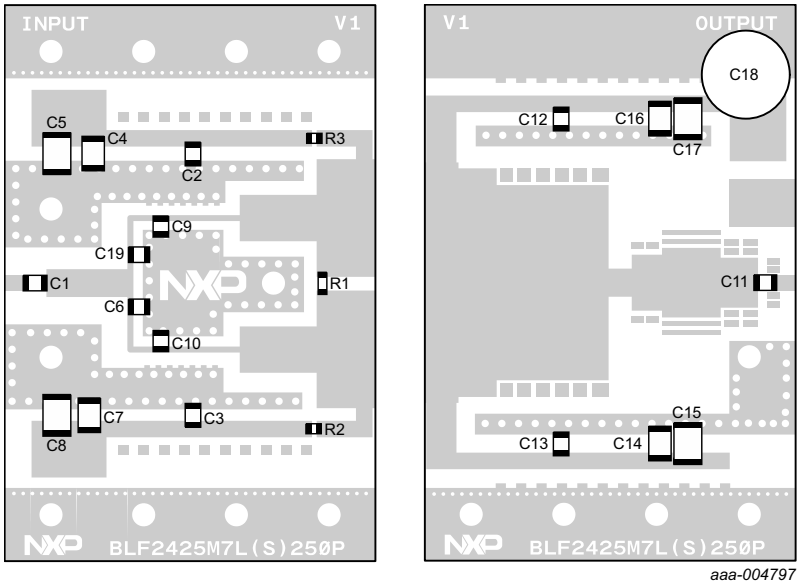


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.76 mm.

See Table 9 for list of components.

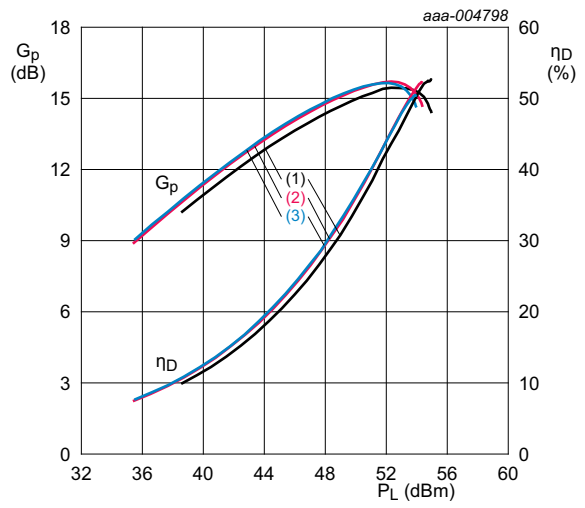
Fig 2. Component layout for test circuit

Table 9. List of components

For test circuit, see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C11, C12, C13	multilayer ceramic chip capacitor	36 pF	ATC800B
C4, C7, C14, C16	SMD capacitor	470 nF, 50 V	
C5, C8, C15, C17	SMD capacitor	10 μF, 50 V	
C6, C19	multilayer ceramic chip capacitor	1.4 pF	ATC100B
C9, C10	multilayer ceramic chip capacitor	1.8 pF	ATC100B
C18	electrolytic capacitor	470 μF, 63 V	
R1	resistor	9.1 Ω	SMD 0805
R2, R3	resistor	5.1 Ω	SMD 0805

7.4 Graphical data



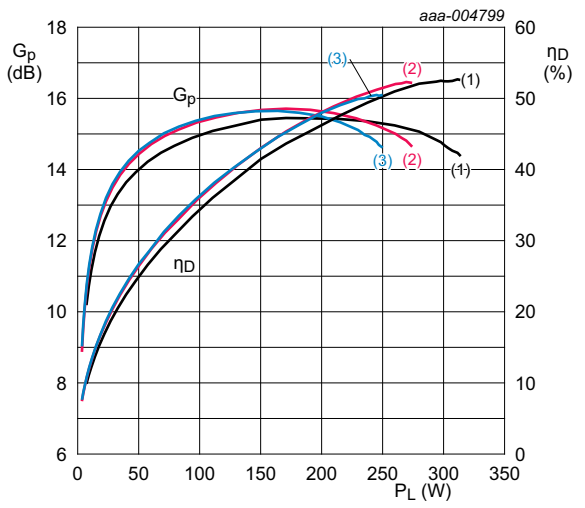
V_{DS} = 28 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

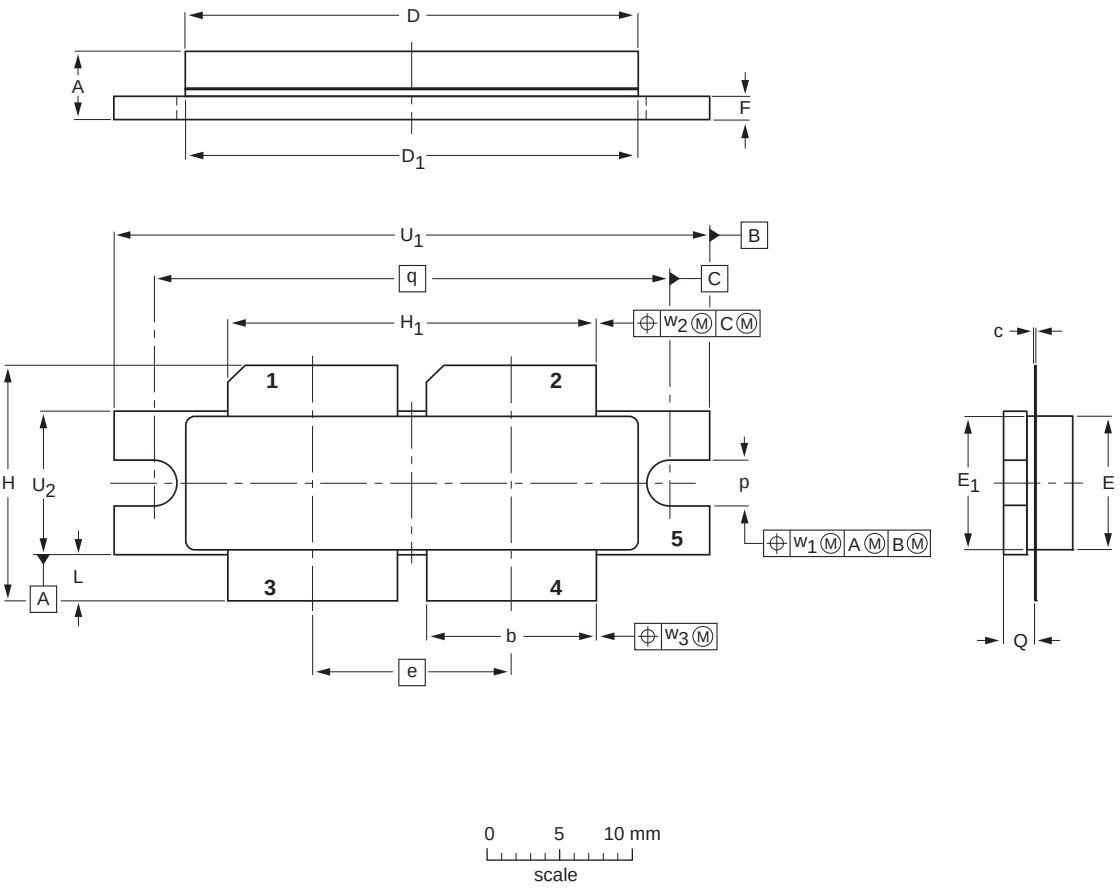
(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of load power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

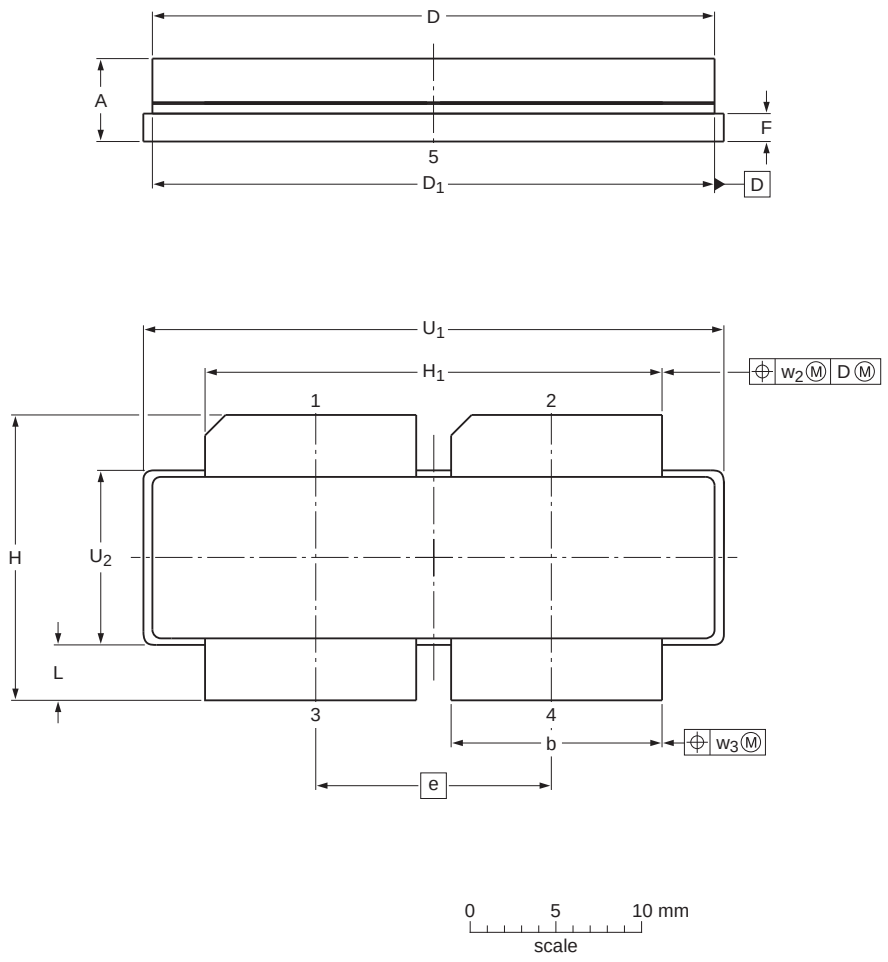
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 5. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 6. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M7L250P_2425M7LS250P v.4	20130712	Product data sheet	-	BLF2425M7L250P_2425M7LS250P v.3
Modifications:	• The package outline Figure 6 is updated.			
BLF2425M7L250P_2425M7LS250P v.3	20130226	Product data sheet	-	BLF2425M7L250P_2425M7LS250P v.2
Modifications:	• Section 1.1 on page 1: updated • Section 1.2 on page 1: updated • Table 4 on page 2: removed row T_{case} • Table 6 on page 3: changed typical value $R_{DS(on)}$ • Table 7 on page 3: updated • Figure 1 on page 4: replaced figure			
BLF2425M7L250P_2425M7LS250P v.2	20120906	Objective data sheet	-	BLF2425M7L250P_2425M7LS250P v.1
BLF2425M7L250P_2425M7LS250P v.1	20110718	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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