

# 12-Bit, Current Output, Complete High Speed D/A Converter

**AD565** 

#### 1.0 **SCOPE**

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at <a href="http://www.analog.com/aerospace">http://www.analog.com/aerospace</a> is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at <a href="https://www.analog.com/AD565">www.analog.com/AD565</a>

**2.0 Part Number**. The complete part number(s) of this specification follow:

Part Number Description

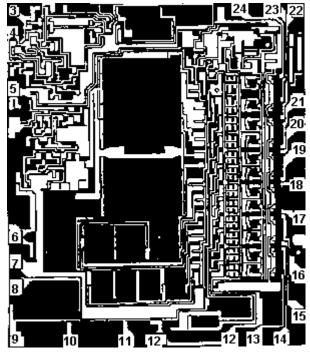
AD565-000C 12-Bit, Current Output, Complete High Speed D/A Converter

#### 3.0 <u>Die Information</u>

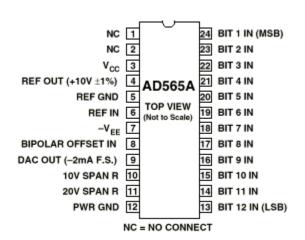
#### 3.1 <u>Die Dimensions</u>

Die Size	Die Thickness mil	Bond Pad Metalization
119 mil x 146 mil	19 mil ± 2 mil	AI/Cu

#### 3.2 Die Picture



ASD0012329 Rev. G
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## **AD565**

#### 3.3 Absolute Maximum Ratings. 1/

V <sub>CC</sub> to power ground	0 to +18V dc
V <sub>EE</sub> to power ground	0 to -18V dc
Voltage on DAC output (pin 9)	3V dc to +12V dc
Digital inputs (pins 13 to 24) to power ground	1.0V dc to +7.0V dc
Ref in to ref ground	±12V dc
Bipolar offset to reference ground	±12V dc
10V span R to reference ground	±12V dc
20V span R to reference ground	±24V dc
Ref out	Indefinite short to power ground
	momentary short to V <sub>CC</sub>
Power dissipation	1000 mW
Storage temperature range	65°C to +150°C
Operating temperature range	55°C to +125°C
Junction temperature (T <sub>J</sub> )	+150°C

<sup>1/</sup> Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

#### 3.4 Recommended operating conditions.

Positive supply voltage (V <sub>CC</sub> )	+15V
Negative supply voltage (V <sub>EE</sub> )	15V
Operating ambient temperature range	55°C to +125°C

### 4.0 <u>Die Qualification</u>

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.

- (a) Qual Sample Package Sidebrazed DIP
- (b) Qual Sample Size and Qual Acceptance Criteria 10/0
- (c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

#### 5.0 **Dice Electrical Characteristics**

		Table I				
Parameter	Symbol	Conditions Limit Note 1 Min		Limit Max	Units	
Relative Accuracy	RA	All bits w/ positive errors on All bits w/ negative errors on		±0.5	LSB	
Differential Nonlinearity	DNL	Major transition		±0.75	LSB	
Gain Error	AE	$R_{REF} = 50 \cdot fixed$		±0.25	% of FS	
Offset Error	Vos			±0.05	% of FS	
Bipolar Zero Error Note 2	B <sub>PZE</sub>	R <sub>BO</sub> = 50• fixed		±0.15	% of FS	
Reference Output Voltage	V <sub>REF</sub>	Note 3	9.90	10.10	V	
Output Current	Іоит	Unipolar (all bits on)	-1.6	-2.4	mA	
Output Current	1001	Bipolar (all bits on)	-0.8	-1.2	IIIA	
Power Supply Rejection Ratio	PSRR	$V_S = +11.4V \text{ to } +16.5V \text{ dc}$		±10.0	PPM of FRS/%	
rower supply nejection natio	Pann	$V_S = -11.4V \text{ to } -16.5V \text{ dc}$		±25.0	PPINI OI FN3/90	
Power Supply Current	Icc			+5.0	mA	
Note 4, 5	I <sub>EE</sub>			-18.0	IIIA	
Power Dissipation	PD			345.0	mW	
Digital Input High Voltage	ViH		2.0	5.5	V	
Digital Input Low Voltage	VIL			0.8	V	
Digital Input High Current	I <sub>IH</sub>	V <sub>IH</sub> = 5.5V		300.0	μΑ	
Digital Input Low Current	I <sub>IL</sub>	V <sub>IL</sub> = 0V		100.0	μΑ	

#### Table I Notes:

- 1.  $V_{CC} = +15V$ ,  $V_{EE} = -15V$ ,  $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$ ,  $T_A = 25^{\circ}C$ .
- MSB on, all other bits off.
- 3. The reference output is loaded with 0.5mA reference input current, 1.0mA bipolar offset current, and 1.5mA additional current.
- Guaranteed for +11.4 ≤ V<sub>CC</sub> ≤ +16.5V.
   Guaranteed for -11.4 ≤ V<sub>EE</sub> ≤ -16.5V.

#### **Electrical Characteristics for Qual Samples** 5.1

Table II							
Parameter	Symbol	Conditions Note 1	Sub- groups	Limit Min	Limit Max	Units	
Relative Accuracy	RA	RA All bits w/ positive errors on All bits w/ negative errors on			±0.5	LSB	
			2, 3		±0.75		
Differential Nonlinearity	DNL	Major transition	1		±0.75	LSB	
,		<u>,                                      </u>	2, 3		±1.0		
Gain Error	AE	R <sub>REF</sub> = 50• fixed	1		±0.25	% of FS	
Gain Error Temperature Coefficient	TCA <sub>E</sub>		2, 3		±30.0	ppm of FS/°C	
Offset Error	Vos		1		±0.05	% of FS	
Offset Error Temperature Coefficient	TCVos		2, 3		±2.0	ppm of FS/°C	
Bipolar Zero Error Note 2	B <sub>PZE</sub>	R <sub>BO</sub> = 50• fixed	1		±0.15	% of FS	
Bipolar Zero Error Temperature Coefficient Note 2	TCB <sub>PZE</sub>		2, 3		±10.0	ppm of FS/°C	
Reference Output Voltage Note 3	$V_{REF}$		1, 2, 3	9.90	10.10	V	
Reference Output Current Note 4	I <sub>REF</sub>		1	1.5		mA	
Outrout Company	,	Unipolar (all bits on)		-1.6	-2.4	A	
Output Current	<b>І</b> оит	Bipolar (all bits on)	1 1	-0.8	-1.2	mA	
Power Supply Rejection Ratio	PSRR	$V_S = +11.4V \text{ to } +16.5V \text{ dc}$	1		±10.0	PPM of FRS/%	
rower supply nejection natio	FJIII	$V_S = -11.4V \text{ to } -16.5V \text{ dc}$			±25.0	- FFWIOITINS/70	
Power Supply Current	lcc .		1		+5.0	mA .	
Note 4, 5	I <sub>EE</sub>				-18.0		
Power Dissipation	P <sub>D</sub>		1		345.0	mW	
Digital Input High Voltage	V <sub>IH</sub>		1	2.0	5.5	V	
Digital Input Low Voltage	V <sub>IL</sub>		1		0.8	V	
Digital Input High Current	I <sub>IH</sub>	V <sub>H</sub> = 5.5V	1		300.0	μΑ	
Digital Input Low Current	IιL	$V_{IL} = 0V$	1		100.0	μΑ	

Table II Notes:

V<sub>CC</sub> = +15V, V<sub>EE</sub> = -15V, V<sub>IH</sub> = 2.0V, V<sub>IL</sub> = 0.8V.
 MSB on, all other bits off.
 In subgroup 1, the reference output is loaded with 0.5mA reference input current, 1.0mA bipolar offset current, and 1.5mA additional current. In subgroup 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

Guaranteed for +11.4  $\leq$  V<sub>CC</sub>  $\leq$  +16.5V.

Guaranteed for -11.4  $\leq$  V<sub>EE</sub>  $\leq$  -16.5V.

#### 6.0 <u>Delta Parameter Table</u>

Table III								
Downstan	6	Sub-	Post Burn In Limit		Post Life Test Limit		Life Test	11
Parameter	Symbol	groups	Min	Max	Min	Max	Delta	Units
Gain Error	AE	1		±0.25		±0.30	±0.05	% of FS
Bipolar Zero Error	B <sub>PZE</sub>	1		±0.15		±0.225	±0.075	% of FS

## 7.0 <u>Life Test/Burn-In Information</u>

- 7.1 HTRB is not applicable for this drawing.
- 7.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.
- 7.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
Α	Initiate	June 26, 2001
В	Update web address. Fix footer	Jan. 25, 2002
С	Update web address.	Aug. 5, 2003
D	Update header/footer & add to 1.0 Scope description.	Feb. 26, 2008
E	Add Absolute Maximum Ratings table in section 3.3	April 2, 2008
F	Updated Section 4.0c note to indicated pre-screen temp testing being performed.	June 6, 2009
G	Updated Fonts and Sizes to ADI standard, enlarged die picture pad numbering	22-Sept-2011