PRELIMINARY

DIGITAL COLOR SPACE CONVERTER

FEATURES

- RGB to YCbCr and YCbCr to RGB conversions
- CyMaYe to YCbCr and YCbCr to CyMaYe conversions
- Bidirectional data buses for convenient interfacing
- Pixel rates up to 30 megapixels per second
- Supports 4:2:2 decimation and interpolation modes, with optional filtering
- Supports 4:1:1 decimation and interpolation with filtering
- CCIR601 and full range data scaling options
- Bidirectional shift registers for sync pulse delay matching
- Compatible with Zoran's ZR36050 JPEG Image Compression Processor and ZR36015 Raster to Block Converter
- 100-Pin PQFP package
- Low power CMOS, 5V

APPLICATIONS

- Image processing
- Image capture and display
- Image compression

GENERAL DESCRIPTION

The ZR36011 Digital Color Space Convertor performs forward or inverse conversions between RGB and YCbCr color spaces. It is intended for use as a building block in systems that require this function. The direction of the conversion (RGB to YCbCr or YCbCr to RGB), and all other operating mode options, are determined by the states of control inputs. The 24-bit RGB and YCbCr data buses are bidirectional, making for straightforward interfacing when the direction of signal flow is reversible, as in a video compression and expansion module. Conversion between CyMaYe (Cyan, Magenta, Yellow) and YCbCr color spaces is also supported. An additional conversion stage, between RGB and CyMaYe color spaces, is inserted in this case, thus redefining the R, G, B pins as Cy, Ma, Ye.

The color space conversion coefficients are fixed. One of two sets of coefficients can be selected: one suitable for component signal ranges conforming to CCIR Recommendation 601, the other for components occupying the full 8 bit numeric range.

Decimation and interpolation of the color difference signals is supported. The available modes are 4:4:4 (undecimated), 4:2:2 and 4:1:1. Filtering is optional in the 4:2:2 mode, and is always performed in the 4:1:1 mode. Other operating modes allow simple two-to-one compression to be performed by an additional decimation of the Y, Cb and Cr data, as well as the corresponding decompression by interpolation.

A two-bit bidirectional shift register, with the same number of stages (eight) as the computation pipeline, is provided. This can be used as a delay line for synchronization signals, to keep them synchronized with the data.

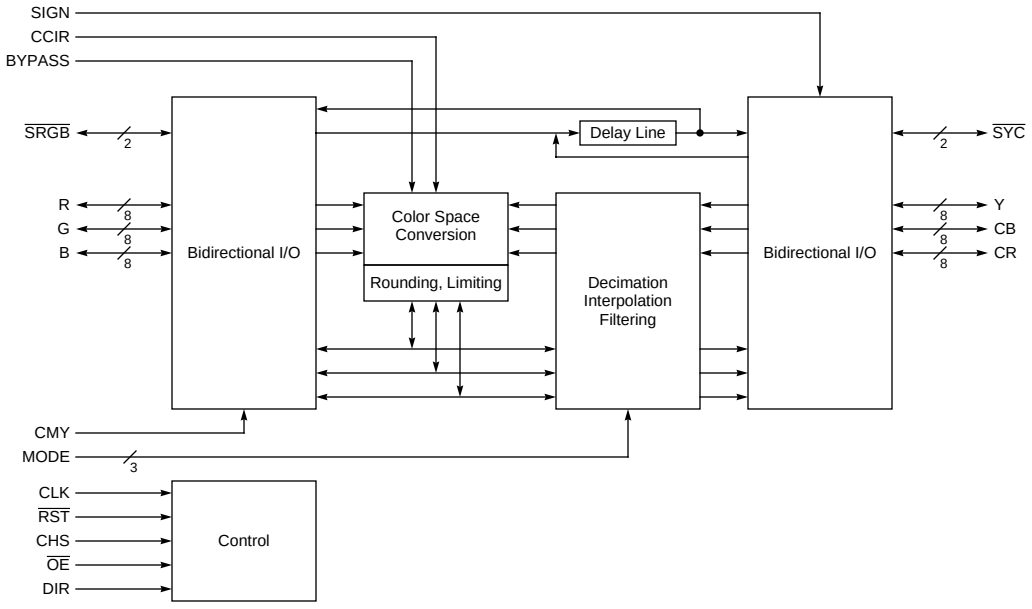


Figure 1. ZR36011 Block Diagram

Table 1. Signal Description

Name	Type	Description
V_{CC}	Power	+5 volt power. All V_{CC} pins must be connected to +5 volts.
V_{SS}	Power	Power supply ground. All V_{SS} pins must be connected to ground.
CLK	Input	System clock input. Input data and sync signals are latched on the rising edge of CLK, and output data and sync signals change state following the rising edge of CLK.
RST	Input	Reset, active low. Must be kept low for at least two clock cycles to reset the device. When active, all stages of the sync delay lines are initialized to the high state, and the delay line output (SRGB if DIR is high, or SYC if DIR is low) is high.
R(7-0)	I/O	Red component data if CMY is low, or Cyan if CMY is high. 8 bits unsigned. R is an input if DIR is low, and an output if DIR is high.
G(7-0)	I/O	Green component data if CMY is low, or Magenta if CMY is high. 8 bits unsigned. G is an input if DIR is low, and an output if DIR is high.
B(7-0)	I/O	Blue component data if CMY is low, or Yellow if CMY is high. 8 bits unsigned. B is an input if DIR is low, and an output if DIR is high.
$\overline{\text{SRGB(1-0)}}$ $\overline{\text{SYC(1-0)}}$	I/O	Sync delay line inputs and outputs. If DIR is low, SRGB is the input and SYC is the output, and vice versa if DIR is high. Input level changes appear at the output with a delay of 8 clock cycles. Since the delay line output is initialized to high by $\overline{\text{RST}}$, these signals are considered active low.
Y(7-0)	I/O	Luminance component data. 8 bits unsigned. Y is an output if DIR is low, and input if DIR is high.
CB(7-0)	I/O	Blue color difference (Cb) component data. 8 bits unsigned if SIGN is low, or 8 bits two's complement if SIGN is high. CB is an output if DIR is low, and input if DIR is high. In 4:2:2 and 4:1:1 modes, CB is unused (if outputs, all CB pins are high).
CR(7-0)	I/O	Red color difference (Cr) component data. 8 bits unsigned if SIGN is low, or 8 bits two's complement if SIGN is high. CR is an output if DIR is low, and input if DIR is high. In 4:2:2 and 4:1:1 modes, Cb and Cr data are multiplexed on CR.
DIR	Input	Direction control. If DIR is low, RGB (or CyMaYe) to YCbCr conversion is performed. If DIR is high, YCbCr to RGB (or CyMaYe) conversion is performed.
CMY	Input	CyMaYe color space control. If CMY is low, conversion between RGB and YCbCr color spaces is performed. If CMY is high, the R, G and B inputs or outputs are complemented, with the result that conversion between CyMaYe and YCbCr color spaces is performed.
CCIR	Input	Signal level control. If CCIR is low, input and output data may occupy the full 8 bit signal level range. If CCIR is high, input and output data signal levels conform to CCIR Recommendation 601-2.
CHS	Input	Chrominance multiplex synchronization signal. The rising edge of this signal is used to synchronize an internal toggle that controls the multiplexing of the Cb and Cr component data on the CB pins, in the operating modes with decimated chrominance. In operating modes with decimated luminance, it determines the temporal alignment of the decimated data.
SIGN	Input	Chrominance numerical representation control. The Cb and Cr data is unsigned if SIGN is low, and two's complement if SIGN is high.
$\overline{\text{OE}}$	Input	Output enable. When low, all outputs are enabled. When high, all outputs are disabled (floating). $\overline{\text{OE}}$ also disables the internal clock of the device when it is high, thus freezing all internal processing.

Table 1. Signal Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>MODE(2-0)</td><td>Input</td><td>Component decimation mode control. The decimation and interpolation modes are selected using MODE as shown follows:

Decimation Mode Selection (0=low, 1=high)
<table>
<tr><th>MODE2</th><th>MODE1</th><th>MODE0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>4:4:4, no decimation or interpolation</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4:2:2 chrominance decimation or interpolation without filtering</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4:2:2 chrominance decimation or interpolation with filtering</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4:1:1 chrominance decimation or interpolation</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Not used</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4:4:4, with 2 to 1 decimation or interpolation of all three YCbCr components</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4:2:2, with 2 to 1 additional decimation or interpolation of all three YCbCr components</td></tr>
</table></td></tr>
<tr><td>BYPASS</td><td>Input</td><td>Conversion bypass control. If BYPASS is high, the color space conversion computation is bypassed, but all decimation mode selections and control inputs are still operational. The data pipeline delay of 8 clock cycles is not affected by the activation of BYPASS.</td></tr>
</table>

FUNCTIONAL OVERVIEW

COLOR SPACE CONVERSION

RGB <-> YCbCr

The Color Space Conversion block (see Figure 1) performs conversion between RGB and YCbCr color spaces, with built in conversion coefficients. One of two data scaling and limiting modes can be selected by means of the CCIR control input, one (with CCIR low) intended for data occupying the full 8 bit signal level range, the other (with CCIR high) intended for data occupying the range of values specified by CCIR Recommendation 601-2. The conversions are performed as follows:

Forward direction, DIR = low:

With CCIR low (8 bit full range data):

Y = 0.299R + 0.587G + 0.114B
Cr = 0.713(R-Y)
Cb = 0.564(B-Y)

With CCIR high (data conforming to CCIR):

Y = 0.299R + 0.587G + 0.114B
Cr = 0.729(R-Y)
Cb = 0.577(B-Y)

Inverse direction, DIR = high:

With CCIR low (8 bit full range data):

R = Y + 1.402Cr
G = Y - 0.714Cr - 0.344Cb
B = Y + 1.772Cb

With CCIR high (data conforming to CCIR):

R = Y + 1.37Cr
G = Y - 0.698Cr - 0.336Cb
B = Y + 1.73Cb

Internally, the color space conversion coefficients are represented with a precision of 12 bits.

RGB <-> CyMaYe

When the CMY control input is high, the 8 bit R, G and B data are logically complemented in the I/O block, thus performing an additional conversion between the internal R, G, B and external Cy, Ma, Ye. This is equivalent to the following conversion formula:

Cy = 255 - R
Ma = 255 - G
Ye = 255 - B

NUMERICAL REPRESENTATION

The results of the color space conversion are rounded to produce 8 bit results, and limited to prevent wrap-around. When CCIR is high, R, G, B, and Y occupy 220 levels, and CR and CB occupy 225 levels. Input data outside the allowed range of levels is internally limited, and output data is limited to the allowed range. When CCIR is low, inputs can occupy the full 8 bit range, and outputs are limited to this range.

CR and CB can have either two's complement or offset binary representations, as selected by the SIGN control input. R, G, B and Y always have unsigned magnitude representation.

Tables 2 and 3 show, for CCIR low and CCIR high, respectively, the equivalent decimal number represented by each hexadecimal value of the data inputs and outputs.

Table 2. Numerical Representation, CCIR = low

Hexadecimal Value	Decimal Equivalent		
	R, G, B, Y (Unsigned)	CR, CB	
		Offset Binary (SIGN = low)	Two's Compliment (SIGN = high)
FF	255	127	-1
FE	254	126	-2
...	...	...	...
81	129	1	-127
80	128	0	-128
7F	127	-1	127
...	...	...	...
01	1	-127	1
00	0	-128	0

Table 3. Numerical Representation, CCIR = high

Hexadecimal Value	Decimal Equivalent		
	R, G, B, Y (Unsigned)	CR, CB	
		Offset Binary (SIGN = low)	Two's Compliment (SIGN = high
FF	235	112	-1
FE	235	112	-2
...	...	....	...
F1	235	112	-15
F0	235	112	-16

Table 3. Numerical Representation, CCIR = high (Continued)

Hexadecimal Value	Decimal Equivalent		
	R, G, B, Y (Unsigned)	CR, CB	
		Offset Binary (SIGN = low)	Two's Compliment (SIGN = high
EF	235	111	-17
EE	235	110	-18
ED	235	109	-19
EC	235	108	-20
EB	235	107	-21
EA	234	106	-22
...	...	...	...
91	145	17	-111
90	144	16	-112
8F	143	15	-112
...	...	...	...
81	129	1	-112
80	128	0	-112
7F	127	-1	112
...	...	...	...
71	113	-15	112
70	112	-16	112
69	111	-17	111
...	...	...	...
11	17	-111	17
10	16	-112	16
0F	16	-112	15
...	...	...	
01	16	-112	1
00	16	-112	0

CONVERSION BYPASS

When the BYPASS control input is high, the color space conversion block (Figure 1), and consequently the RGB <-> YCbCr color space conversion computation, is bypassed. All the other functional blocks, and all control inputs, continue to operate normally. Thus, when BYPASS is high, the device can be utilized as a data format convertor, for example:

- With CMY high, and MODE(2-0) = 000, as a RGB to CyMaYe convertor
- With MODE(2-0) = 010, to perform conversions between 4:4:4 and 4:2:2 formats
- With MODE(2-0) = 110, to perform 2:1 decimation and interpolation of all three components

INPUT TO OUTPUT LATENCY

The output data has a latency or pipeline delay of eight clock cycles. This latency is constant, in all modes of operation, regardless of the direction of conversion, decimation or interpolation setting, or whether the color space conversion is bypassed or not.

DELAY LINE

The delay line consists of an eight stage shift register with a two bit wide data path. Its delay is equal to the latency of the data outputs. Thus, it is useful as a matching delay line for horizontal and vertical video synchronization signals, to keep them in synchronization with the data flowing through the device.

The $\overline{RST}$ input resets all stages of the delay line to the high state, and consequently the output ($\overline{SYC}$ or $\overline{SRGB}$ depending on the state of DIR) is also high when reset is active. The delay line is therefore suitable for active low synchronization signals. The input at $\overline{SYC}$ or $\overline{SRGB}$ is effectively ignored when RST is active, and is clocked into the delay line starting from the second rising edge of CLK following the deactivation of $\overline{RST}$, as shown in Figure 2.

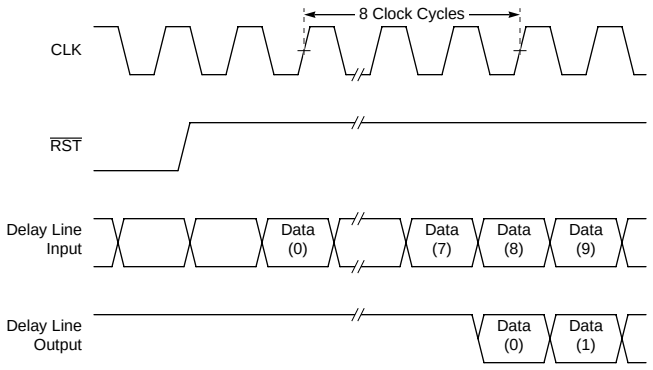


Figure 2. Delay Line Reset Timing

OUTPUT ENABLE AND PIPELINE FREEZE

The $\overline{OE}$ input simultaneously controls the enabling of all output pins (color components and delay line), and the freezing of the computational pipeline. When $\overline{OE}$ is low, the output pins are enabled, and data is clocked through the pipeline. When $\overline{OE}$ goes high, the outputs go into a high impedance state, and the clock is disabled internally starting at the second rising edge of CLK following the rising edge of $\overline{OE}$, thus freezing all operations in their current state, including the color space conversion computation, decimation and interpolation, and the delay line. Input data is ignored while the clock is disabled. The clock is enabled

again starting at the second rising edge of CLK following the falling edge of $\overline{OE}$. Note that since OE enables and disables the internal clock, it is a synchronous input and must have sufficient setup and hold time. See Figure 3 for an example of the operation of $\overline{OE}$.

DECIMATION AND INTERPOLATION MODES

The three MODE control pins select the operating mode of the decimation and interpolation function block, as shown in Table 1. Decimation is performed in forward color space conversion (DIR = low), and interpolation is performed in inverse color space conversion (DIR = high).

Whenever decimation or interpolation of the luminance and/or chrominance data is performed (all modes with the exception of MODE = 000), each data sample on the Y, CB, CR pins occupies more than one clock cycle, or the chrominance data is multiplexed on the CR pins, or both (multiplexed chrominance samples that occupy more than one clock cycle each). The CHS input signal must be used, as shown in the timing diagrams for each of the modes, to synchronize the operation of the device to the data on the Y, CR, CB pins. The second rising edge of CLK following the rising edge of CHS always samples the first input data point. CHS is used to initialize the state of the internal mechanism that subsequently maintains the synchronization.

MODE = 000

In this mode no decimation or interpolation is performed. YCbCr pixels are 24 bits wide; the CR pins carry the Cr data and the CB pins carry the Cb data. A timing diagram for forward conversion is shown in Figure 3; inverse conversion in this mode has identical timing, except that the functions of the R, G, B pins are exchanged with those of the Y, CR, CB pins. The operation of the $\overline{OE}$ signal is also depicted in Figure 3. CHS is not used in this mode of operation.

MODE = 001

In this mode, YCbCr data is in 4:2:2 format. The CB pins are not used; Cb and Cr data are multiplexed on the CR pins. The Cb and Cr samples are co-sited with the Y sample that is simultaneous with the Cb sample. Cb and Cr are decimated in forward conversion by dropping the unused samples, and interpolated in inverse conversion by replication. No filtering is performed in either direction. Figures 4 and 5, respectively, illustrate how the decimation and interpolation are performed.

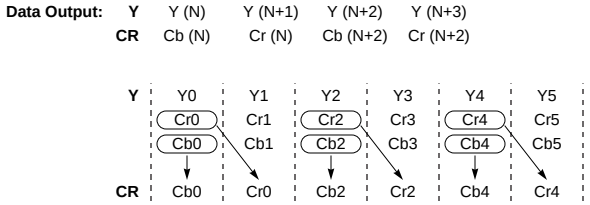


Figure 4. Illustration of Decimation Method, MODE = 001

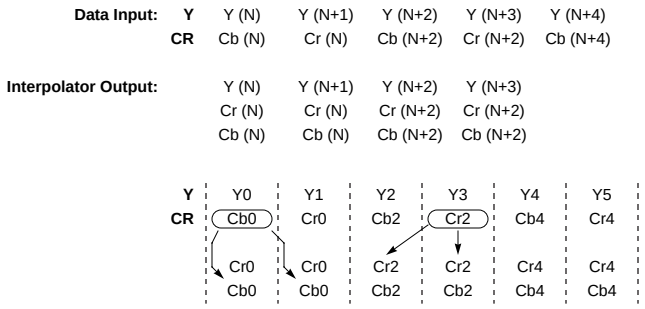


Figure 5. Illustration of Interpolation Method, MODE = 001

CHS determines the validity of input data and synchronizes the multiplexing of Cr and Cb on the CR pins. As shown in Figure 6 for forward conversion, and Figure 7 for inverse conversion, the second rising edge of CLK following the rising edge of CHS latches the first valid input data sample and determines the multiplex order.

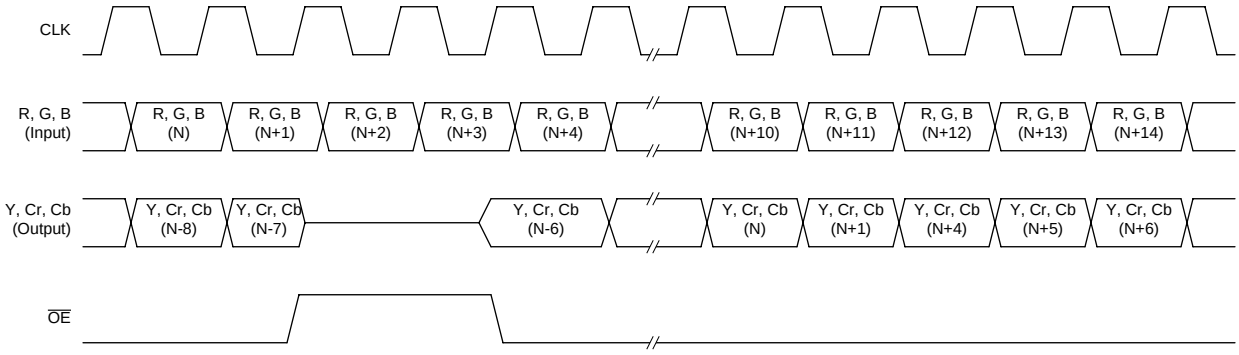


Figure 3. RGB to YCbCr Conversion, MODE = 000, also Showing $\overline{OE}$ Timing

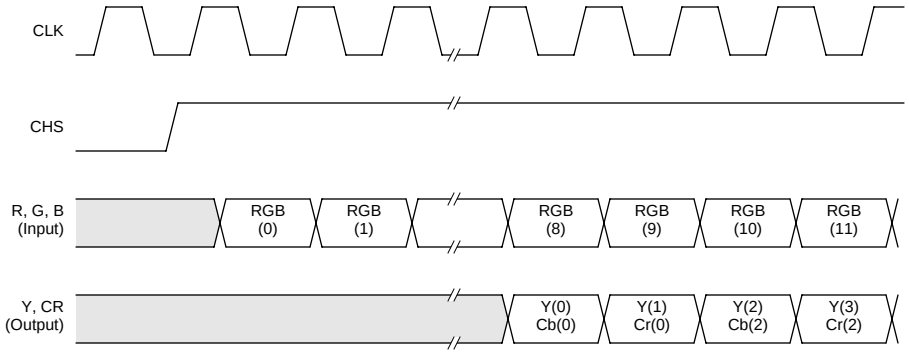


Figure 6. RGB to YCbCr Timing, MODE = 001

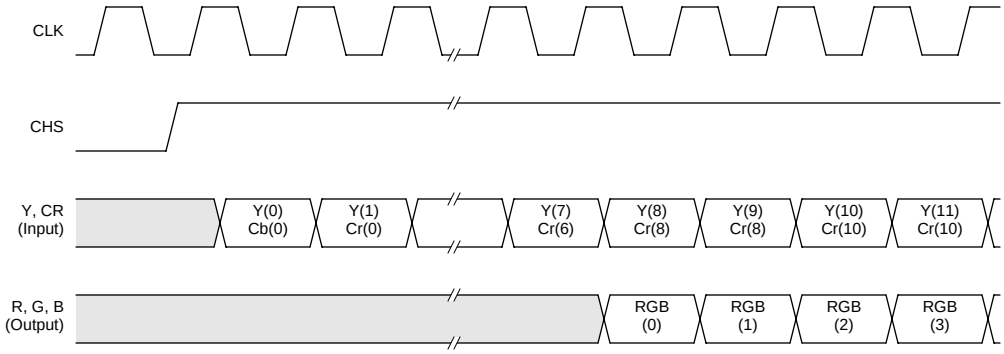


Figure 7. YCbCr to RGB Timing, MODE = 001

MODE = 010

This mode is similar to MODE = 001, with the addition of a filtering stage in decimation and interpolation. A three tap decimation filter is used, and the interpolation is performed by averaging adjacent samples. This is illustrated in Figures 8 and 9, respectively.

The signal timing in MODE = 010 is as shown in Figures 6 and 7.

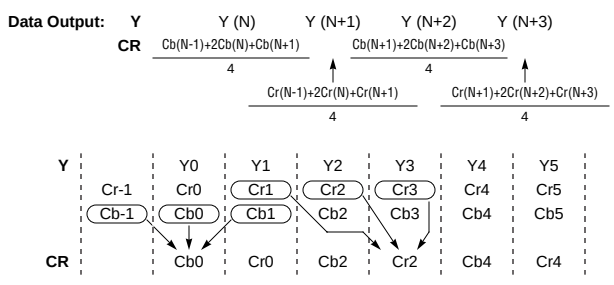


Figure 8. Illustration of Decimation Method, MODE = 010

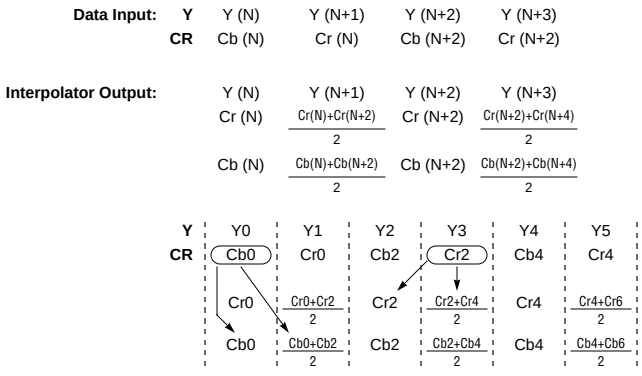


Figure 9. Illustration of Interpolation Method, MODE = 001

MODE = 011

In this mode, YCbCr data is in 4:1:1 format, with one sample each of Cb and Cr for every four samples of Y. Cb and Cr are multiplexed on the CR pins, valid for two clock cycles each.The CB pins are not used. Decimation in forward conversion, and interpolation in inverse conversion, are performed as illustrated in Figures 10 and 11.

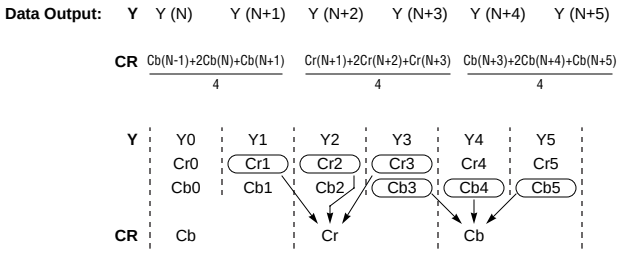


Figure 10. Illustration of Decimation Method, MODE = 011

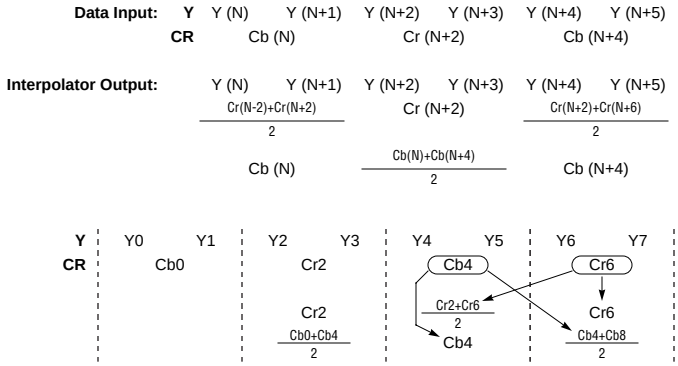


Figure 11. Illustration of Interpolation Method, MODE = 011

CHS determines the validity of input data and synchronizes the multiplexing of Cr and Cb on the CR pins. As shown in Figure 12 for forward conversion, and Figure 13 for inverse conversion, the second rising edge of CLK following the rising edge of CHS latches the first valid input data sample and determines the multiplex order.

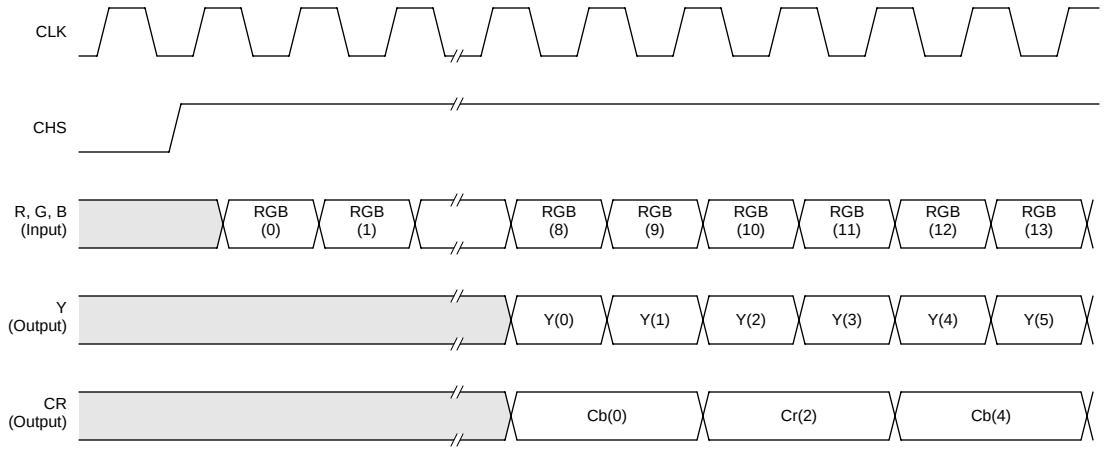


Figure 12. RGB to YCbCr Timing, MODE = 011

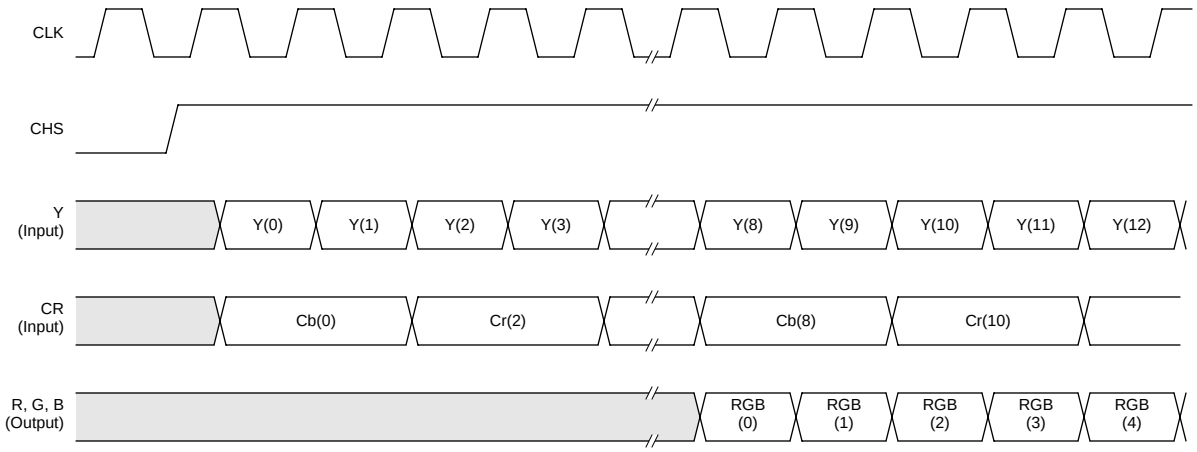


Figure 13. YCbCr to RGB Timing, MODE = 011

MODE = 110

In this mode, the YCbCr format is 4:4:4, but the YCbCr pixel rate is one half the RGB pixel rate. The CR pins carry the Cr data and the CB pins carry the Cb data. In forward conversion, the YCbCr data is 2:1 decimated through a three tap filter, as illustrated in Figure 14. In inverse conversion, the input YCbCr data is interpolated by averaging two adjacent samples, as illustrated in Figure 15.

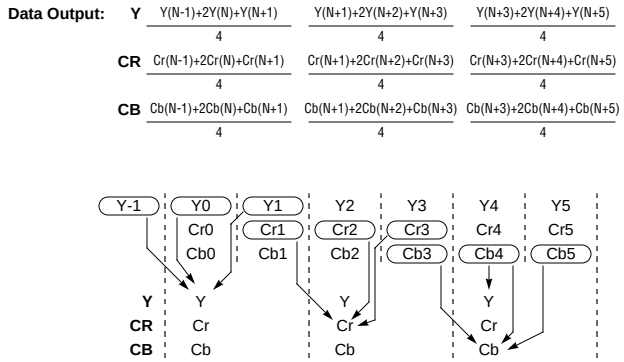


Figure 14. Illustration of Decimation, MODE = 110

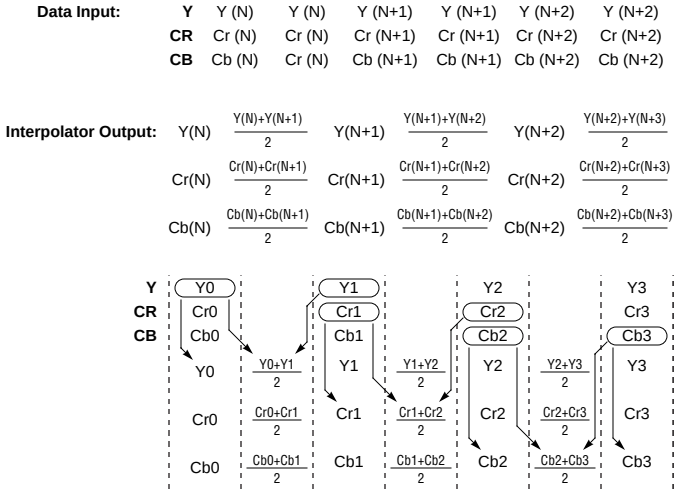


Figure 15. Illustration of Interpolation, MODE = 110

CHS determines the validity of input data and synchronizes the half-clock-rate data transitions on the Y, CR and CB pins. As shown in Figure 16 for forward conversion, and Figure 17 for inverse conversion, the second rising edge of CLK following the rising edge of CHS latches the first valid input data sample.

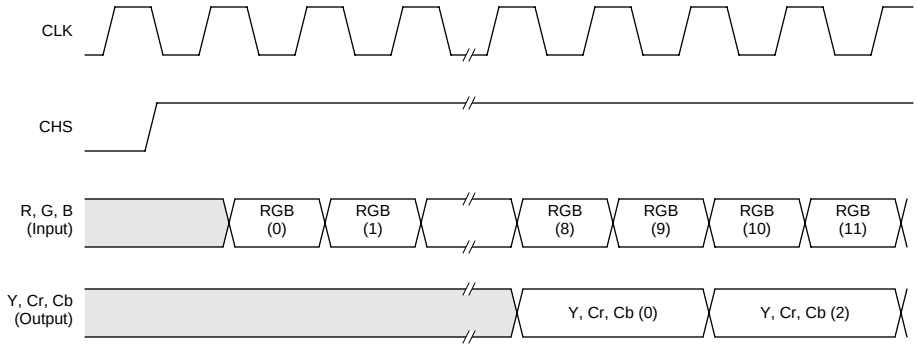


Figure 16. RGB to YCbCr Timing, MODE = 110

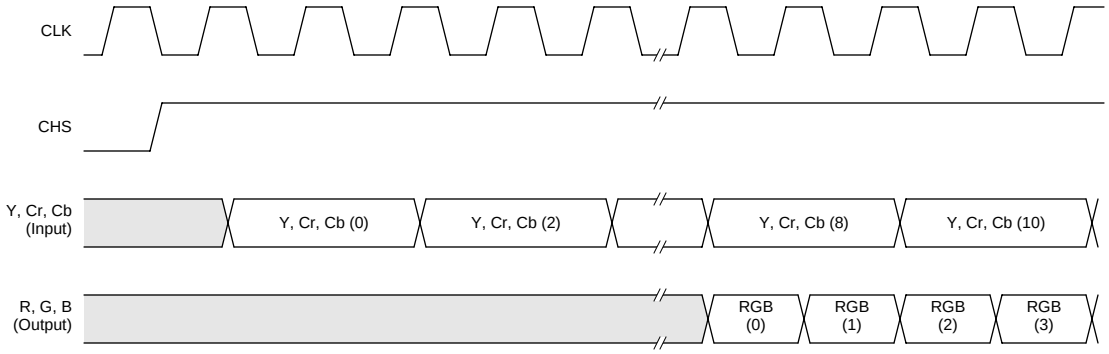


Figure 17. YCbCr to RGB Timing, MODE = 110

MODE = 111

In this mode, YCbCr data is in 4:2:2 format, with Cb and Cr multiplexed on the CR pins, and the data rate of Y, Cb and Cr is reduced by an additional factor of two. The decimation method for forward conversion is illustrated in Figure 17, and the interpolation method for inverse conversion in Figure 18.

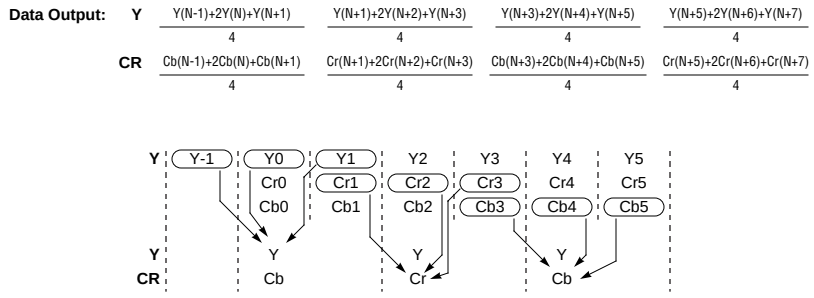


Figure 18. Illustration of Decimation, MODE = 111

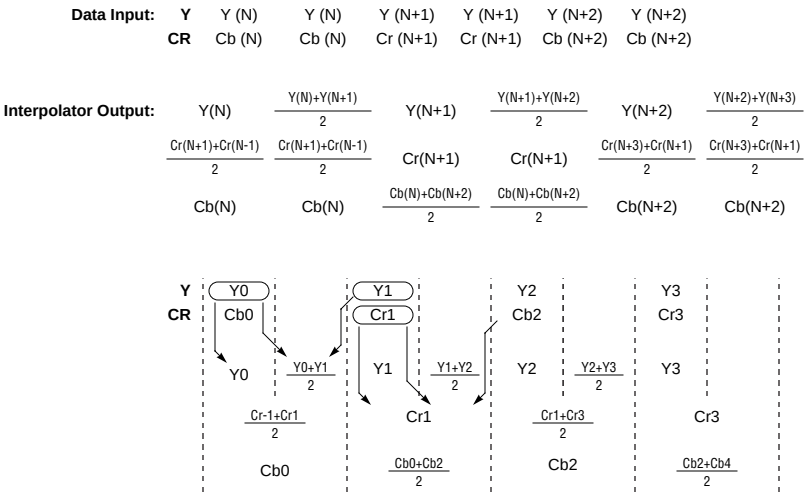


Figure 19. Illustration of Interpolation, MODE = 111

CHS determines the validity of input data and synchronizes the half-clock-rate data transitions on the Y, CR pins, and the multiplexing of Cb and Cr. As shown in Figure 20 for forward conversion, and Figure 21 for inverse conversion, the second rising edge of CLK following the rising edge of CHS latches the first valid input data sample.

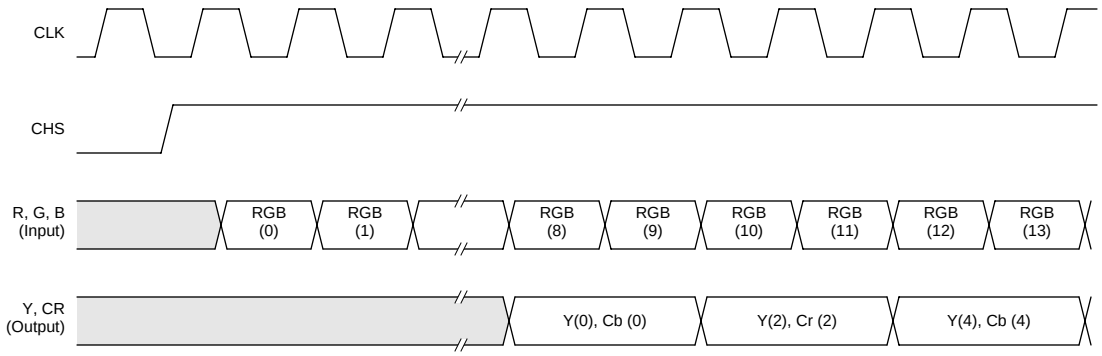


Figure 20. RGB to YCbCr Timing, MODE = 111

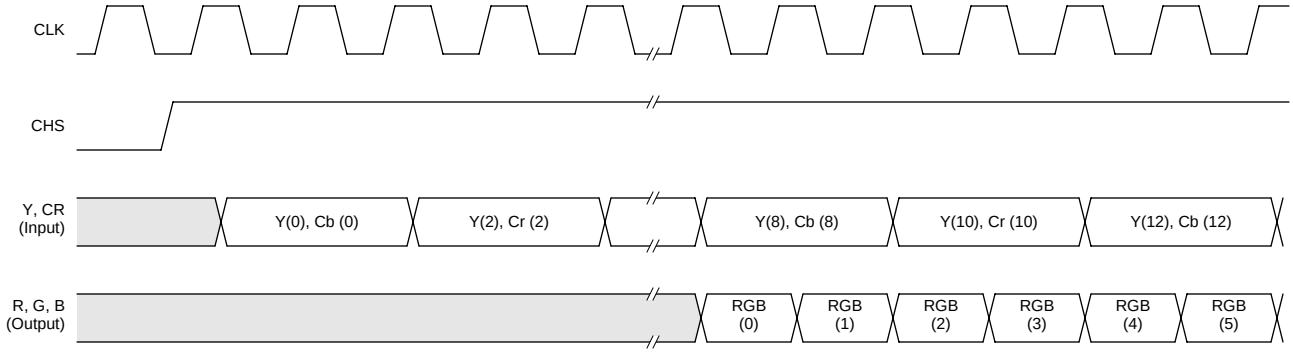


Figure 21. YCbCr to RGB timing, MODE = 111

ABSOLUTE MAXIMUM RATINGS

Storage Temperature..... -65°C to +150°C
Supply Voltage to Ground .....-0.3V to +7.0V
DC Output Voltage ..... -0.3V to V_{CC}+0.3V
DC Input Voltage ..... -0.3V to V_{CC}+0.3V
DC Input Current.....-10mA to +10mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Temperature .....$0°C \le T_A \le +70°C$
Supply Voltage .....$4.75V \le V_{CC} \le 5.25V$

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400µA
I_{CC}	Power Supply Current		90		mA	V_{CC} = 5.0 V, C_L = 20pF, T_A = 25°C, 30 MHz
I_{LI}	Input Leakage Current			±10	µA	$V_{IN} = V_{CC}$ or V_{SS}
I_{OZ}	Output Leakage Current			±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, output disabled

During AC testing, inputs are driven at 0.4V and 2.4V levels. Unless othrewise specified, switching times are measured from the 1.5V level of DCLK to the 0.8V or 2.0V levels at the input/output.

Figure 22. AC Testing Input, Output

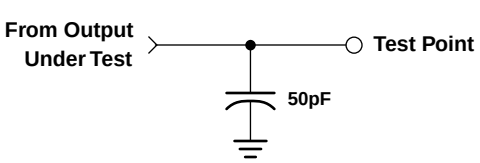


Figure 23. Normal AC Test Load

AC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
T_{CP}	Clock period	33		ns	
T_{CWH}	Clock high width	10		ns	
T_{CWL}	Clock low width	10		ns	
T_{DS}	Input data setup time	7		ns	
T_{DH}	Input data hold time	1		ns	
T_{DD}	Output data delay time	4	18	ns	C_L = 50pF
T_{OD}	Output disable time	3		ns	
T_{OE}	Output enable time		13	ns	
T_{OS}	$\overline{OE}$ setup time	5		ns	
T_{OH}	$\overline{OE}$ hold time	1		ns	
T_{SW}	CHS pulse width	T_{CP}			
T_{SI}	CHS setup time	3		ns	
T_{SH}	CHS hold time	0		ns	
T_{RW}	$\overline{RST}$ pulse width	$2*T_{CP}$			
T_{RS}	$\overline{RST}$ setup time	5		ns	
T_{RH}	$\overline{RST}$ hold time	1		ns	

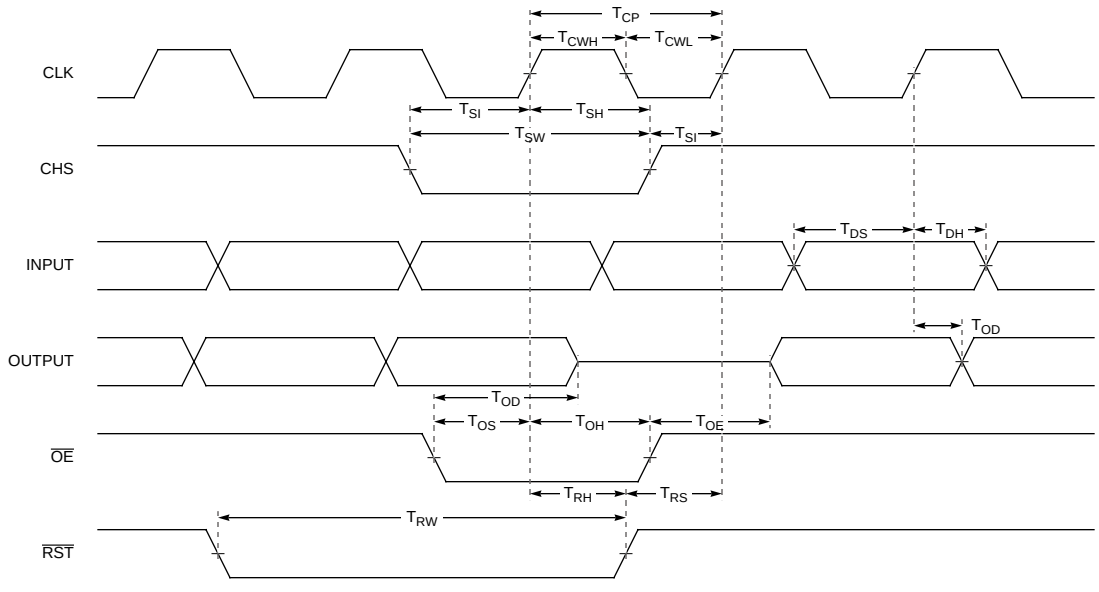


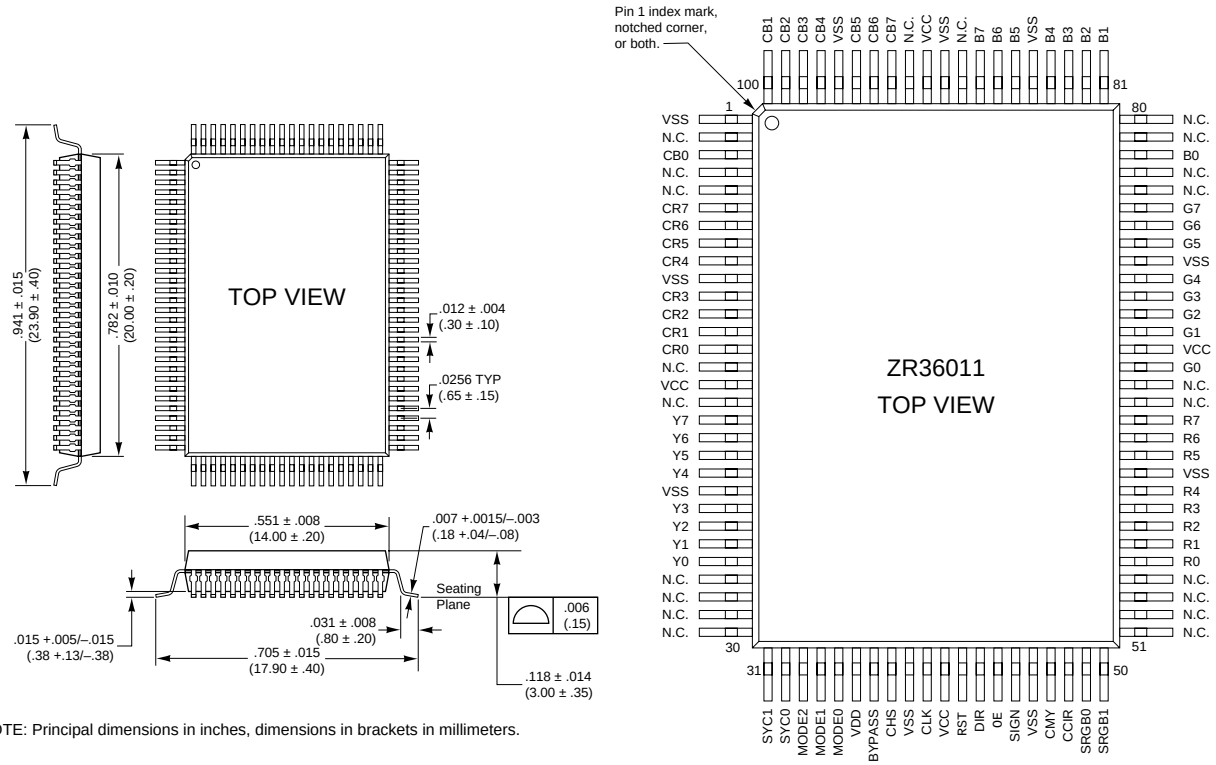
Figure 24. Input Timing Requirements and Output Switching Characteristics

PACKAGE INFORMATION

100-Pin Flat Pack Pin Assignment

Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
1	VSS	P	21	Y4	B	41	VCC	P	61	R5	B	81	B1	B
2	N.C.	-	22	VSS	P	42	$\overline{RST}$	I	62	R6	B	82	B2	B
3	CB0	B	23	Y3	B	43	DIR	I	63	R7	B	83	B3	B
4	N.C.	-	24	Y2	B	44	$\overline{OE}$	I	64	N.C.	-	84	B4	B
5	N.C.	-	25	Y1	B	45	SIGN	I	65	N.C.	-	85	VSS	P
6	CR7	B	26	Y0	B	46	VSS	P	66	G0	B	86	B5	B
7	CR6	B	27	N.C.	-	47	CMY	I	67	VCC	P	87	B6	B
8	CR5	B	28	N.C.	-	48	CCIR	I	68	G1	B	88	B7	B
9	CR4	B	29	N.C.	-	49	SRGB0	B	69	G2	B	89	N.C.	-
10	VSS	P	30	N.C.	-	50	SRGB1	B	70	G3	B	90	VSS	P
11	CR3	B	31	SYC1	B	51	N.C.	-	71	G4	B	91	VCC	P
12	CR2	B	32	SYC0	B	52	N.C.	-	72	VSS	P	92	N.C.	-
13	CR1	B	33	MODE2	I	53	N.C.	-	73	G5	B	93	CB7	B
14	CR0	B	34	MODE1	I	54	N.C.	-	74	G6	B	94	CB6	B
15	N.C.	-	35	MODE0	I	55	R0	B	75	G7	B	95	CB5	B
16	VCC	P	36	VCC	P	56	R1	B	76	N.C.	-	96	VSS	P
17	N.C.	-	37	BYPASS	I	57	R2	B	77	N.C.	-	97	CB4	B
18	Y7	B	38	CHS	I	58	R3	B	78	B0	B	98	CB3	B
19	Y6	B	39	VSS	P	59	R4	B	79	N.C.	-	99	CB2	B
20	Y5	B	40	CLK	I	60	VSS	P	80	N.C.	-	100	CB1	B

P = Power, I = Input, B = Bidirectional

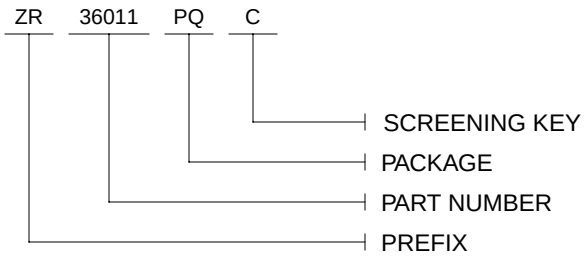


NOTE: Principal dimensions in inches, dimensions in brackets in millimeters.

Figure 25. ZR36011 Plastic Quad Flat Pack

Notes:

ORDERING INFORMATION



PACKAGE

PQ - Plastic Quad Flat Pack (EIAJ)

SCREENING KEY

C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)

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