PEMD13; PUMD13

NPN/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 47 kΩ

Rev. 3 — 7 December 2011 Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/NPN complement	Package configuration
	NXP	JEITA			
PEMD13	SOT666	-	PEMB13	PEMH13	ultra small and flat lead
PUMD13	SOT363	SC-88	PUMB13	PUMH13	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

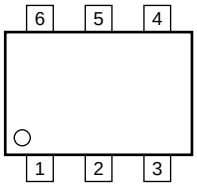
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		8	10	12	

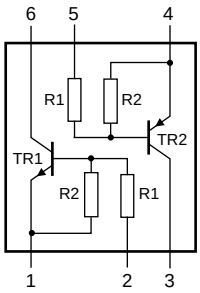
2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		



001aab555



006aaa143

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMD13	-	plastic surface-mounted package; 6 leads	SOT666
PUMD13	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PEMD13	Z1
PUMD13	3*1

[1] * = placeholder for manufacturing site code

5. Limiting values

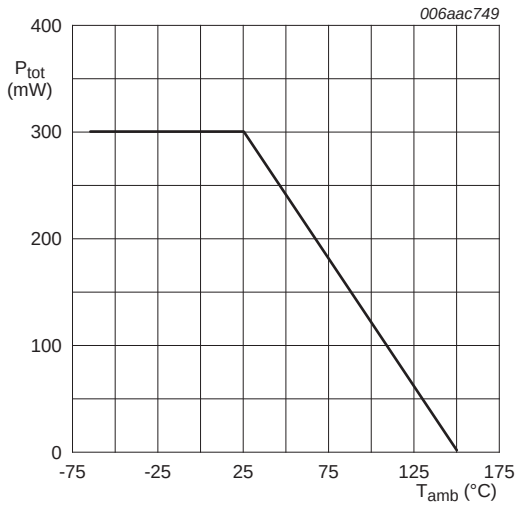
Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
V_I	input voltage TR1					
	positive			-	+30	V
	negative			-	–5	V
	input voltage TR2					
	positive			-	+5	V
	negative			-	–30	V
I_O	output current			-	100	mA
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD13 (SOT666)		[1][2]	-	200	mW
	PUMD13 (SOT363)		[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD13 (SOT666)		[1][2]	-	300	mW
	PUMD13 (SOT363)		[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–65	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 1. Per device: Power derating curve for SOT363 (SC-88) and SOT666

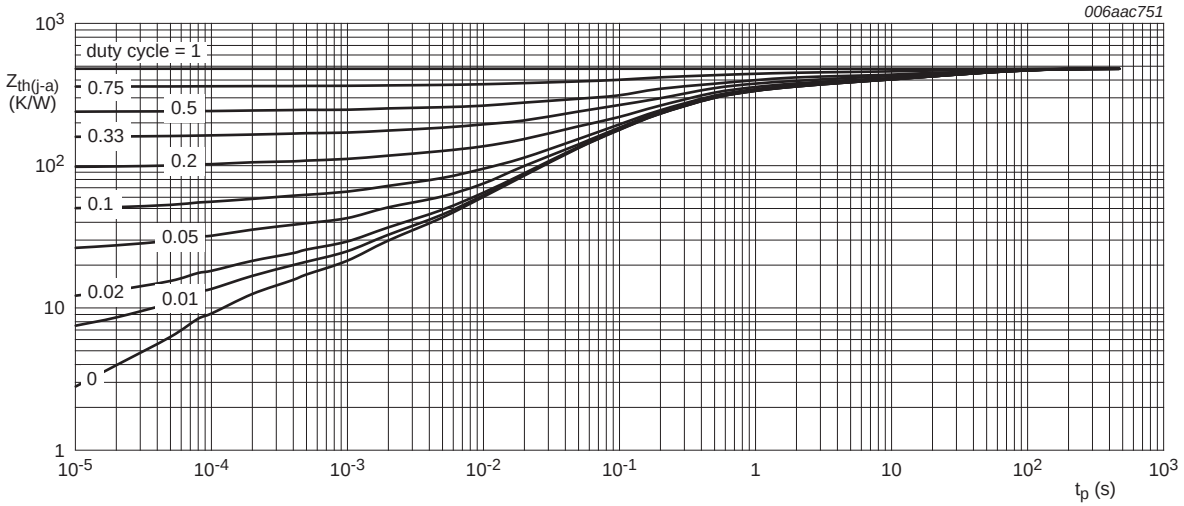
6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	PEMD13 (SOT666)		[1][2]	-	-	625	K/W
	PUMD13 (SOT363)		[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	PEMD13 (SOT666)		[1][2]	-	-	417	K/W
	PUMD13 (SOT363)		[1]	-	-	417	K/W

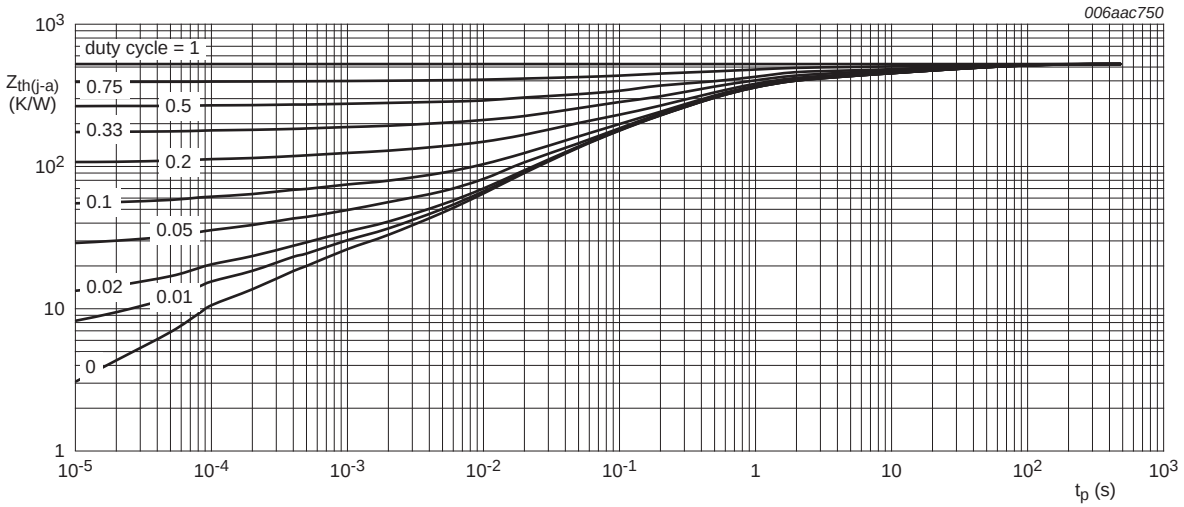
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD13 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMD13 (SOT363); typical values

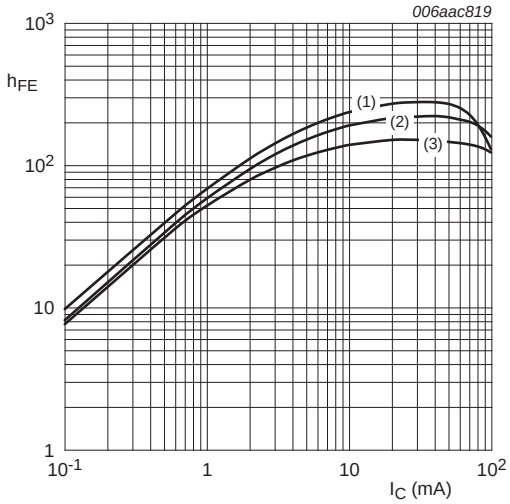
7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A	-	-	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	-	-	5	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	-	-	170	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 5 mA; I_B = 0.25 mA	-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 μA	-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 5 mA	1.3	0.9	-	V
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		8	10	12	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz [1]				
	TR1 (NPN)		-	230	-	MHz
	TR2 (PNP)		-	180	-	MHz

[1] Characteristics of built-in transistor



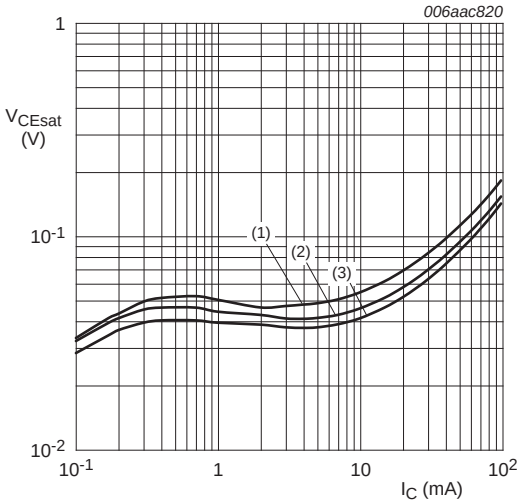
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values



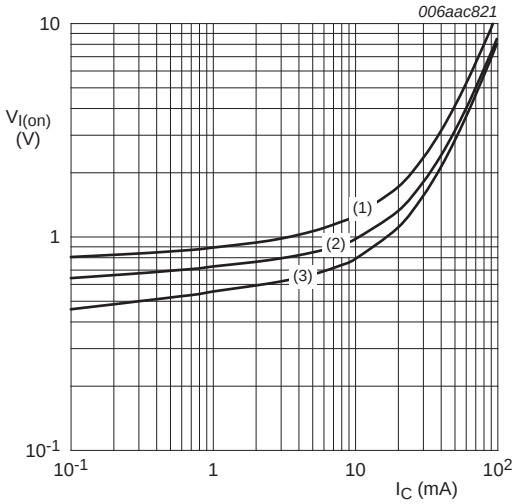
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



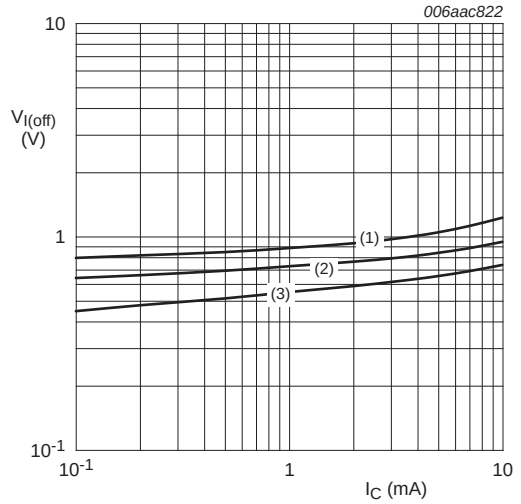
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



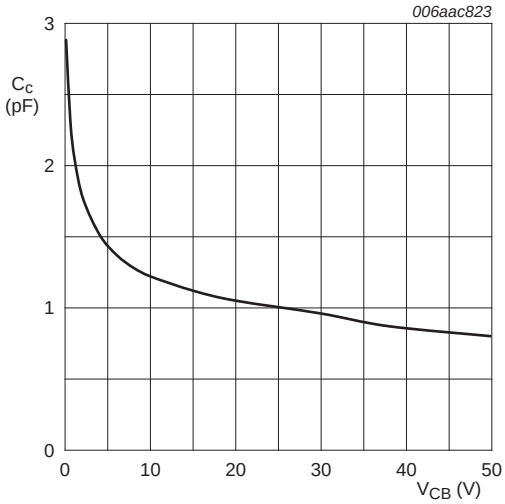
V_{CE} = 5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

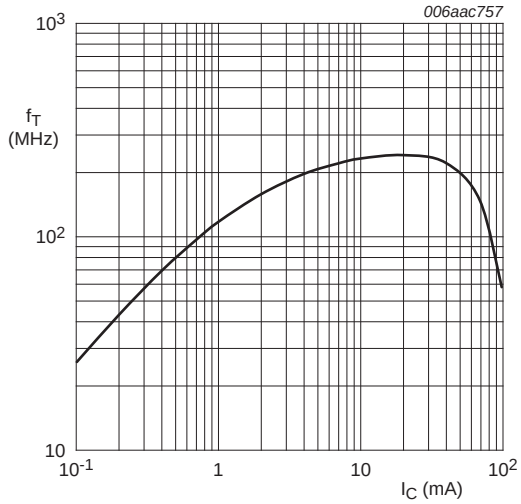
(3) T_{amb} = 100 °C

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



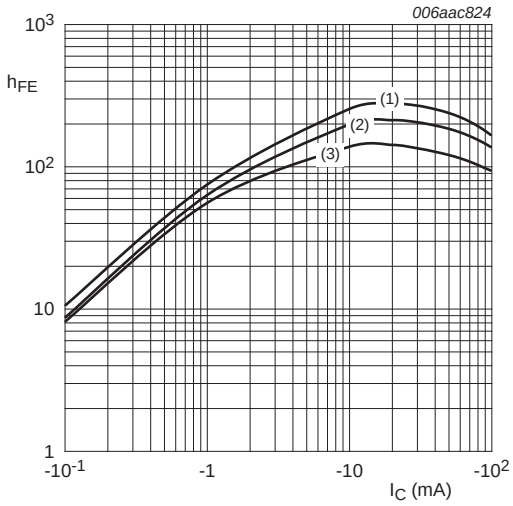
f = 1 MHz; T_{amb} = 25 °C

Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = 5 V; T_{amb} = 25 °C

Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



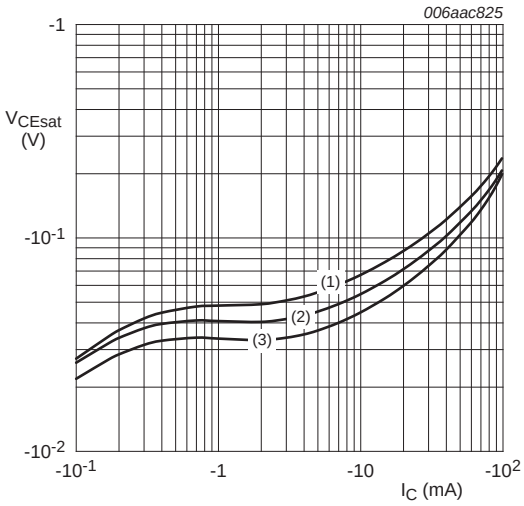
V_{CE} = −5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values



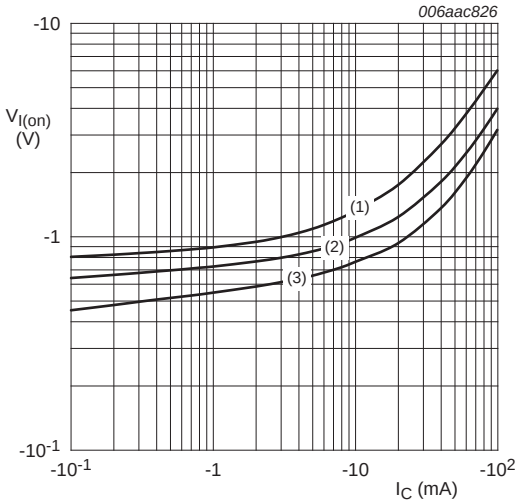
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



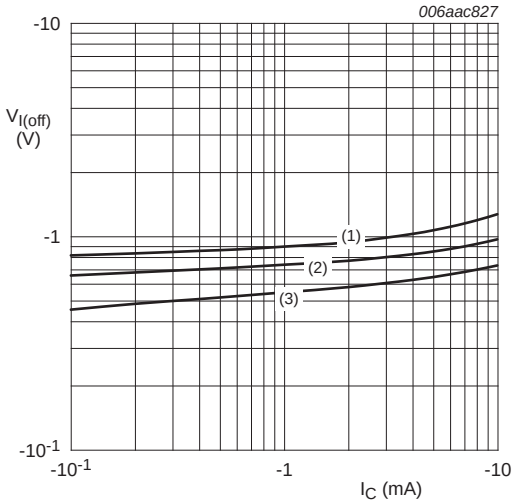
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values



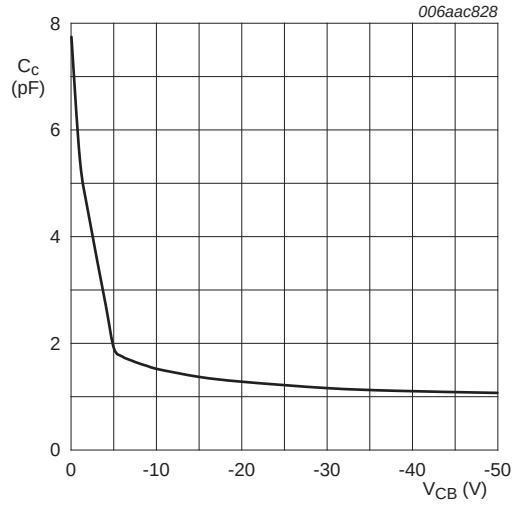
V_{CE} = −5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

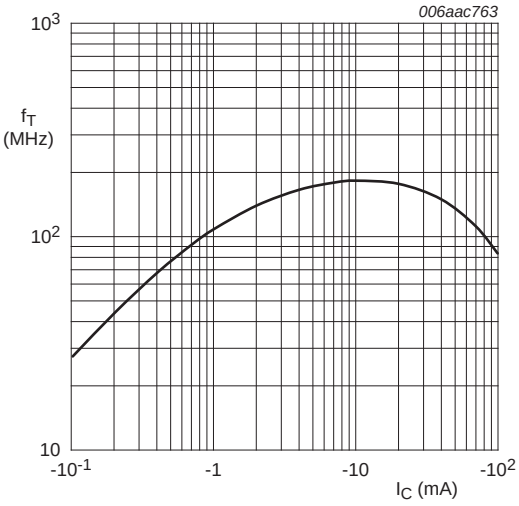
(3) T_{amb} = 100 °C

Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = −5 V; T_{amb} = 25 °C

Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

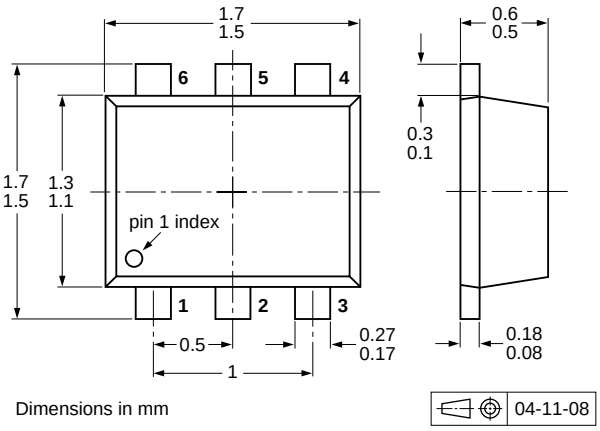


Fig 16. Package outline PEMD13 (SOT666)

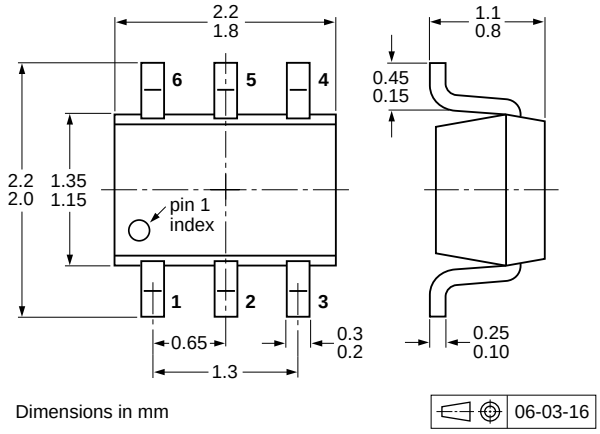


Fig 17. Package outline PUMD13 (SOT363)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

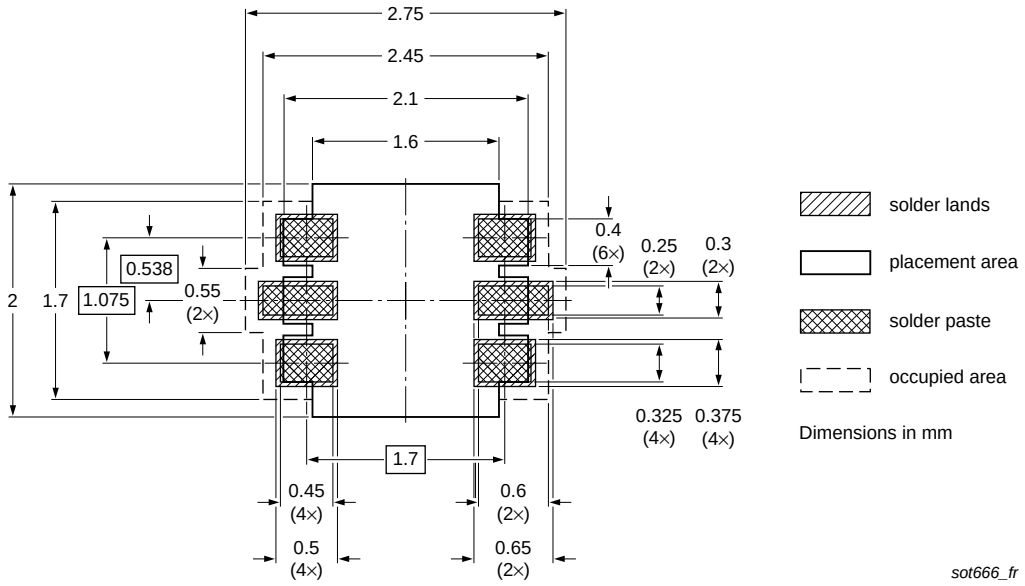
Type number	Package	Description		Packing quantity			
				3000	4000	8000	10000
PEMD13	SOT666	2 mm pitch, 8 mm tape and reel		-	-	-315	-
		4 mm pitch, 8 mm tape and reel		-	-115	-	-
PUMD13	SOT363	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 18. Reflow soldering footprint PEMD13 (SOT666)

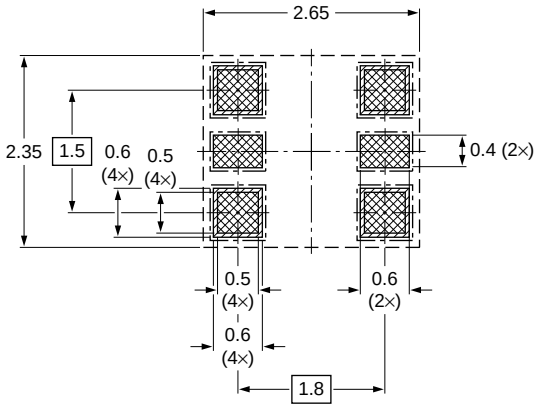


Fig 19. Reflow soldering footprint PUMD13 (SOT363)

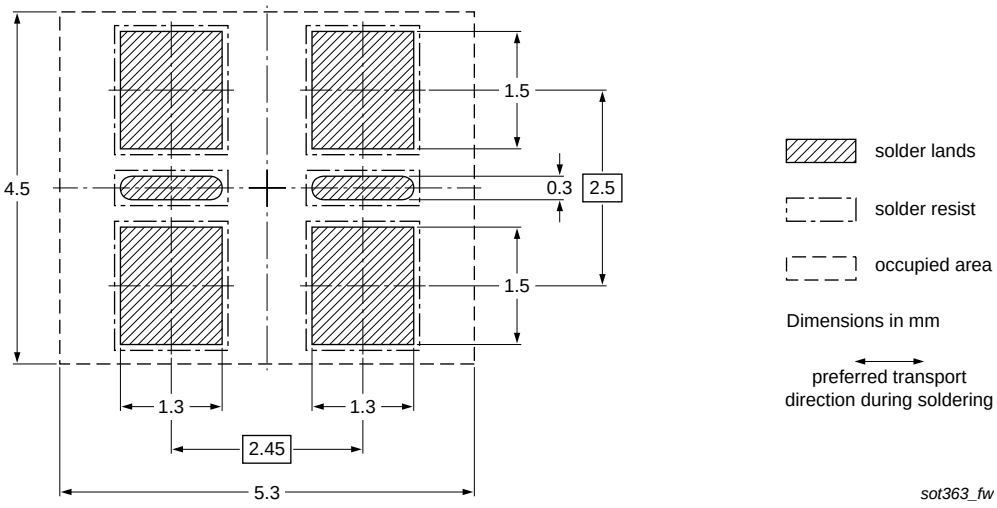


Fig 20. Wave soldering footprint PUMD13 (SOT363)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD13_PUMD13 v.3	20111207	Product data sheet	-	PEMD13_PUMD13 v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 “Product profile”: updated • Section 4 “Marking”: updated • Figure 1 to 15: added • Section 5 “Limiting values”: updated • Section 6 “Thermal characteristics”: updated • Table 8 “Characteristics”: $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated, f_T added • Section 8 “Test information”: added • Section 9 “Package outline”: superseded by minimized package outline drawings • Section 10 “Packing information”: added • Section 11 “Soldering”: added • Section 13 “Legal information”: updated			
PEMD13_PUMD13 v.2	20031008	Product data sheet	-	PEMD13 v.1 PUMD13 v.1
PEMD13 v.1	20010911	Preliminary specification	-	-
PUMD13 v.1	20010227	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 December 2011
Document identifier: PEMD13_PUMD13