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# 1.1 Overview

## 1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EFA6/A5/A1/A0 has an internal 32 KB of ROM and 1 KB of RAM. Peripheral functions include 5 external interrupts, including NMI, 8 timer counters, 3 (MN101EFA5/A0: 2) types of serial interfaces, A/D converter, watchdog timer and buzzer output (MN101EFA5/A0: no buzzer). The system configuration is suitable for system control microcontroller.

With 2 oscillation systems (internal frequency: 16 MHz, crystal/ceramic frequency: max. 10 MHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

## 1.1.2 Product Summary

This manual describes the following model.

Table:1.1.1 Product Summary

| Model | ROM Size | RAM Size | Classification | Capacitive Touch Detection Circuit | Package |
|-------|----------|----------|----------------|-----------------------------------|---------|
| MN101EFA6A | 32 KB | 1 KB | Flash EEPROM version | √ | 44-Pin QFP 48-Pin TQFP |
| MN101EFA1A | 32 KB | 1 KB | Flash EEPROM version | - | |
| MN101EFA5A | 32 KB | 1 KB | Flash EEPROM version | √ | 32-Pin SSOP 32-Pin TQFP |
| MN101EFA0A | 32 KB | 1 KB | Flash EEPROM version | - | |

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# 1.2 Hardware Functions

■ Feature

- ROM capacity: 32 KB
- RAM capacity: 1 KB

- Package:
    MN101EFA6/A1
        44-Pin QFP (10 mm × 10 mm / 0.8 mm pitch)
        48-Pin TQFP (7 mm × 7 mm / 0.5 mm pitch)

    MN101EFA5/A0
        32-Pin TQFP (7 mm × 7 mm / 0.8mm pitch)
        32-Pin SSOP (6.1 mm × 11 mm / 0.65mm pitch, halogen free)

    Panasonic "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.
        - Bromine : 900 ppm (Maximum Concentration Value)
        - Chlorine : 900 ppm (Maximum Concentration Value)
        - Bromine + Chlorine : 1500 ppm (Maximum Concentration Value)
    The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
    Antimony and its compounds are not added intentionally.

- Machine Cycle:
    0.05 μs / fs: 20 MHz (4.0 V to 5.5 V)

- Oscillation circuit: 2 channel oscillation circuit
    Internal oscillation (frc): 16 MHz
    Crystal/ceramic (fosc): Maximum 10 MHz

-Clock Multiplication circuit (PLL Circuit)
    PLL circuit output clock (fpll): fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
                                    $1/2 \times$ frc multiplication by 4, 5 enable

-Clock Gear for System Clock
    System Clock (fs): fpll divided by 1, 2, 4, 16, 32, 64, 128

-Clock Gear for control clock of peripheral function
    Control clock of peripheral function (fpll-div): stop or fpll divided by 1, 2, 4, 8, 16

- Operation Mode:
    NORMAL mode
    HALT mode
    STOP mode
    (The operation clock can be switched in each mode.)

- Operating Voltage: 4.0 V to 5.5 V

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- Operation ambient temperature: -40 °C to +85 °C

- Interrupt:
    MN101EFA6: 27 levels
    MN101EFA1: 23 levels
    MN101EFA5: 25 levels
    MN101EFA0: 21 levels

    <Non-maskable interrupt>
        - Non-maskable interrupt and Watchdog timer overflow interrupt

    <Timer interrupts>
        - Timer 0 interrupt
        - Timer 1 interrupt
        - Timer 2 interrupt
        - Timer 6 interrupt
        - Time base timer interrupt
        - Timer 7 interrupt
        - Timer 7 compare register 2 match interrupt
        - Timer 9 overflow interrupt
        - Timer 9 underflow interrupt
        - Timer 9 compare register 2 match interrupt

    <Serial Interface interrupts>
        - Serial interface 0 interrupt
        - Serial interface 0 UART reception interrupt
        - Serial interface 1 interrupt (MN101EFA5/A0 don't have this function)
        - Serial interface 1 UART reception interrupt (MN101EFA5/A0 don't have this function)
        - Serial interface 4 interrupt
        - Serial interface 4 stop condition interrupt

    <A/D interrupt>
        - A/D conversion interrupt

    <External interrupts>
        - IRQ0: Edge selectable, noise filter connection available
        - IRQ1: Edge selectable, noise filter connection available
        - IRQ2: Edge selectable, noise filter connection available, both edges interrupt
        - IRQ3: Edge selectable, noise filter connection available, both edges interrupt
        - IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

    <Touch Detect interrupts>
        - Touch detect interrupt
        - Touch detect error interrupt
        - Touch round interrupt
        - Touch data transmission interrupt
            (MN101EFA1/A0 don't have this function)

- Timer Counter: 8 timers
    - 8-bit timer for general use × 3 sets

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- 16-bit timer for general use × 1 set
- Motor control 16-bit timer × 1 set
- 8-bit free-run timer × 1 set
- Time base timer × 1 set
- Baud rate timer × 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM0IOB
- Event count
- Simple pulse measurement
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock,
  Timer A output

Timer 1 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM1IOB
- Event count
- 16-bit cascade connected (with Timer 0)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock,
  Timer A output

Timer 2 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOB
- Event count
- Simple pulse measurement
- 24-bit cascade connected (with Timer 0 and Timer 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock,
  Timer A output

Timer 6 (8-bit free-run timer, Time base timer)
  8-bit free-run timer
- Clock source
  fpll-div, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, fs
  Time base timer
- Interrupt generation cycle
  $fpll\text{-}div/2^7$, $fpll\text{-}div/2^8$, $fpll\text{-}div/2^9$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{15}$

Timer 7 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin
  TM7IOB
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 9 (Motor control 16-bit timer)
- Square wave output (Timer pulse output)
- Event count
- Complementary 3-phase PWM output can be output to large current pin TM9OD0 to TM9OD5

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(Triangle wave and saw tooth wave are supported, dead time insertion available)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer A (Baud rate timer)
- Clock output for peripheral functions
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

- Watchdog timer

  Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
  On detection of 2 errors, forcibly hard reset inside LSI.
  Operation start timing is selectable. (At reset release or write to register)

- Buzzer Output/ Reverse Buzzer Output

  Output frequency can be selected from $fpll-div/2^9$, $fpll-div/2^{10}$, $fpll-div/2^{11}$, $fpll-div/2^{12}$, $fpll-div/2^{13}$, $fpll-div/2^{14}$

- A/D Converter: 10-bit × 12 channels (MN101EFA6/A1)
                 10-bit × 8 channels (MN101EFA5/A0)

- Serial Interface: 3 channels (MN101EFA6/A1)
                    2 channels (MN101EFA5/A0)

Serial 0: UART (full duplex)/ Clock synchronous
    Clock synchronous serial interface
        - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
          Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
        - MSB/LSB can be selected as the first bit to be transferred,
          arbitrary sizes of 1 to 8 bits are selectable.
        - Sequence transmission, reception or both are available
    Full duplex UART
        - Baud rate timer, selected from Timer 0 to 2 or Timer A
        - Parity check, overrun error/ framing error detection
        - Transfer size 7 to 8 bits can be selected

Serial 1: UART (full duplex)/ Clock synchronous (MN101EFA5/A0 don't have this function)
    Clock synchronous serial interface
        - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
          Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
        - MSB/LSB can be selected as the first bit to be transferred,
          arbitrary sizes of 1 to 8 bits are selectable.
        - Sequence transmission, reception or both are available.
    Full duplex UART
        - Baud rate timer, selected from Timer 0 to 2 or Timer A
        - Parity check, overrun error/ framing error detection
        -Transfer size 7 to 8 bits can be selected

Serial 4: Multi master IIC/ Clock synchronous
    Clock synchronous serial interface
        - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/32, fs/2, fs/4,

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Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB can be selected as the first bit to be transferred,
    arbitrary sizes of 1 to 8 bits are selectable.
- Sequence transmission, reception or both are available.
Multi master IIC
- 7-bit slave address is settable.
- General call communication mode is supported.

- Automatic Reset:
    Power detection level: 4.3 V (at rising), 4.2 V (at falling)

- LED Driver: 16 pins (Port 0 or Port A)

- Touch Sensor TImer: 1 unit/ 8 channels (MN101EFA1/A0 don't have this function)

- Ports (MN101EFA6/A1)
    I/O ports                                      36 pins
        Serial Interface pins                      12 pins
        Timer I/O                                  15 pins
        Buzzer output pins                          2 pins
        A/D input pins                             12 pins
        External Interrupt pins                     6 pins
        LED (large current) driver                 16 pins (Port 0 or Port A)
        Touch sensor input pins                     8 pins (MN101EFA1 does not have this function)
        Touch sensor resistor connect pins          2 pins (MN101EFA1 does not have this function)
        High-speed oscillation                      2 pins

    Special pins                                    8 pins
        Operation mode input pins                   3 pins
        Reset input pin                             1 pin
        Analog reference voltage input pin          1 pin
        Power pins                                  3 pins
- Ports (MN101EFA5/A0)
    I/O ports                                      24 pins
        Serial Interface pins                       9 pins
        Timer I/O                                   9 pins
        A/D input pins                              8 pins
        External Interrupt pins                     5 pins
        LED (large current) driver                 16 pins (Port 0 or Port A)
        Touch sensor input pins                     8 pins (MN101EFA0 does not have this function)
        Touch sensor resistor connect pins          2 pins (MN101EFA0 does not have this function)
        High-speed oscillation                      2 pins

    Special pins                                    8 pins
        Operation mode input pins                   3 pins
        Reset input pin                             1 pin
        Analog reference voltage input pin          1 pin

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# 1.3 Pin Description

## 1.3.1 Pin configuration
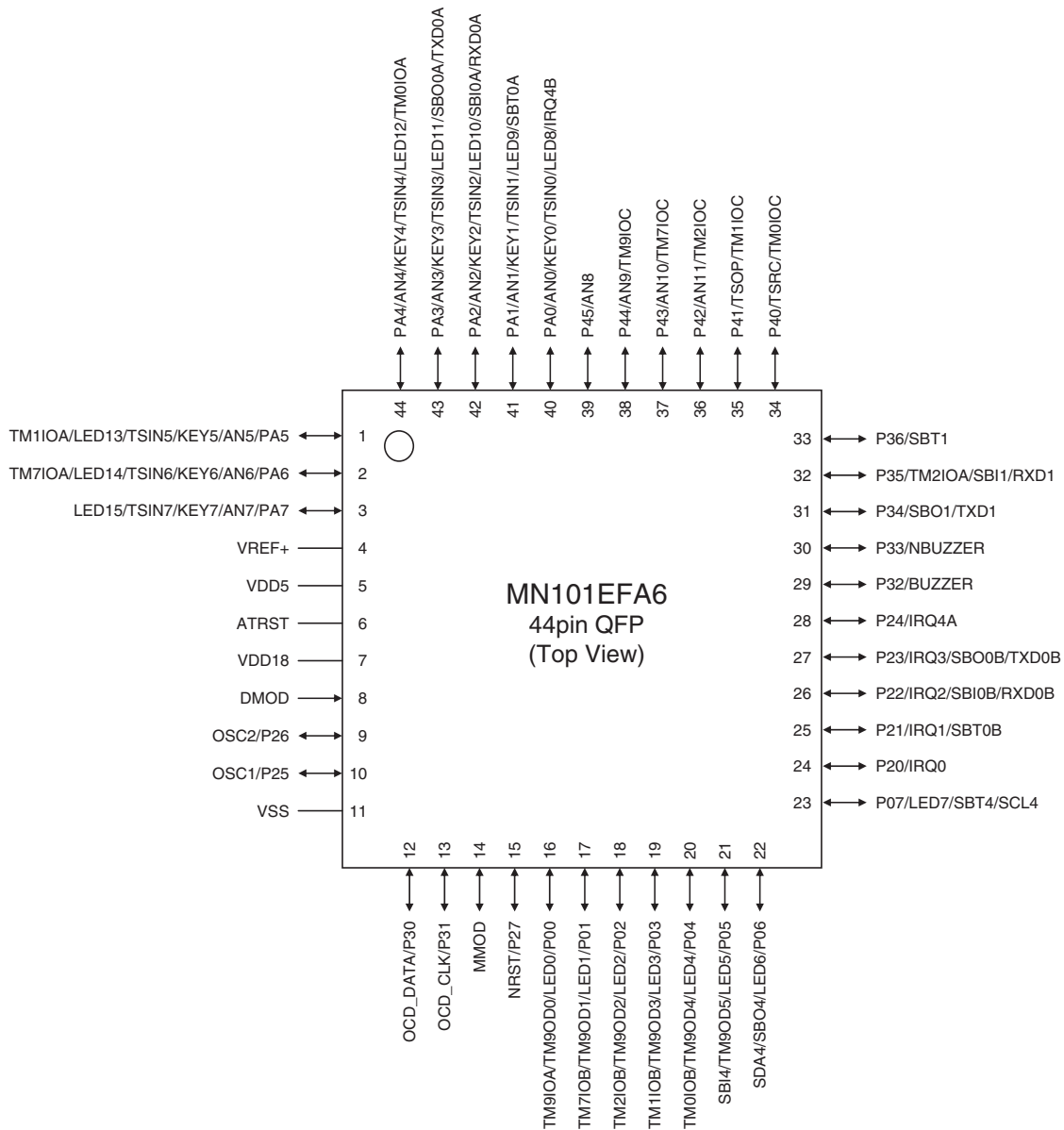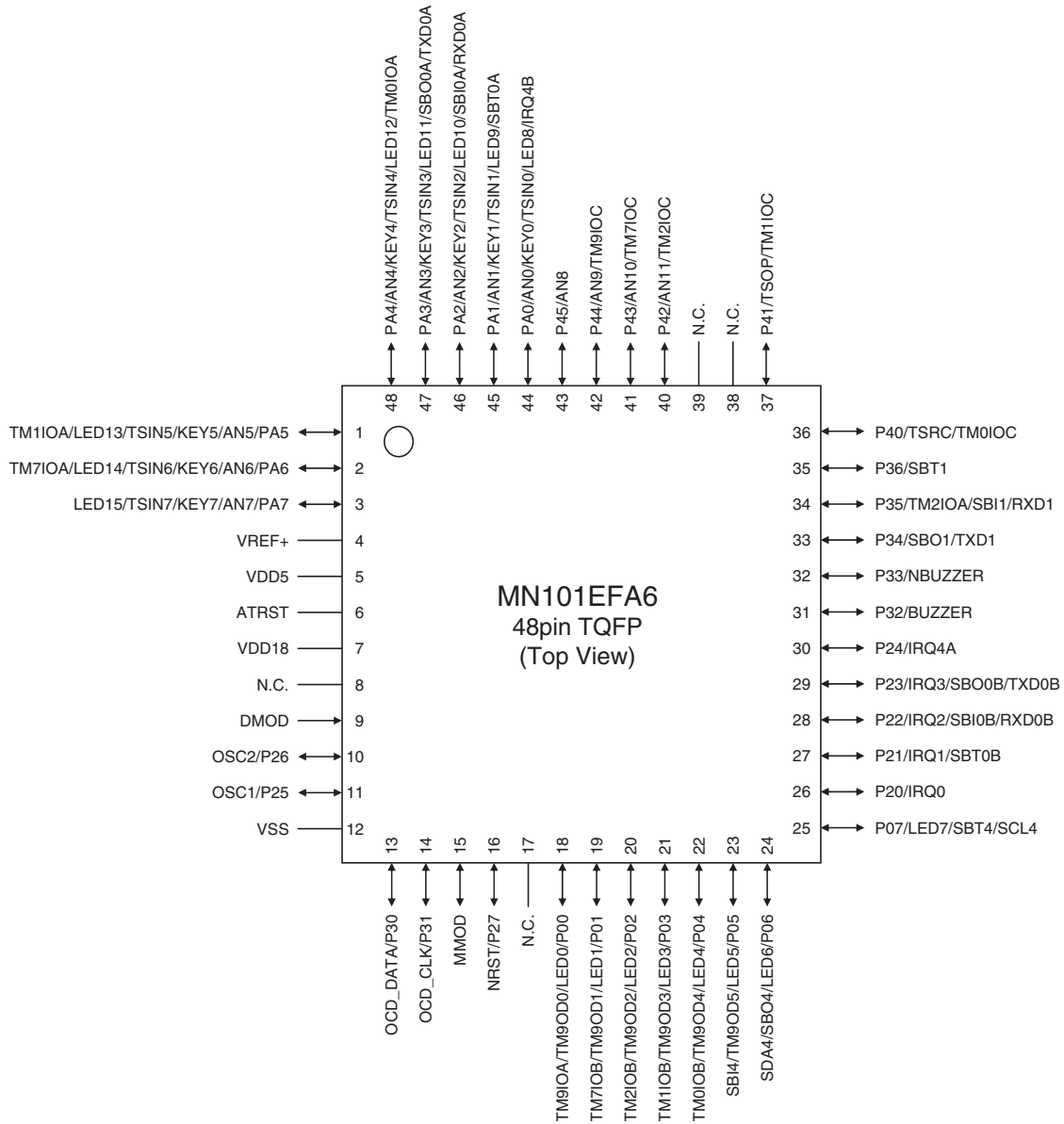


Figure:1.3.1 Pin Configuration (MN101EFA6 44-pin QFP)

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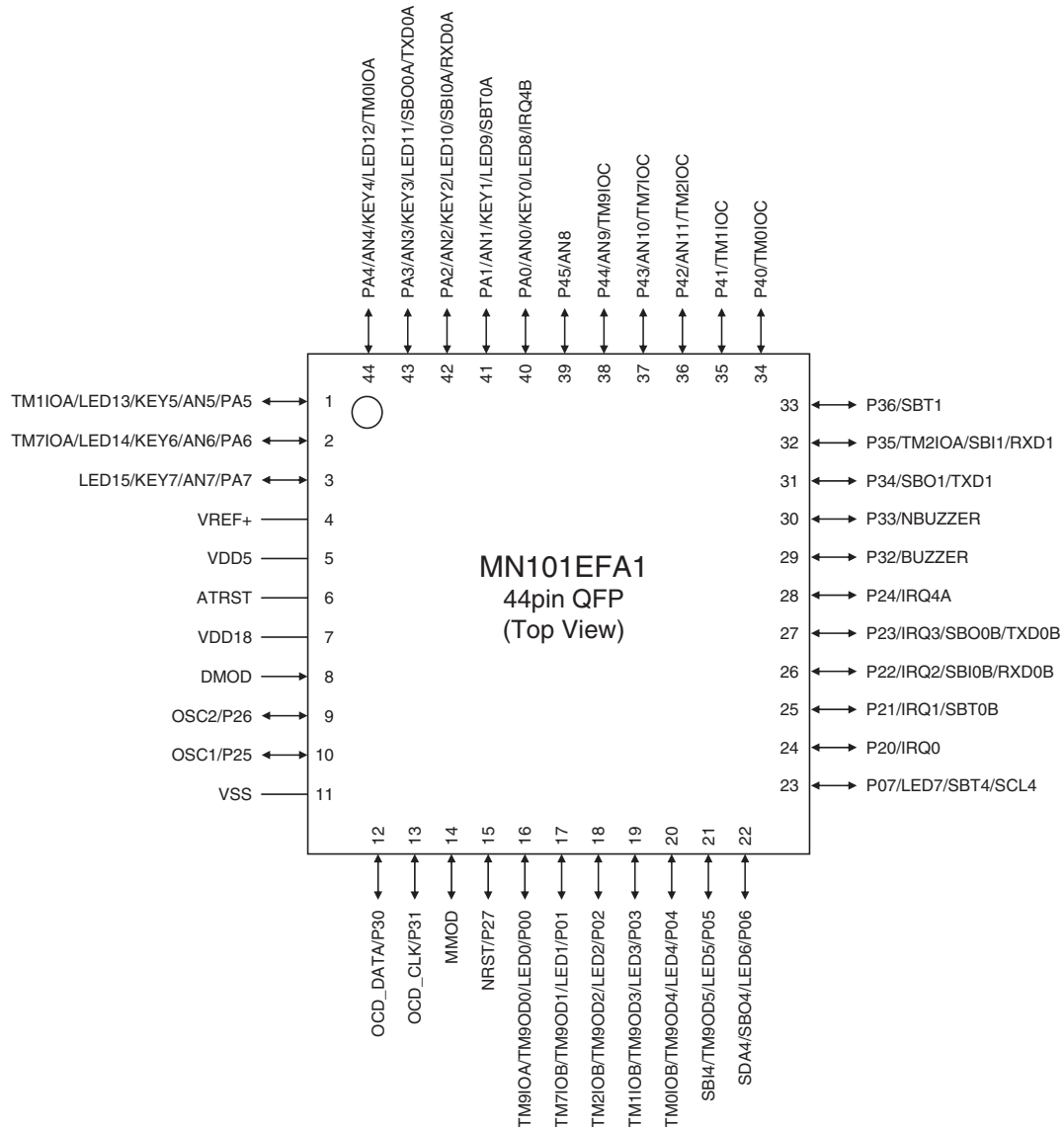


Figure:1.3.2  Pin Configuration (MN101EFA6 48-pin TQFP)

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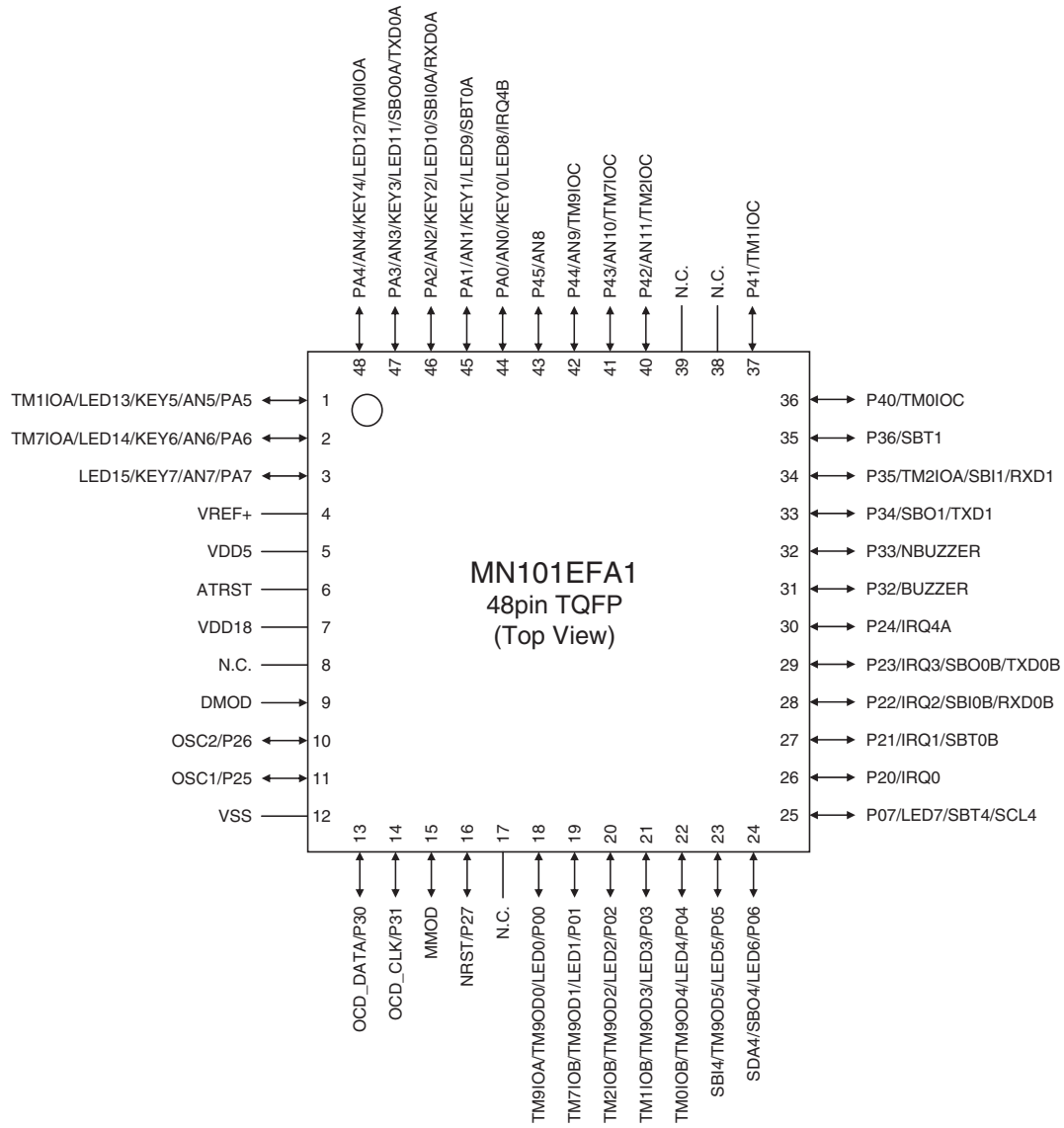Figure:1.3.3  Pin Configuration (MN101EFA1 44-pin QFP)
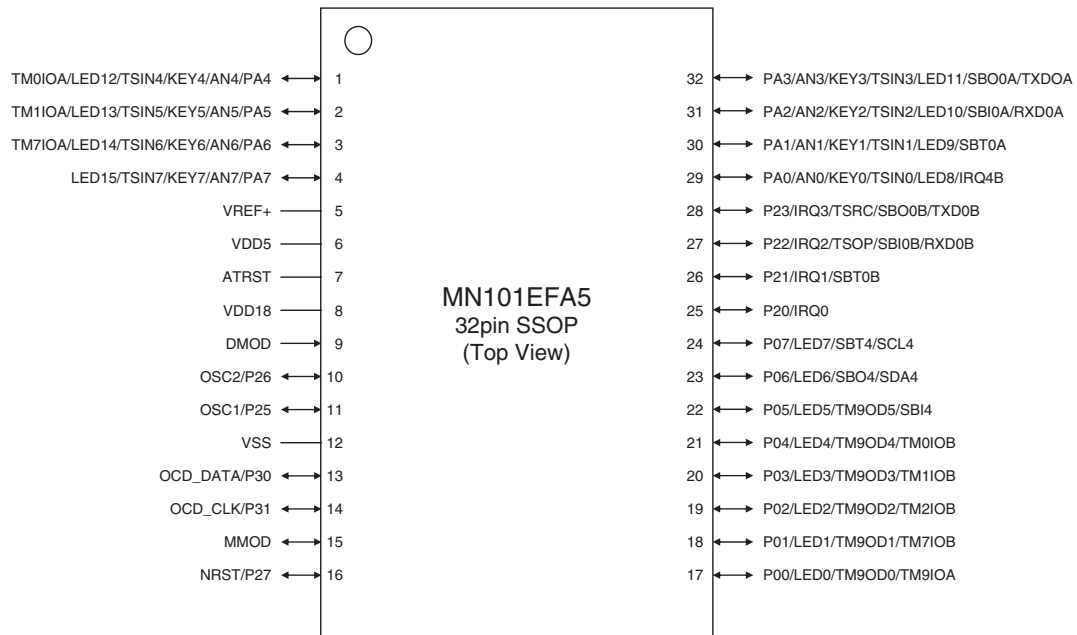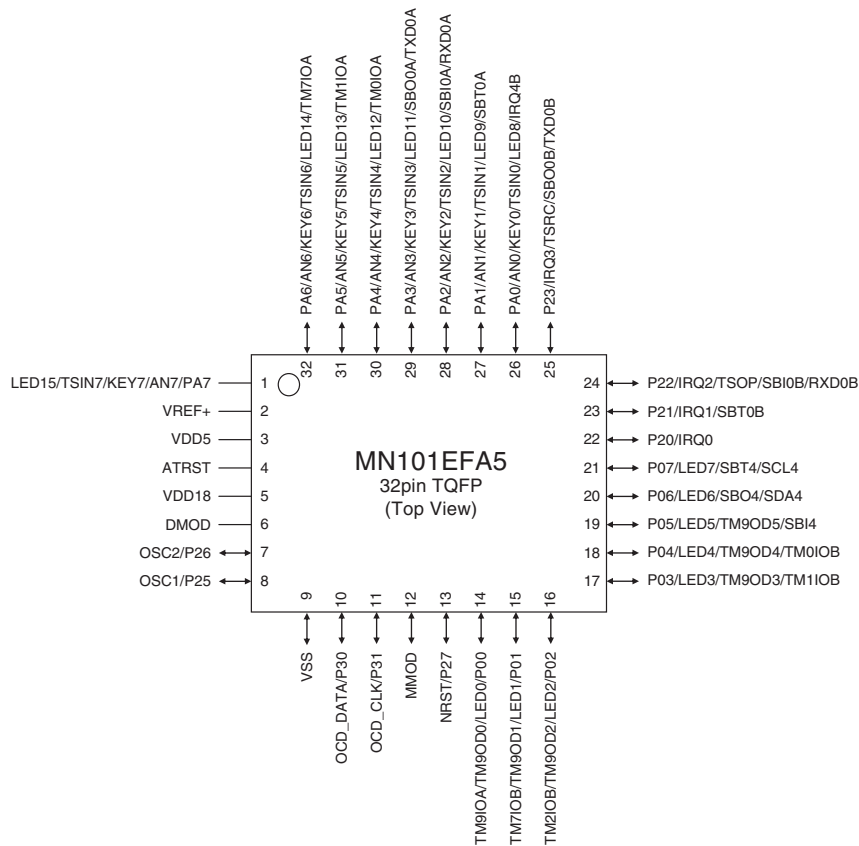
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Figure:1.3.4 Pin Configuration (MN101EFA1 48-pin TQFP)

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Figure:1.3.5  Pin Configuration (MN101EFA5 32-pin SSOP)
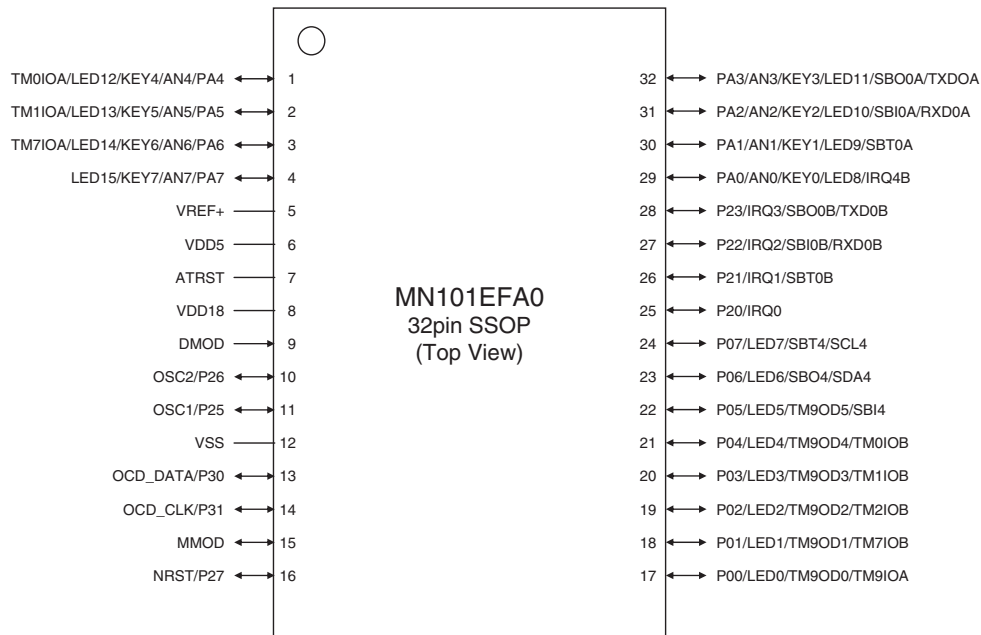


Figure:1.3.6  Pin Configuration (MN101EFA5 32-pin TQFP)

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Figure:1.3.7  Pin Configuration (MN101EFA0 32-pin SSOP)
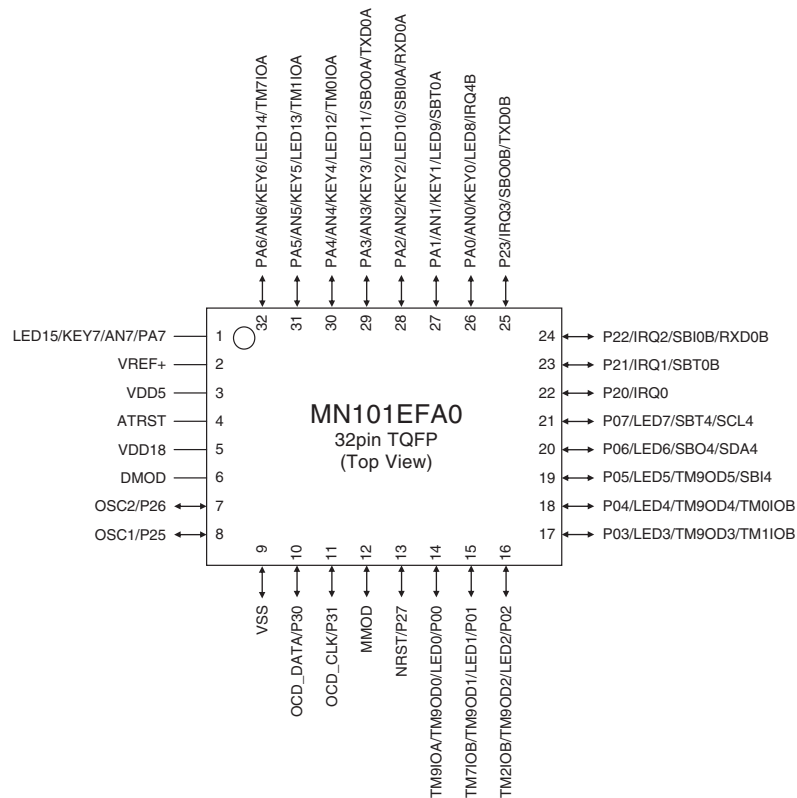


Figure:1.3.8  Pin Configuration (MN101EFA0 32-pin TQFP)

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## 1.3.2    Pin Specification

Table remarks    √: With function   -: Without function

| Pins | MN101 EFA6 | MN101 EFA1 | MN101 EFA5 | MN101 EFA0 | Special Functions | | I/O | Direction Control | Pin Control | Functions Description | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P00 | √ | √ | √ | √ | LED0 | TM9IOA | in/out | P0DIR0 | P0PLU0 | LED0:LED driving pin 0 | TM9IOA:Timer 9 input/output |
| | √ | √ | √ | √ | TM9OD0 | | | | | TM9OD0:Timer 9 output | |
| P01 | √ | √ | √ | √ | LED1 | TM7IOB | in/out | P0DIR1 | P0PLU1 | LED1:LED driving pin 1 | TM7IOB:Timer 7 input/output |
| | √ | √ | √ | √ | TM9OD1 | | | | | TM9OD1:Timer 9 output | |
| P02 | √ | √ | √ | √ | LED2 | TM2IOB | in/out | P0DIR2 | P0PLU2 | LED2:LED driving pin 2 | TM2IOB:Timer 2 input/output |
| | √ | √ | √ | √ | TM9OD2 | | | | | TM9OD2:Timer 9 output | |
| P03 | √ | √ | √ | √ | LED3 | TM1IOB | in/out | P0DIR3 | P0PLU3 | LED3:LED driving pin 3 | TM1IOB:Timer 1 input/output |
| | √ | √ | √ | √ | TM9OD3 | | | | | TM9OD3:Timer 9 output | |
| P04 | √ | √ | √ | √ | LED4 | TM0IOB | in/out | P0DIR4 | P0PLU4 | LED4:LED driving pin 4 | TM0IOB:Timer 0 input/output |
| | √ | √ | √ | √ | TM9OD4 | | | | | TM9OD4:Timer 9 output | |
| P05 | √ | √ | √ | √ | LED5 | SBI4 | in/out | P0DIR5 | P0PLU5 | LED5:LED driving pin 5 | SBI4:Serial 4 data input |
| | √ | √ | √ | √ | TM9OD5 | | | | | TM9OD5:Timer 9 output | |
| P06 | √ | √ | √ | √ | LED6 | SBO4 | in/out | P0DIR6 | P0PLU6 | LED6:LED driving pin 6 | SBO4:Serial 4 data input/output |
| | √ | √ | √ | √ | SDA4 | | | | | SDA4:Multi-master IIC4 data input/output | |
| P07 | √ | √ | √ | √ | LED7 | SBT4 | in/out | P0DIR7 | P0PLU7 | LED7:LED driving pin 7 | SBT4:Serial 4 clock input/output |
| | √ | √ | √ | √ | SCL4 | | | | | SCL4:Multi-master IIC4 clock input/output | |
| P20 | √ | √ | √ | √ | IRQ0 | | in/out | P2DIR0 | P2PLU0 | IRQ0:External interrupt 0 | |
| P21 | √ | √ | √ | √ | IRQ1 | SBT0B | in/out | P2DIR1 | P2PLU1 | IRQ1:External interrupt 1 | SBT0B:Serial 0 clock input/output |
| P22 | √ | √ | √ | √ | IRQ2 | SBI0B | in/out | P2DIR2 | P2PLU2 | IRQ2:External interrupt 2 | SBI0B:Serial 0 data input |
| | √ | √ | √ | √ | RXD0B | | | | | RXD0B:UART0 data input | |
| | - | - | √ | - | TSOP | | | | | TSOP:Touch sensor output | |
| P23 | √ | √ | √ | √ | IRQ3 | SBO0B | in/out | P2DIR3 | P2PLU3 | IRQ3:External interrupt 3 | SBO0B:Serial 0 data input/output |
| | √ | √ | √ | √ | TXD0B | | | | | TXD0B:UART0 data input/output | |
| | - | - | √ | - | TSRC | | | | | TSRC:Touch sensor RC connect | |
| P24 | √ | √ | - | - | IRQ4A | | in/out | P2DIR4 | P2PLU4 | IRQ4A:External interrupt 4 | |
| P25 | √ | √ | √ | √ | OSC1 | | in/out | P2DIR5 | P2PLU5 | OSC1:Seramic/crystal high-speed clock input | |
| P26 | √ | √ | √ | √ | OSC2 | | in/out | P2DIR6 | P2PLU6 | OSC2:Seramic/crystal high-speed clock output | |
| P27 | √ | √ | √ | √ | NRST | | in/out | - | - | NRST:Reset | |
| P30 | √ | √ | √ | √ | OCD_DATA | | in/out | P3DIR0 | P3PLU0 | OCD_DATA:On-board programmer data pin | |
| P31 | √ | √ | √ | √ | OCD_CLK | | in/out | P3DIR1 | P3PLU1 | OCD_CLK:On-board programmer clock supply pin | |
| P32 | √ | √ | - | - | BUZZER | | in/out | P3DIR2 | P3PLU2 | BUZZER:Buzzer output | |
| P33 | √ | √ | - | - | NBUZZER | | in/out | P3DIR3 | P3PLU3 | NBUZZER:Buzzer reverse output | |
| P34 | √ | √ | - | - | SBO1 | TXD1 | in/out | P3DIR4 | P3PLU4 | SBO1:Serial 1 data input/output | TXD1:UART1 data input/output |
| P35 | √ | √ | - | - | TM2IOA | SBI1 | in/out | P3DIR5 | P3PLU5 | TM2IOA:Timer 2 input/output | SBI1:Serial 1 data input |
| | √ | √ | - | - | RXD1 | | | | | RXD1:UART1 data input | |
| P36 | √ | √ | - | - | SBT1 | | in/out | P3DIR6 | P3PLU6 | SBT1:Serial 1 clock input/output | |
| P40 | √ | √ | - | - | TM0IOC | | in/out | P4DIR0 | P4PLUD0 | TM0IOC:Timer 0 input/output | |
| | √ | - | - | - | TSRC | | | | | TSRC:Touch sensor RC connect | |
| P41 | √ | √ | - | - | TM1IOC | | in/out | P4DIR1 | P4PLUD1 | TM1IOC:Timer 1 input/output | |
| | √ | - | - | - | TSOP | | | | | TSOP:Touch sensor output | |
| P42 | √ | √ | - | - | AN11 | TM2IOC | in/out | P4DIR2 | P4PLUD2 | AN11:Analog 11 input | TM2IOC:Timer 2 input/output |
| P43 | √ | √ | - | - | AN10 | TM7IOC | in/out | P4DIR3 | P4PLUD3 | AN10:Analog 10 input | TM7IOC:Timer 7 input/output |
| P44 | √ | √ | - | - | AN9 | TM9IOC | in/out | P4DIR4 | P4PLUD4 | AN9:Analog 9 input | TM9IOC:Timer 9 input/output |
| P45 | √ | √ | - | - | AN8 | | in/out | P4DIR5 | P4PLUD5 | AN8:Analog 8 input | |
| PA0 | √ | √ | √ | √ | AN0 | KEY0 | in/out | PADIR0 | PAPLU0 | AN0:Analog 0 input | KEY0:Key interrupt 0 |
| | √ | √ | √ | √ | IRQ4B | LED8 | | | | IRQ4B:External interrupt 4 | LED8:LED drive 8 |
| | √ | - | √ | - | TSIN0 | | | | | TSIN0:Touch sensor input 0 | |
| PA1 | √ | √ | √ | √ | AN1 | KEY1 | in/out | PADIR1 | PAPLU1 | AN1:Analog 1 input | KEY1:Key interrupt 1 |
| | √ | √ | √ | √ | SBT0A | LED9 | | | | SBT0A:Serial 0 clock input/output | LED9:LED drive 9 |
| | √ | - | √ | - | TSIN1 | | | | | TSIN1:Touch sensor input 1 | |

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Table remarks　√: With function　-: Without function

| Pins | MN101 EFA6 | MN101 EFA1 | MN101 EFA5 | MN101 EFA0 | Special Functions | | I/O | Direction Control | Pin Control | Functions Description | |
|------|------|------|------|------|------|------|------|------|------|------|------|
| PA2 | √ | √ | √ | √ | AN2 | KEY2 | in/out | PADIR2 | PAPLU2 | AN2:Analog 2 input | KEY2:Key interrupt 2 |
| | √ | √ | √ | √ | SBI0A | RXD0A | | | | SBI0A:Serial 0 data input | RXD0A:UART0 data input |
| | √ | √ | √ | √ | LED10 | | | | | LED10:LED drive 10 | |
| | √ | - | √ | - | TSIN2 | | | | | TSIN2:Touch sensor input 2 | |
| PA3 | √ | √ | √ | √ | AN3 | KEY3 | in/out | PADIR3 | PAPLU3 | AN3:Analog 3 input | KEY3:Key interrupt 3 |
| | √ | √ | √ | √ | SBO0A | TXD0A | | | | SBO0A:Serial 0 data input/output | TXD0A:UART0 data input/output |
| | √ | √ | √ | √ | LED11 | | | | | LED11:LED drive 11 | |
| | √ | - | √ | - | TSIN3 | | | | | TSIN3:Touch sensor input 3 | |
| PA4 | √ | √ | √ | √ | AN4 | KEY4 | in/out | PADIR4 | PAPLU4 | AN4:Analog 4 input | KEY4:Key interrupt 4 |
| | √ | √ | √ | √ | TM0IOA | LED12 | | | | TM0IOA:Timer 0 input/output | LED12:LED drive 12 |
| | √ | - | √ | - | TSIN4 | | | | | TSIN4:Touch sensor input 4 | |
| PA5 | √ | √ | √ | √ | AN5 | KEY5 | in/out | PADIR5 | PAPLU5 | AN5:Analog 5 input | KEY5:Key interrupt 5 |
| | √ | √ | √ | √ | TM1IOA | LED13 | | | | TM1IOA:Timer 1 input/output | LED13:LED drive 13 |
| | √ | - | √ | - | TSIN5 | | | | | TSIN5:Touch sensor input 5 | |
| PA6 | √ | √ | √ | √ | AN6 | KEY6 | in/out | PADIR6 | PAPLU6 | AN6:Analog 6 input | KEY6:Key interrupt 6 |
| | √ | √ | √ | √ | TM7IOA | LED14 | | | | TM7IOA:Timer 7 input/output | LED14:LED drive 14 |
| | √ | - | √ | - | TSIN6 | | | | | TSIN6:Touch sensor input 6 | |
| PA7 | √ | √ | √ | √ | AN7 | KEY7 | in/out | PADIR7 | PAPLU7 | AN7:Analog 7 input | KEY7:Key interrupt 7 |
| | √ | √ | √ | √ | LED15 | | | | | LED15:LED drive 15 | |
| | √ | - | √ | - | TSIN7 | | | | | TSIN7:Touch sensor input 7 | |

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## 1.3.3　　Pin Functions

Table remarks　　-: Without function

| Pins | MN101EF A6/A1 | | MN101EF A5/A0 | | I/O | Function | Description |
|---|---|---|---|---|---|---|---|
| | 48pin TQFP | 44pin QFP | 32pin SSOP | 32pin TQFP | | | |
| VDD5 | 5 | 5 | 6 | 3 | - | Power connect pins | Apply 4.0 V to 5.5 V to VDD5 and 0 V to VSS connect 0.1 μF + 1 μF or larger bypass capacitor for internal power stabilization. |
| VSS | 12 | 11 | 12 | 9 | - | | |
| VDD18 | 7 | 7 | 8 | 5 | - | Internal power output pin | This pin is output 1.8 V from internal power circuit. Don't use the power supply to external device. For internal power circuit output sta-bility, connect at least 0.1 μF + 1 μF one bypass capacitor between VDD18 and VSS. |
| OSC1 | 11 | 10 | 11 | 8 | Input | High speed operation clock input pin | Connect these oscillation pins to ceramic or crystal ocsillators for high-frequency clock operation. |
| OSC2 | 10 | 9 | 10 | 7 | Output | High speed operation clock output pin | If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using STOP mode. |
| NRST | 16 | 15 | 16 | 13 | I/O | Reset pins [Active low] | This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset inter-rupt. If a capacitor is to be inserted between NRST and VSS, it is recom-mended that a discharge diode be placed between NRST and VDD5. |
| ATRST | 6 | 6 | 7 | 4 | Input | Auto reset setting pin | Input "High" to enable auto reset function and "Low" to disable this function |
| P00 | 18 | 16 | 17 | 14 | I/O | I/O port 0 | 8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistor is disabled (high impedance). |
| P01 | 19 | 17 | 18 | 15 | | | |
| P02 | 20 | 18 | 19 | 16 | | | |
| P03 | 21 | 19 | 20 | 17 | | | |
| P04 | 22 | 20 | 21 | 18 | | | |
| P05 | 23 | 21 | 22 | 19 | | | |
| P06 | 24 | 22 | 23 | 20 | | | |
| P07 | 25 | 23 | 24 | 21 | | | |
| P20 | 26 | 24 | 25 | 22 | I/O | I/O port 2 | 7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P2DIR register. A pull-up resistor for each bit can be selected individually by P2PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance) |
| P21 | 27 | 25 | 26 | 23 | | | |
| P22 | 28 | 26 | 27 | 24 | | | |
| P23 | 29 | 27 | 28 | 25 | | | |
| P24 | 30 | 28 | - | - | | | |
| P25 | 11 | 10 | 11 | 8 | | | |
| P26 | 10 | 9 | 10 | 7 | | | |
| P27 | 16 | 15 | 16 | 13 | Input | Input port 2 | P27 has an N-channel open-drain configuration. |
| P30 | 13 | 12 | 13 | 10 | I/O | I/O port 3 | 7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P3DIR register. A pull-up resistor for each bit can be selected individually by P3PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance). |
| P31 | 14 | 13 | 14 | 11 | | | |
| P32 | 31 | 29 | - | - | | | |
| P33 | 32 | 30 | - | - | | | |
| P34 | 33 | 31 | - | - | | | |
| P35 | 34 | 32 | - | - | | | |
| P36 | 35 | 33 | - | - | | | |
| P40 | 36 | 34 | - | - | I/O | I/O port 4 | 6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by P4PLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance). |
| P41 | 37 | 35 | - | - | | | |
| P42 | 40 | 36 | - | - | | | |
| P43 | 41 | 37 | - | - | | | |
| P44 | 42 | 38 | - | - | | | |
| P45 | 43 | 39 | - | - | | | |

## Panasonic

Table remarks    -: Without function

| Pins | MN101EF A6/A1 | | MN101EF A5/A0 | | I/O | Function | Description |
|------|------|------|------|------|-----|----------|-------------|
| | 48pin TQFP | 44pin QFP | 32pin SSOP | 32pin TQFP | | | |
| PA0 | 44 | 40 | 29 | 26 | I/O | I/O port 0 | 8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistor is disabled (high impedance). |
| PA1 | 45 | 41 | 30 | 27 | | | |
| PA2 | 46 | 42 | 31 | 28 | | | |
| PA3 | 47 | 43 | 32 | 29 | | | |
| PA4 | 48 | 44 | 1 | 30 | | | |
| PA5 | 1 | 1 | 2 | 31 | | | |
| PA6 | 2 | 2 | 3 | 32 | | | |
| PA7 | 3 | 3 | 4 | 1 | | | |
| SBO0A | 47 | 43 | 32 | 29 | Output | Serial interface transmission data output pins | Transmission data output pins for serial interface 0,1,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLU and PAPLU registers. Select output mode in P0DIR, P2DIR, P3DIR and PADIR registers and set serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used. |
| SBO0B | 29 | 27 | 28 | 25 | | | |
| SBO1 | 33 | 31 | - | - | | | |
| SBO4 | 24 | 22 | 23 | 20 | | | |
| SBI0A | 46 | 42 | 31 | 28 | Input | Serial interface reception data input pins | Reception data input pins for serial interface 0,1,4. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLUand PAPLU registers. Select the output mode in P0DIR, P2DIR, P3DIR and PADIR registers and select serial data input mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used. |
| SBI0B | 28 | 26 | 27 | 24 | | | |
| SBI1 | 34 | 32 | - | - | | | |
| SBI4 | 23 | 21 | 22 | 19 | | | |
| SBT0A | 45 | 41 | 30 | 27 | I/O | Serial interface Clock I/O pins | Clock I/O pins for serial interface 0,1,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLU and PAPLU registers. Select clock I/O in P0DIR, P2DIR, P3DIR and PADIR registers and serial mode register 1 (SC0MD1, SC1MD1, SC4MD1) with the communication mode. These can be used as normal I/O pins when serial interface is not used. |
| SBT0B | 27 | 25 | 26 | 23 | | | |
| SBT1 | 35 | 33 | - | - | | | |
| SBT4 | 25 | 23 | 24 | 21 | | | |
| TXD0A | 47 | 43 | 32 | 29 | Output | UART transmission data output pins | In serial interface 0,1 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or Nch open-drain can be selected in P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected by P2PLU, P3PLU and PAPLU registers. Select the output mode in P2DIR, P3DIR and PADIR registers and select serial data output mode in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when serial interface is not used. |
| TXD0B | 29 | 27 | 28 | 25 | | | |
| TXD1 | 33 | 31 | - | - | | | |
| RXD0A | 46 | 42 | 31 | 28 | Input | UART reception data input pins | In serial interface 0,1 in UART mode, this pin is configured as the reception data input pin. Pull-up resistor can be selected in P2PLU, P3PLU and PAPLU registers. Select the input mode in P2DIR, P3DIR and PADIR registers and select serial input in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when serial interface is not used. |
| RXD0 | 28 | 26 | 27 | 24 | | | |
| RXD1 | 34 | 32 | - | - | | | |
| SDA4 | 24 | 22 | 23 | 20 | I/O | IIC data I/O pins | In serial interface 4 in IIC mode, this pin is configured as the data I/O pin. For the output configuration, select Nch open-drain in P0ODC register and set pull-up resistor in P0PLU register. Select the output mode in P0DIR register and select serial data I/O mode by serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used. |
| SCL4 | 25 | 23 | 24 | 21 | I/O | IIC clock I/O pins | In serial interface 4 in IIC mode, this pin is configured as the clock I/O pin. For the output configuration, select Nch open-drain in P0ODC register and set pull-up resistor by P0PLU register. Select the output mode at P0DIR register and select serial clock I/O mode in serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used |

# Panasonic

Table remarks    -: Without function

| Pins | MN101EF A6/A1 | | MN101EF A5/A0 | | I/O | Function | Description |
|---|---|---|---|---|---|---|---|
| | 48pin TQFP | 44pin QFP | 32pin SSOP | 32pin TQFP | | | |
| TM0IOA | 48 | 44 | 1 | 30 | I/O | Timer I/O pins | Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 2. To use this pin as event clock input, configure it as input by P0DIR register, P3DIR register, P4DIR register and PADIR register. In the input mode, pull-up resistor can be selected in P0PLU, P3PLU, P4PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD, P3OMD, P4OMD and PAOMD registers, and set to the output mode in P0DIR, P3DIR, P4DIR and PADIR registers. These can be used as normal I/O pins when Timer I/O pin is not used. |
| TM0IOB | 22 | 20 | 21 | 18 | | | |
| TM0IOC | 36 | 34 | - | - | | | |
| TM1IOA | 1 | 1 | 2 | 31 | | | |
| TM1IOB | 21 | 19 | 20 | 17 | | | |
| TM1IOC | 37 | 35 | - | - | | | |
| TM2IOA | 34 | 32 | - | - | | | |
| TM2IOB | 20 | 18 | 19 | 16 | | | |
| TM2IOC | 40 | 36 | - | - | | | |
| BUZZER | 31 | 29 | - | - | Output | Buzzer output pins | Piezoelectric buzzer driving pin. Buzzer output is available to Port 3. The driving frequency can be set in DLYCTR register. In order to select Buzzer output to Port 3, select the special function pin in P3OMD register, and set P3DIR register to the output mode. At the same time, select Buzzer output in oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when Buzzer output is not used. |
| NBUZZER | 32 | 30 | - | - | | | |
| TM7IOA | 2 | 2 | 2 | 32 | I/O | Timer I/O pins | Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 9. To use this pin as event clock input, configure it as input with P0DIR, P4DIR and PADIR registers. In the input mode, pull-up resistor can be selected by P0PLU, P4PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD, P4OMD and PAOMD registers, and set to the output mode in P0DIR, P4DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins. |
| TM7IOB | 19 | 17 | 18 | 15 | | | |
| TM7IOC | 41 | 37 | - | - | | | |
| TM9IOA | 18 | 16 | 17 | 14 | | | |
| TM9IOC | 42 | 38 | - | - | | | |
| TM9OD0 | 18 | 16 | 17 | 14 | Output | Timer PWM output | PWM signal output pin for 16-bit timer 9. Select the special function pin in P0OMD register, and set to the output mode in P0DIR register. These can be used as normal I/O pins when not used as timer I/O pins. |
| TM9OD1 | 19 | 17 | 18 | 15 | | | |
| TM9OD2 | 20 | 18 | 19 | 16 | | | |
| TM9OD3 | 21 | 19 | 20 | 17 | | | |
| TM9OD4 | 22 | 20 | 21 | 18 | | | |
| TM9OD5 | 23 | 21 | 22 | 19 | | | |
| VREF+ | 4 | 4 | 5 | 2 | - | A/D reference voltage input pin | Reference power supply pin for A/D converter. Normally, the values of $V_{REF+} = V_{DD5}$ is used. |
| AN0 | 44 | 40 | 29 | 26 | Input | Analog input pins | Analog input pins for 12-channel, 10-bit A/D converter. Select the analog input by PAIMD register. When not used for analog input, these pins can be used as normal input pins. |
| AN1 | 45 | 41 | 30 | 27 | | | |
| AN2 | 46 | 42 | 31 | 28 | | | |
| AN3 | 47 | 43 | 32 | 29 | | | |
| AN4 | 48 | 44 | 1 | 30 | | | |
| AN5 | 1 | 1 | 2 | 31 | | | |
| AN6 | 2 | 2 | 3 | 32 | | | |
| AN7 | 3 | 3 | 4 | 1 | | | |
| AN8 | 43 | 39 | - | - | | | |
| AN9 | 42 | 38 | - | - | | | |
| AN10 | 41 | 37 | - | - | | | |
| AN11 | 40 | 36 | - | - | | | |
| IRQ0 | 26 | 24 | 25 | 22 | Input | External interrupt | External interrupt input pins. Select the external interrupt input enable by IRQCNT register. The valid edge for IRQ0 to 4 can be selected with IRQnICR register. IRQ2 to 4 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins. |
| IRQ1 | 27 | 25 | 26 | 23 | | | |
| IRQ2 | 28 | 26 | 27 | 24 | | | |
| IRQ3 | 29 | 27 | 28 | 25 | | | |
| IRQ4A | 30 | 28 | - | - | | | |
| IRQ4B | 44 | 40 | 29 | 26 | | | |

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Table remarks    -: Without function

| Pins | MN101EF A6/A1 | | MN101EF A5/A0 | | I/O | Function | Description |
|---|---|---|---|---|---|---|---|
| | 48pin TQFP | 44pin QFP | 32pin SSOP | 32pin TQFP | | | |
| KEY0 | 44 | 40 | 29 | 26 | Input | Key interrupt input pins | Input pins for KEY interrupt based on OR condition result of pin inputs. These can be set to key input pins by 1-bit with KEY interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins. |
| KEY1 | 45 | 41 | 30 | 27 | | | |
| KEY2 | 46 | 42 | 31 | 28 | | | |
| KEY3 | 47 | 43 | 32 | 29 | | | |
| KEY4 | 48 | 44 | 1 | 30 | | | |
| KEY5 | 1 | 1 | 2 | 31 | | | |
| KEY6 | 2 | 2 | 3 | 32 | | | |
| KEY7 | 3 | 3 | 4 | 1 | | | |
| LED0 | 18 | 16 | 17 | 14 | Output | LED drive pins | Large current output pins. Select the large current output by P0LED and PALED registers. When not used for LED output, these pins can be used as normal I/O pins. |
| LED1 | 19 | 17 | 18 | 15 | | | |
| LED2 | 20 | 18 | 19 | 16 | | | |
| LED3 | 21 | 19 | 20 | 17 | | | |
| LED4 | 22 | 20 | 21 | 18 | | | |
| LED5 | 23 | 21 | 22 | 19 | | | |
| LED6 | 24 | 22 | 23 | 20 | | | |
| LED7 | 25 | 23 | 24 | 21 | | | |
| LED8 | 44 | 40 | 29 | 26 | | | |
| LED9 | 45 | 41 | 30 | 27 | | | |
| LED10 | 46 | 42 | 31 | 28 | | | |
| LED11 | 47 | 43 | 32 | 29 | | | |
| LED12 | 48 | 44 | 1 | 30 | | | |
| LED13 | 1 | 1 | 2 | 31 | | | |
| LED14 | 2 | 2 | 3 | 32 | | | |
| LED15 | 3 | 3 | 4 | 1 | | | |
| DMOD | 9 | 8 | 9 | 6 | Input | Mode switch input pins | Set always to $V_{DD5}$. |
| MMOD | 15 | 14 | 15 | 12 | Input | ROM area switch input pins at start | Set always to $V_{SS}$. |
| TSIN0 | 44 | 40 | 29 | 26 | Input | Touch sensor input pins These pins are not equipped in MN101EFA1 and MN101EFA0. | Input pins for Touch Sensor Timer of 8 channels. Set "Used" to corresponding channel by TSTCHSEL register. This setup is available regardless of the setting of port control registers. These can be used as normal I/O pins when Touch Sensor Timer is not used. |
| TSIN1 | 45 | 41 | 30 | 27 | | | |
| TSIN2 | 46 | 42 | 31 | 28 | | | |
| TSIN3 | 47 | 43 | 32 | 29 | | | |
| TSIN4 | 48 | 44 | 1 | 30 | | | |
| TSIN5 | 1 | 1 | 2 | 31 | | | |
| TSIN6 | 2 | 2 | 3 | 32 | | | |
| TSIN7 | 3 | 3 | 4 | 1 | | | |
| TSRC | 36 | 34 | 28 | 25 | Input | Touch sensor resistor connect pins. These pins are not equipped in MN101EFA1 and MN101EFA0. | These are used in the following cases. 1. External resistor connection for Touch Sensor Timer  Set both TSMD and RSMD of TSTMD register to "1". 2. The capacitor/resistor connection for Touch Sensor using A/D converter  Set TSADCNT register. This setup is available regardless of the setting of port control registers. These can be used as normal I/O pins when Touch Sensor Timer is not used. |
| TSOP | 37 | 35 | 27 | 24 | Output | | |

For the MMOD setup in rewriting the flash memory, refer to [Chapter 16 16.4 User Mode Microcontroller Rewriting], [Chapter 16 16.5 BOOT Mode Microcontroller Rewriting], [Chapter 16 16.6 Appendix].

## Panasonic

# 1.4   Block Diagram

## 1.4.1   Block Diagram
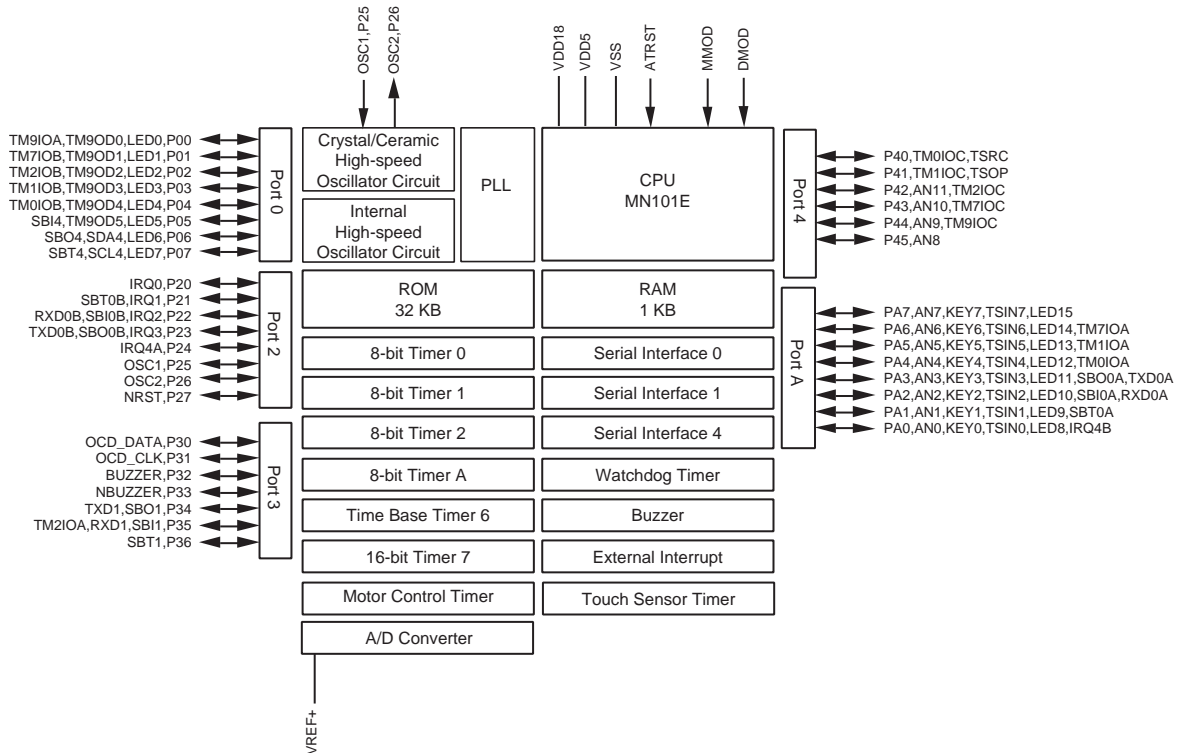


Figure:1.4.1  Block Diagram

* Varies depending on models.
  Refer to [Chapter 1 1.1.2 Product Summary] and [Chapter 1 1.3.3 Pin Functions].

# Panasonic

# 1.5   Electrical Characteristics

This LSI manual describes standard specifications.

When using this LSI, consult our sales offices for the product specifications.

| Structure | CMOS integrated circuit |
|---|---|
| Application | General-purpose |
| Function | CMOS 8-bit single chip microcomputer |

## Panasonic

### 1.5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings  *2 *3 *4                                                                    $V_{SS} = 0$ V

| | Parameter | | | Symbol | Rating | Unit |
|---|---|---|---|---|---|---|
| A1 | Power supply voltage | | | $V_{DD5}$ | -0.3 to +7.0 | V |
| A2 | Power supply voltage | | | $V_{DD18}$ | -0.3 to +2.5 | |
| A3 | Input pin voltage | | | $V_I$ | -0.3 to $V_{DD5}$ +0.3 (upper limit: 7.0) | |
| A4 | Output pin voltage | | | $V_O$ | -0.3 to $V_{DD5}$ +0.3 (upper limit: 7.0) | |
| A5 | I/O pin voltage | | | $V_{IO1}$ | -0.3 to $V_{DD5}$ +0.3 (upper limit: 7.0) | |
| A6 | Peak output current | LED output | | $I_{OL1}$ (peak) | 30 | mA |
| A7 | | Other than LED output | | $I_{OL2}$ (peak) | 20 | |
| A8 | | All pins | | $I_{OH}$ (peak) | -10 | |
| A9 | Average output current  *1 | LED output | | $I_{OL1}$ (avg) | 20 | |
| A10 | | Other than LED output | | $I_{OL2}$ (avg) | 15 | |
| A11 | | All pins | | $I_{OH}$ (avg) | -5 | |
| A12 | Power dissipation | MN101EF A6/A1 | 48pin TQFP | $P_{D1}$ | 300 | mW |
| A13 | | | 44pin QFP | $P_{D2}$ | 400 | |
| A14 | | MN101EF A5/A0 | 32pin SSOP | $P_{D3}$ | 300 | |
| A15 | | | 32pin TQFP | $P_{D4}$ | 400 | |
| A16 | Operating ambient temperature | | | $T_{opr}$ | -40 to +85 | °C |
| A17 | Storage temperature | | | $T_{STG}$ | -55 to +125 | |

*1    Applied to any 100 ms period.

*2    Connect at least one bypass capacitor of 0.1 µF + 1.0 µF or larger between VDD5 pin and GND for the internal power voltage stabilization.

*3    Connect appropriate capacitor about 0.1 µF + 1.0 µF between VDD18 pin and VSS pin, near the microcontroller according to the Figure:1.5.1 shown below for the internal power supply stabilization.
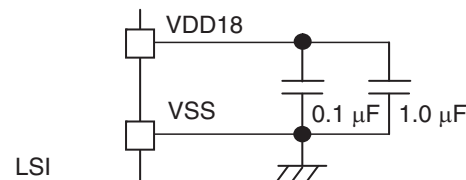


Figure:1.5.1  Capacitor Connection between VDD18 and VSS Pins

*4    The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

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## 1.5.2    Operating Conditions

$V_{SS}$ = 0 V

B. Operating Conditions

Ta = -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Power supply voltage *5 | | | | | | | |
| B1 | Power supply voltage | $V_{DD1}$ | fs ≤ 20 MHz | 4.0 | | 5.5 | V |
| B2 | RAM retention power supply voltage | $V_{DD8}$ | During STOP mode | 2.2 | | 5.5 | |
| Operating speed  *6 | | | | | | | |
| B3 | Instruction execution time  fs | $t_{c1}$ | $V_{DD5}$ = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is "1".) | 0.05 | | | μs |
| B4 | | $t_{c2}$ | $V_{DD5}$ = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is "0".) | 0.10 | | | |

*5    fs: Machine clock frequency

*6    tc1 to 2 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscil-
        lations multiplied by PLL.

External Oscillator Figure:1.5.2

| | Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| B5 | Frequency | $f_{hosc1}$ | $V_{DD5}$ is within the specified operating power supply voltage range. (Refer to the ratings of B1 to B2 for the operating supply voltage range) | 2.0 | | 10 | MHz |
| B6 | Internal feedback resistor | $R_{f10}$ | $V_{DD5}$ = 5.0 V | | 980 | | kΩ |
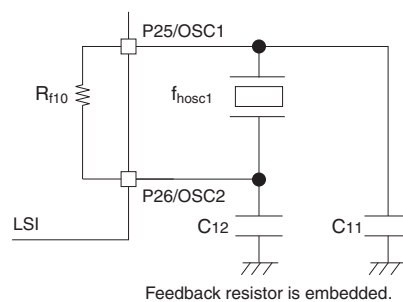


Figure:1.5.2  External Oscillator

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed
depending on the value of capacitor. For external capacity value, please consult the oscillator
manufacturer and perform matching tests enough for determining appropriate values.

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$V_{DD5}$ = 4.0 V to 5.5 V
$V_{SS}$ = 0 V
Ta = -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |

External clock input 1 OSC1 (OSC2 is unconnected)

| | Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| B7 | Clock frequency | $f_{hosc2}$ | | 2 | | 10.0 | MHz |
| B8 | High-level pulse width *7 | $t_{wh1}$ | Figure:1.5.3 | 45 | | | ns |
| B9 | Low-level pulse width *7 | $t_{wl1}$ | | 45 | | | |
| B10 | Rising time | $t_{wr1}$ | Figure:1.5.3 | 0 | | 5.0 | |
| B11 | Falling time | $t_{wf1}$ | | 0 | | 5.0 | |

*7    The clock duty ratio should be 45 % to 55 %
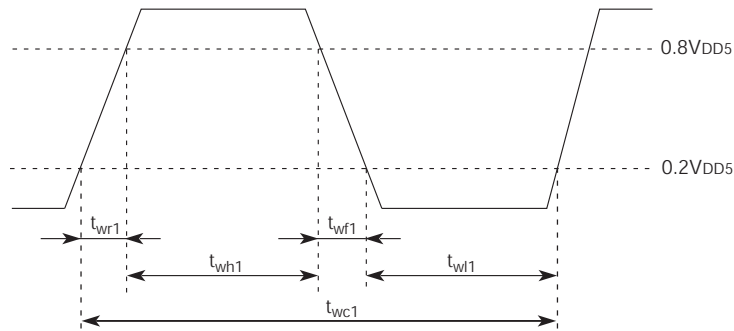


Figure:1.5.3  OSC1 Timing Chart

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## 1.5.3　DC Characteristics

C. DC Characteristics

$V_{SS}$ = 0 V
Ta = -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Power supply current *8 | | | | | | | |
| C1 | Power supply current during operation | $I_{DD1}$ | fosc=10 MHz [Double-speed mode: fs=fosc] $V_{DD5}$=5 V (PLL is not used) *9 | | 5 | 14 | mA |
| C2 | | $I_{DD2}$ | fosc=10 MHz [Multiplied by 2, Divided by 2: fs=fosc] $V_{DD5}$=5 V (PLL is used) *9 | | 6 | 18 | |
| C3 | | $I_{DD3}$ | fosc=10 MHz [Multiplied by 2: fs=20 MHz] $V_{DD5}$=5 V (PLL is used) *9 | | 9 | 20 | |
| C4 | | $I_{DD4}$ | frc=16 MHz [Double-speed mode: fs=16 MHz] $V_{DD5}$=5 V (PLL is used) *9 | | 6 | 15 | |
| C5 | Power supply current during STOP mode | $I_{DD5}$ | $V_{DD5}$=5 V Ta = -40 °C to +85 °C | | 145 | 245 | μA |

*8　Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation $I_{DD1}$ to $I_{DD4}$;
1. Set all I/O pins to input mode,
2. Set the CPU mode to "NORMAL mode",
3. Fix pin MMOD to $V_{SS}$ level and input pins to $V_{DD5}$ level
4. Input the rectangular wave of 10 MHz(4 MHz) with amplitude of $V_{DD5}$ and $V_{SS}$, from pin OSC1.

To measure the power supply current during STOP mode $I_{DD5}$;
1. Set the CPU mode to "STOP mode",
2. Fix pin MMOD to $V_{SS}$ level and input pin to $V_{DD5}$ level
3. Open pin OSC1.

*9　When ROMHND of HANDSHAKE register is set to "1"

$V_{DD5}$ = 4.0 V to 5.5 V $V_{SS}$ = 0 V

Ta = -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |

Input pin 1  ATRST, MMOD

| | Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| C10 | Input high voltage | $V_{IH1}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C11 | Input low voltage | $V_{IL1}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C12 | Input leakage current | $I_{LK1}$ | $V_{IN}$ = 0 V to $V_{DD5}$ | | | ± 2 | μA |

Input pin 2  P27/NRST

| | Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| C13 | Input high voltage | $V_{IH2}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C14 | Input low voltage | $V_{IL2}$ | | 0 | | 0.15 $V_{DD5}$ | |
| C15 | Pull-up resistor | $R_{RH1}$ | $V_{DD5}$=5 V, $V_{IN}$= $V_{SS}$ | 10 | 50 | 100 | kΩ |

I/O pin 3 P00 to P07

| | Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| C16 | Input high voltage 2 | $V_{IH3}$ | | 0.54 $V_{DD5}$ | | $V_{DD5}$ | V |
| C17 | Input low voltage | $V_{IL3}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C18 | Input leakage current | $I_{LK2}$ | $V_{IN}$=0 V to $V_{DD5}$ | | | ± 2 | μA |
| C19 | Pull-up resistor | $R_{RH2}$ | $V_{DD5}$=5 V, $V_{IN}$= $V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |
| C20 | Output high voltage | $V_{OH1}$ | $V_{DD5}$=5.0 V, $I_{OH}$=-0.5 mA | 4.5 | | | |
| C21 | Output low voltage 1 | $V_{OL1}$ | $V_{DD5}$=5.0 V, $I_{OL}$=1.0 mA LED output OFF | | | 0.5 | V |
| C22 | Output low voltage 2 | $V_{OL2}$ | $V_{DD5}$=5.0 V, $I_{OL}$=15.0 mA LED output ON | | | 1.0 | |

I/O pin 4 P20, P21

| | Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| C23 | Input high voltage 2 | $V_{IH4}$ | | 0.54 $V_{DD5}$ | | $V_{DD5}$ | V |
| C24 | Input low voltage | $V_{IL4}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C25 | Input leakage current | $I_{LK3}$ | $V_{IN}$=0 V to $V_{DD5}$ | | | ± 2 | μA |
| C26 | Pull-up resistor | $R_{RH3}$ | $V_{DD5}$=5 V, $V_{IN}$=$V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |
| C27 | Output high voltage | $V_{OH2}$ | $V_{DD5}$=5.0 V, $I_{OH}$=-0.5 mA | 4.5 | | | V |
| C28 | Output low voltage | $V_{OL3}$ | $V_{DD5}$=5.0 V, $I_{OL}$=1.0 mA | | | 0.5 | |

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$V_{DD5}$ = 4.0 V to 5.5 V $V_{SS}$ = 0 V
Ta = -40 °C to +85 °C

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| I/O pin 5 P22 to P24, P25 to P26 *10 P30 to P31, P32 to P36 | | | | | | | |
| C29 | Input high voltage | $V_{IH5}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C30 | Input low voltage | $V_{IL5}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C31 | Input leakage current | $I_{LK4}$ | $V_{IN}$=0 V to $V_{DD5}$ | | | ± 2 | μA |
| C32 | Pull-up resistor | $R_{RH4}$ | $V_{DD5}$=5.0 V, $V_{IN}$=$V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |
| C33 | Output high voltage | $V_{OH3}$ | $V_{DD5}$=5.0 V, $I_{OH}$=-0.5 mA | 4.5 | | | V |
| C34 | Output low voltage | $V_{OL4}$ | $V_{DD5}$=5.0 V, $I_{OL}$=1.0 mA | | | 0.5 | |
| I/O pin 6 PA0 to PA7 | | | | | | | |
| C35 | Input high voltage | $V_{IH6}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C36 | Input low voltage | $V_{IL6}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C37 | Input leakage current | $I_{LK5}$ | $V_{IN}$=0 V to $V_{DD5}$ | | | ± 2 | μA |
| C38 | Pull-up resistor | $R_{RH5}$ | $V_{DD5}$=5.0 V, $V_{IN}$=$V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |
| C39 | Output high voltage | $V_{OH4}$ | $V_{DD5}$=5.0 V, $I_{OH}$=-0.5 mA | 4.5 | | | V |
| C40 | Output low voltage 1 | $V_{OL5}$ | $V_{DD5}$=5.0 V, $I_{OL}$=1.0 mA LED output OFF | | | 0.5 | |
| C41 | Output low voltage 2 | $V_{OL6}$ | $V_{DD5}$=5.0 V, $I_{OL}$=15.0 mA LED output ON | | | 1.0 | |
| I/O pin 7 P40 to P45 | | | | | | | |
| C42 | Input high voltage | $V_{IH7}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C43 | Input low voltage | $V_{IL7}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C44 | Input leakage current | $I_{LK5}$ | $V_{IN}$=0 V to $V_{DD5}$ | | | ± 2 | μA |
| C45 | Pull-up resistor | $R_{RH6}$ | $V_{DD5}$=5.0 V, $V_{IN}$=$V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |
| C46 | Pull-down resistor | $R_{RL1}$ | $V_{DD5}$=5.0 V, $V_{IN}$=$V_{DD5}$ Pull-down resistor ON | 10 | 50 | 100 | |
| C47 | Output high voltage | $V_{OH5}$ | $V_{DD5}$=5.0 V, $I_{OH}$=-0.5 mA | 4.5 | | | V |
| C48 | Output low voltage | $V_{OL7}$ | $V_{DD5}$=5.0 V, $I_{OL}$=1.0 mA | | | 0.5 | |
| Input pin 8 DMOD *11 | | | | | | | |
| C49 | Input high voltage | $V_{IH8}$ | | 0.8 $V_{DD5}$ | | $V_{DD5}$ | V |
| C50 | Input low voltage | $V_{IL8}$ | | 0 | | 0.2 $V_{DD5}$ | |
| C51 | Pull-up resistor | $R_{RH8}$ | $V_{DD5}$=5.0 V, $V_{IN}$=$V_{SS}$ Pull-up resistor ON | 10 | 50 | 100 | kΩ |

*10 These are not used for oscillation pins.

*11 Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using In-Circuit Emulator, connect pull-up resistor to DMOD on the target board.

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## 1.5.4　A/D Converter Characteristics

$V_{DD5}$ = 5.0 V $V_{SS}$ = 0 V
Ta = -40 °C to +85 °C

D. A/D Converter Characteristics *12

| | Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| D1 | Resolution | | | | | 10 | Bits |
| D2 | Non-linearity error 1 | | $V_{DD5}$=5.0 V, $V_{SS}$=0 V $V_{REF+}$=5.0 V $T_{AD}$=800 ns | | | ± 3 | LSB |
| D3 | Differential non-linearity error 1 | | | | | ± 3 | |
| D4 | Zero transition voltage | | $V_{DD5}$=5.0 V, $V_{SS}$=0 V $V_{REF+}$=5.0 V $T_{AD}$=800 ns | | 10 | 30 | mV |
| D5 | Full-scale transition voltage | | | 4970 | 4990 | | |
| D6 | A/D conversion time | | $T_{AD}$=800 ns | 12.93 | | | μs |
| D7 | Sampling time | | $T_{AD}$=800 ns | 1.6 | | | |
| D8 | Reference voltage | $V_{REF+}$ | $V_{REF+}$= $V_{DD5}$ | 4.0 | | $V_{DD5}$ | V |
| D9 | Analog input voltage | | | $V_{SS}$ | | $V_{REF+}$ | |
| D10 | Analog input leakage current | | Channel OFF $V_{ADIN}$=$V_{SS}$ to $V_{DD5}$ | | | ± 2 | μA |
| D11 | Reference voltage pin input leakage current | | Ladder resistance OFF $V_{SS} \leq V_{REF+} \leq V_{DD5}$ | | | ± 5 | |
| D12 | Ladder resistance | $R_{LADD}$ | $V_{DD5}$=5.0 V | 15 | 40 | 80 | kΩ |

*12　$T_{AD}$ is A/D conversion clock cycle.
The specification values of D2 to D5 are guaranteed on the condition of $V_{DD5}$=$V_{REF+}$=5 V, $V_{SS}$=0 V.

⚠ Even if A/D function is not used, $V_{REF+}$ must be set between $V_{DD5}$ and 4.0 V.

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### 1.5.5    Auto Reset Characteristics

E. Auto Reset Characteristics

| | Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Power supply voltage | | | | | | | |
| E1 | Operating supply voltage | $V_{DD7}$ | Auto reset is used | $V_{RST}$ | | 5.5 | V |
| Power supply voltage | | | | | | | |
| E2 | Power detection level | $V_{RST1}$ | At rising | 4.10 | 4.30 | 4.50 | V |
| E3 | Power detection level | $V_{RST2}$ | At falling | 4.00 | 4.20 | 4.40 | |
| E4 | Supply voltage change rate | $\Delta t / \Delta V$ | | 2 | | | ms/V |

### 1.5.6    Internal High-speed Oscillation Circuit

F. Internal High-speed Oscillation Circuit

| | Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| F1 | Internal high-speed oscillation circuit frequency | $f_{rc}$ | Ta = -40 °C to +85 °C | | 16 | | MHz |
| F2 | Temperature dependence of oscillation frequency *13 | $f_{rc3}$ | Ta = 25 °C | -5.0 | | 5.0 | % |
| | | $f_{rc4}$ | Ta = -40 °C to +85 °C | | | | |

*13   The specification values described in G are for standard application.
For special application (such as for automotive product) has different value.
When using this LSI, consult our sales offices for the product specifications.

### 1.5.7    Flash EEPROM Program Conditions

G. Flash EEPROM Program Conditions *14

| | Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| G1 | Voltage for rewriting | $V_{DDEW}$ | | 4.0 | | 5.0 | V |
| G1 | Programming guarantee number of times | $E_{MAX}$ | | | | 1000 | Time |
| G2 | Data retention period | $T_{HOLD}$ | | 20 | | | Year |

*14   The specification values described in G are for standard application.
For special application (such as for automotive product) has different value.
When using this LSI, consult our sales offices for the product specifications.

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# 1.6 Package Dimension

■ Package code: QFP044-P-1010FUnit: mm
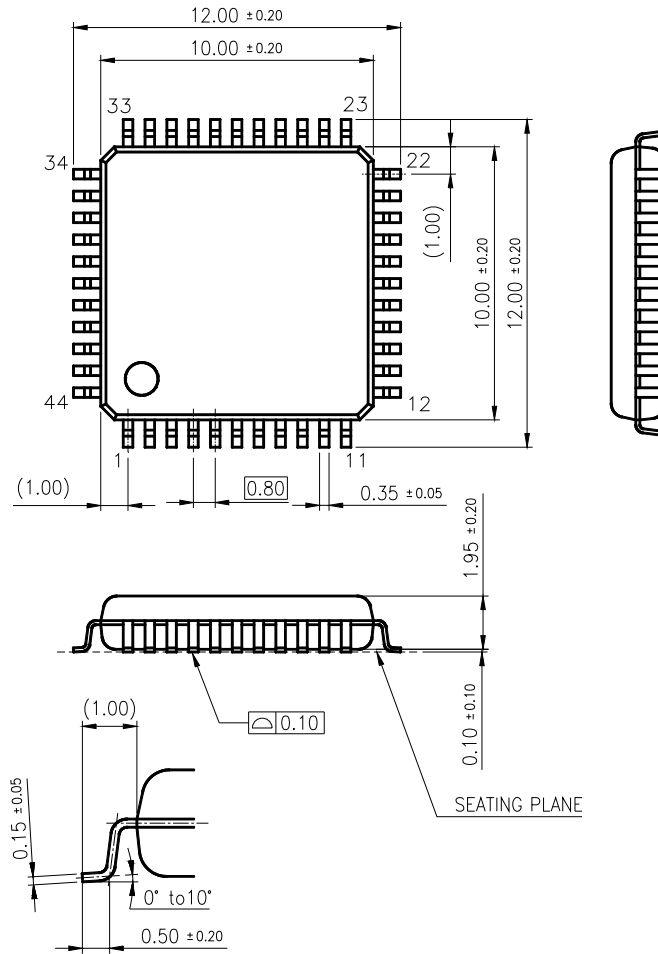


Figure:1.6.1  44-pin QFP Package Dimension

⚠ This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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■ Package code: TQFP048-P-0707BUnit: mm
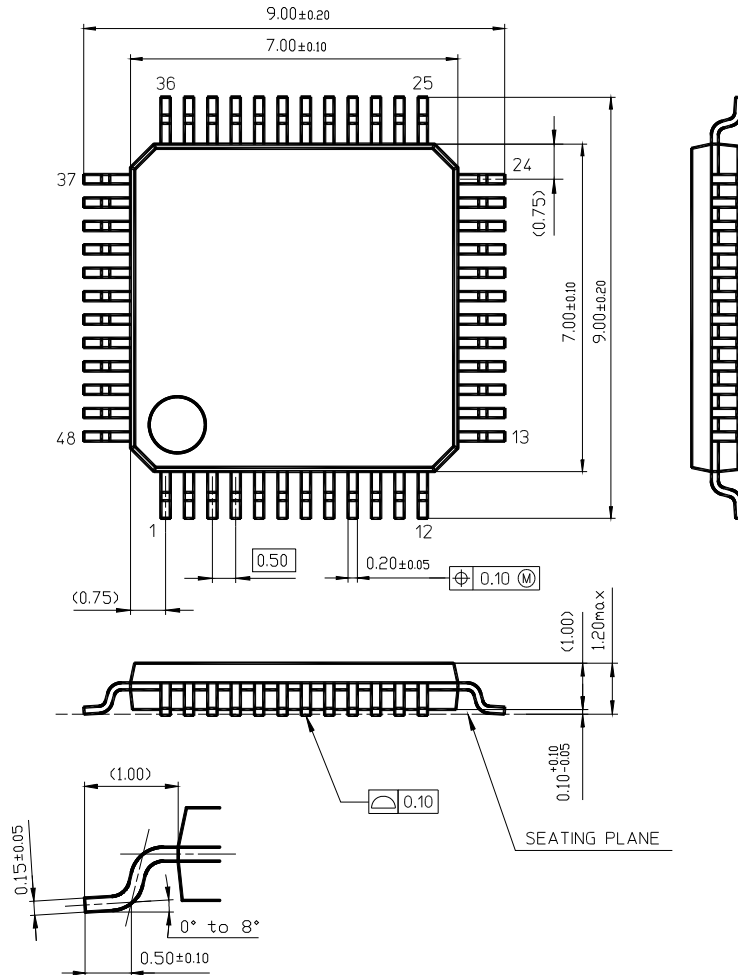


Figure:1.6.2  48-pin TQFP Package Dimension

⚠ This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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■ Package code: SSOP032-P-0300DUnit: mm
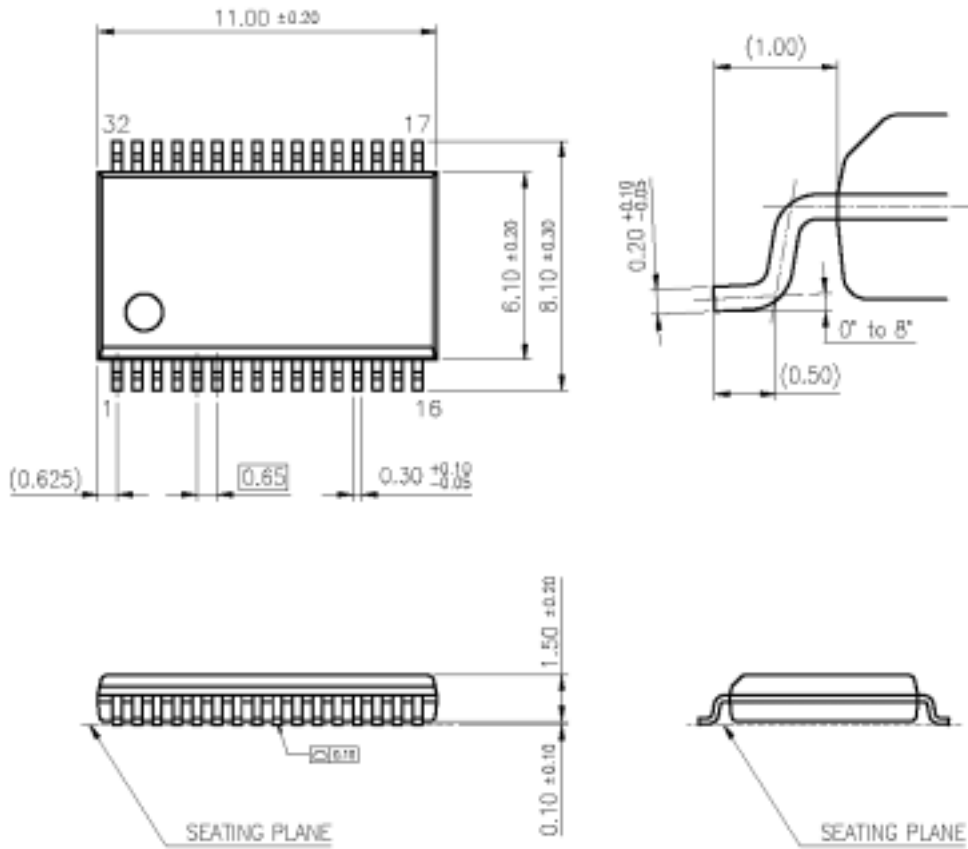


Figure:1.6.3  32-pin SSOP Package Dimension

⚠ This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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■ Package code: TQFP032-P-0707AUnit: mm
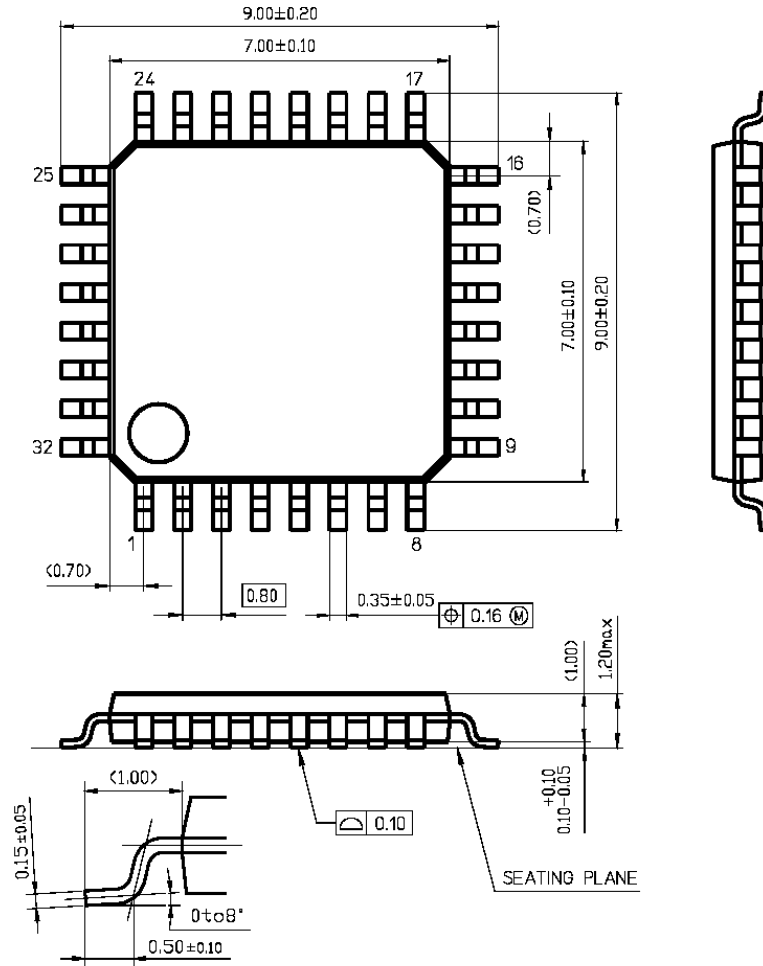


Figure:1.6.4  32-pin TQFP Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.