

MX-COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX615

Digital Line to POTS Interface

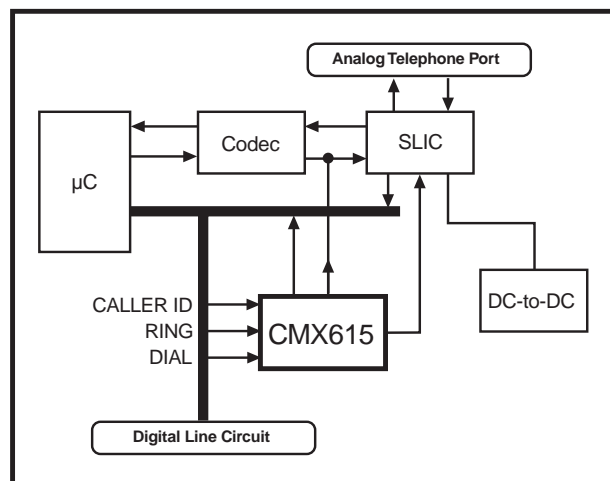
PRELIMINARY INFORMATION

Features

- Pre-Programmed Tone Generators
- Fully Integrated DTMF Encoder
- SPM Generator
- Simple Serial Control Interface
- 'Zero-Power' (1 μ A) Standby Mode
- 3.58MHz Xtal/Clock
- Bell 202 / V.23 FSK Generator
- Digital Ringing Voltage Generator

Applications

- Digital Line to POTS Interface
- Subscriber Terminal Adapters
- Wireless Local Loop
- Computer Telephony Integration
- Telephone/Radio Patch Systems
- Pair Gain Systems
- Billing/SPM Systems



The CMX615 is an integrated telecom tone generator and DTMF encoder designed for ISDN interfaces, Wireless Local Loop and Analog to Digital Telephone Conversion systems. The tone generator covers an extensive range of pre-programmed tones used in analog telephone systems (POTS). Three outputs are provided: 'Ringing signals', 'In-band tones or FSK data', and '12kHz/16kHz Metering pulses'. Simple software control facilitates the interface to a wide range of commonly used μ Cs and SLICs, enabling a comprehensive analog telephone line presentation.

The DTMF encoder generates the appropriate DTMF tones for the POTS interface. DTMF tone pairs can be encoded along with each tone singly or with other dual tone signals, such as those used in CIDCW systems and 'On Hook' signaling systems.

Other tone standards supported are: Fax and Modem 'answer' and 'originate', ITU (CCITT) 'R1' and 'R2' signals, and sufficient tones for simple melody generation. Communication to and from the host μ C is performed by a 'C-BUS' serial interface, which is compatible with common serial interfaces such as: SCI, SPI, and Microwire.

The CMX615 operates using a 2.7V to 5.5V supply and is available in the following packages: 16-pin SOIC (CMX615D4) and 16-pin PDIP (CMX615P3).

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1 Block Diagram

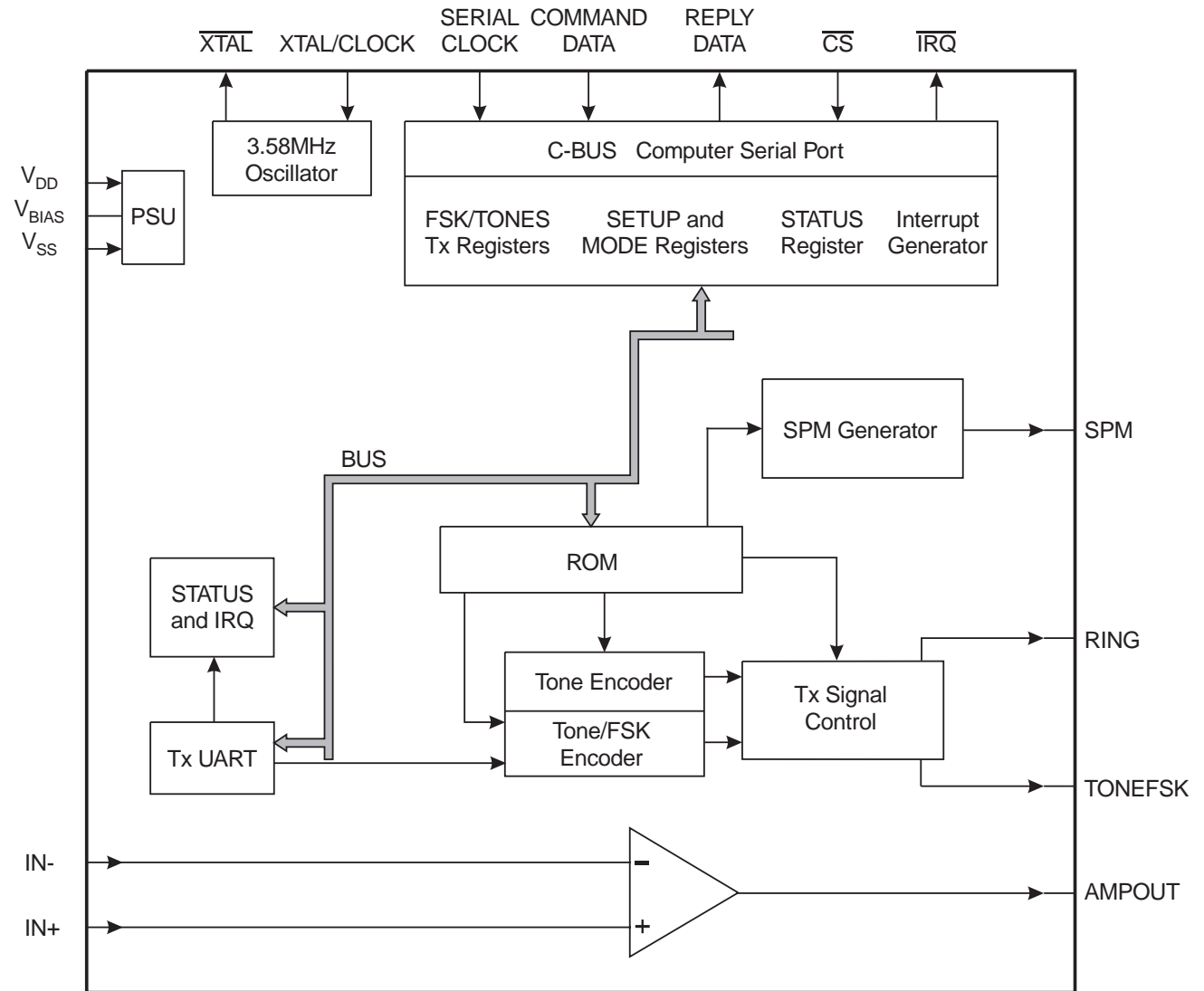


Figure 1: Block Diagram

2 Signal List

CMX615 D4/P3	Signal		Description
	Pin No.	Name	
1	$\overline{\text{XTAL}}$	output	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	input	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	SERIAL CLOCK	input	The 'C-BUS' serial clock input from the host μC . See Section 4.8
4	COMMAND DATA	input	The 'C-BUS' serial data input from the host μC .
5	REPLY DATA	tri-state	A 3-state 'C-BUS' serial data output to the host μC . This output is high impedance when not sending data to the host μC .
6	$\overline{\text{CS}}$	input	Chip Select. The 'C-BUS' transfer control input provided by the host μC .
7	$\overline{\text{IRQ}}$	output	A 'wire-ORable' output for connection to a host μC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.
8	V_{SS}	power	The negative supply rail (ground).
9	TONEFSK	output	The sinewave output of the Tones and FSK signal generators.
10	SPM	output	The sinewave output of the SPM signal generator.
11	V_{BIAS}	output	An internally generated bias voltage of $V_{\text{DD}}/2$, except when the device is in 'Zero Power' mode when V_{BIAS} will discharge to V_{SS} . It should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
12	IN+	input	The non-inverting input to the uncommitted amplifier.
13	IN-	input	The inverting input to the uncommitted amplifier.
14	AMPOUT	output	The output of the uncommitted amplifier.
15	RING	output	The squarewave output of the Ringing Signal generator.
16	V_{DD}	power	The positive supply rail. Levels within the device are proportional to this voltage. It should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

It is recommended that the printed circuit board is laid out with a ground plane in the CMX615 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} bypass capacitors.

Table 1: Signal List

3 External Components

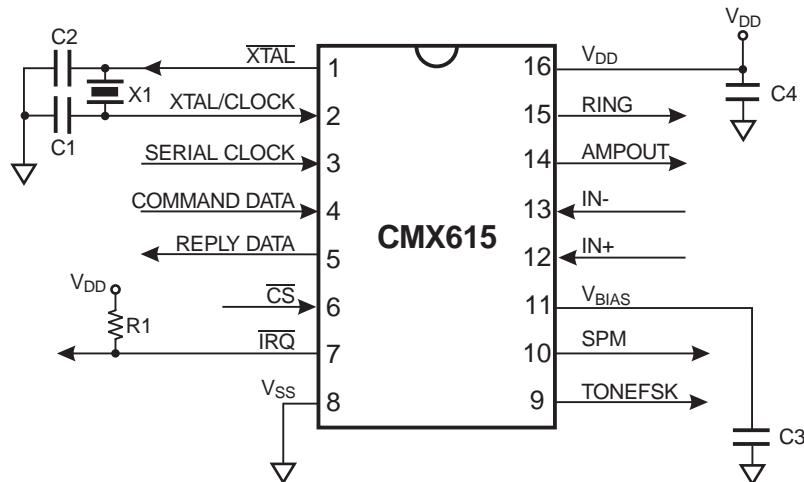


Figure 2: Recommended External Components

R1		100k Ω
C1, C2		18pF
C3, C4		1.0 μ F
X1		3.579545 MHz

Resistors $\pm 5\%$, capacitors $\pm 10\%$ unless otherwise stated.

Table 2: Recommended External Components

Recommended External Component Notes:

1. Resistors $\pm 5\%$, capacitors $\pm 10\%$ unless otherwise stated.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} , peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult your crystal manufacturer.

4 General Description

The CMX615 is a telecom tone generator and DTMF tone encoder. It has separate output ports for the three different classes of signals encoded. These include Ringing signal, In-band tones or FSK data at 1200bps, and High frequency metering pulses (SPM tones). It has a transmit level attenuator for In-band tones or FSK data and an envelope control for SPM tones. It also has an uncommitted amplifier and uses the industry standard 3.58MHz Xtal for its oscillator. These functions are controlled over a 'C-BUS' serial μ C interface, which also carries the transmit FSK data.

The CMX615 may be powersaved into 'Zero-Power' mode for minimum power consumption by issuing a 'C-BUS' RESET command. Individual functions may be powersaved by the use of bits 6 and 7 in the SETUP Register. Not powersaving the Tx Powersave (set bit 6 of the SETUP Register to '1') will take the Tx functions (tone/FSK encoding, DTMF, SPM and Ringing signal generation) out of powersave. Not powersaving the Uncommitted Amplifier (Set bit 7 of the SETUP Register to '1') will take the amplifier out of powersave. Approximately 50ms should be allowed for the Tx DC level to settle at V_{BIAS} before enabling the Tx functions (set bit 6 of the MODE Register to '1').

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the CMX615 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If the clock is supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source, which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a rise in the supply current drawn by CMX615.

4.2 Uncommitted Amplifier

This amplifier, with suitable external components, can be used for adjusting the transmit signal level (for the line hybrid).

4.3 Tone/FSK Encoder and Tone Encoder

When bit 5 of the MODE Register is set to '1' then these blocks generate FSK signals as determined by bit 0 of the SETUP Register and the Tx data bits from the UART block, as shown in the table below:

SETUP Register Bit 0	Tone/FSK Generator	FSK Signal Frequency '0' (Space)	FSK Signal Frequency '1' (Mark)
0	V23 1200bps FSK	2100Hz	1300Hz
1	Bell 202 1200bps FSK	2200Hz	1200Hz

Table 3: Tone/FSK Encoder and Tone Encoder

When bit 5 of the MODE Register is set to '0', these blocks generate single or dual tones from the range shown in Table 4, Table 5, Table 6, and Table 7 on the following pages. Bit 6 of the MODE Register is then used to enable or disable the block's output to the TX Signal Control, RING, and TONEFSK outputs. There are four tone fields addressed by bits 0 and 1 of the MODE Register.

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	252.4	0	0	0	1	* 17.1
0	0	1	0	268.7	0	0	1	0	* 20.5
0	0	1	1	285.3	0	0	1	1	* 24.9
0	1	0	0	315.5	0	1	0	0	* 34.1
0	1	0	1	330.5	0	1	0	1	* 41.0
0	1	1	0	375.2	0	1	1	0	* 51.2
0	1	1	1	404.3	0	1	1	1	-
1	0	0	0	468.0	1	0	0	0	262.9
1	0	0	1	495.8	1	0	0	1	293.6
1	0	1	0	520.6	1	0	1	0	348.2
1	0	1	1	548.0	1	0	1	1	392.6
1	1	0	0	562.8	1	1	0	0	1600
1	1	0	1	578.4	1	1	0	1	1633
1	1	1	0	595.0	1	1	1	0	1827
1	1	1	1	612.5	1	1	1	1	587.2

Table 4: Tone Field 0, MODE Register bit 1 and bit 0 = '0' and '0' respectively

NOTE: * These outputs are routed to the RING digital output instead of the TONEFSK output. Any single tone output level at TONEFSK output is 0dBm.

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	120	0	0	0	1	330
0	0	1	0	150	0	0	1	0	416
0	0	1	1	154	0	0	1	1	420
0	1	0	0	250	0	1	0	0	425
0	1	0	1	300	0	1	0	1	433
0	1	1	0	350	0	1	1	0	440
0	1	1	1	360	0	1	1	1	450
1	0	0	0	367	1	0	0	0	460
1	0	0	1	375	1	0	0	1	480
1	0	1	0	380	1	0	1	0	500
1	0	1	1	383	1	0	1	1	600
1	1	0	0	400	1	1	0	0	620
1	1	0	1	450	1	1	0	1	720
1	1	1	0	475	1	1	1	0	930
1	1	1	1	480	1	1	1	1	-

Table 5: Tone Field 1, MODE Register bit 1 and bit 0 = '0' and '1' respectively

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	700	0	0	0	1	700
0	0	1	0	900	0	0	1	0	900
0	0	1	1	1100	0	0	1	1	1100
0	1	0	0	1300	0	1	0	0	1300
0	1	0	1	1500	0	1	0	1	1500
0	1	1	0	1700	0	1	1	0	1700
0	1	1	1	-	0	1	1	1	-
1	0	0	0	950	1	0	0	0	2100
1	0	0	1	1400	1	0	0	1	2225
1	0	1	0	1800	1	0	1	0	-
1	0	1	1	2130	1	0	1	1	2750
1	1	0	0	697	1	1	0	0	1209
1	1	0	1	770	1	1	0	1	1336
1	1	1	0	852	1	1	1	0	1477
1	1	1	1	941	1	1	1	1	1633

Table 6: Tone Field 2, MODE Register bit 1 and bit 0 = '1' and '0' respectively

TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	540	0	0	0	1	540
0	0	1	0	660	0	0	1	0	660
0	0	1	1	780	0	0	1	1	780
0	1	0	0	900	0	1	0	0	900
0	1	0	1	1020	0	1	0	1	1020
0	1	1	0	1140	0	1	1	0	1140
0	1	1	1	-	0	1	1	1	-
1	0	0	0	1380	1	0	0	0	1380
1	0	0	1	1500	1	0	0	1	1500
1	0	1	0	1620	1	0	1	0	1620
1	0	1	1	1740	1	0	1	1	1740
1	1	0	0	1860	1	1	0	0	1860
1	1	0	1	1980	1	1	0	1	1980
1	1	1	0	-	1	1	1	0	-
1	1	1	1	-	1	1	1	1	-

Table 7: Tone Field 3, MODE Register bit 1 and bit 0 = '1' and '1' respectively

4.4 SPM Generator

This block operates independently and has its own output pin. It can transmit 12kHz or 16kHz and is controlled by bit 4 of the SETUP Register. Bit 7 of the MODE Register is used to enable or disable this block. The signal has a rise and fall time each of about 4.5ms. The SPM signal rises from the bias level to 0dBm in 16 steps of ≈ 2 dB magnitude, and falls from 0dBm to bias level in 16 steps of ≈ 2 dB magnitude.

4.5 Tx Signal Control

This block adjusts the amplitude of the FSK transmit signal output level, the level skew between DTMF tones, and the signal routing to the output ports.

Output signal levels are proportional to V_{DD} . The nominal output signal levels (at 0dB attenuation and $V_{DD} = 5.0V$) are:

Single Tone	0dBm
Dual Tone (per tone)	-3dBm
DTMF High Frequency Tone	-3dBm
DTMF Low Frequency Tone	-5dBm
FSK Signal	0dBm

The RING signal is digital: a square wave with amplitude of $\approx V_{DD}$ peak to peak. When the RING signal is not selected, the RING output pin is connected to V_{SS} .

The level attenuator provides for level adjustment from 0dB to -14dB in -2dB steps. The typical level is determined by bits 2 to 4 of the MODE Register as shown in Table 8.

MODE Register			Signal Level Adjustment
Bit 4	Bit 3	Bit 2	(dB)
0	0	0	0
0	0	1	-2
0	1	0	-4
0	1	1	-6
1	0	0	-8
1	0	1	-10
1	1	0	-12
1	1	1	-14

Table 8: Typical Level settings as determined by bits 2, 3, and 4 of the Mode Register

4.6 Tx UART

This block connects the μC , via the 'C-BUS' interface, to the FSK Encoder.

The block can be programmed to convert transmit data from 8-bit bytes to asynchronous data characters by adding Start and Stop bits. The transmit data is then passed to the FSK Encoder.

Data to be transmitted should be loaded by the μC into the TX DATA Register when the Tx Data Ready bit (bit 6) of the STATUS Register goes high. It will then be treated by the Tx UART block in one of two ways, depending on the setting of bit 1 of the SETUP Register:

If bit 1 of the SETUP Register is '0' (Tx Sync mode) then the 8 bits from the TX DATA Register will be transmitted sequentially at 1200bps, LSB (D0) first.

If bit 1 of the SETUP Register is '1' (Tx Async mode) then bits will be transmitted as asynchronous data characters at 1200bps according to the following format:

- One Start bit (Space)
- Eight Data bits (D0-D7) from the TX DATA Register, with the LSB (D0) transmitted first
- One Stop bit (Mark)

Failure to load the TX DATA Register with a new value when required will result in bit 7 (Tx Data Underflow) of the STATUS Register being set to '1'. If the 'Tx Async' mode of operation is selected then a continuous Mark ('1') signal will be transmitted until a new value is loaded into TX DATA. If the 'Tx Sync' mode is selected then the byte already in the TX DATA Register will be re-transmitted.

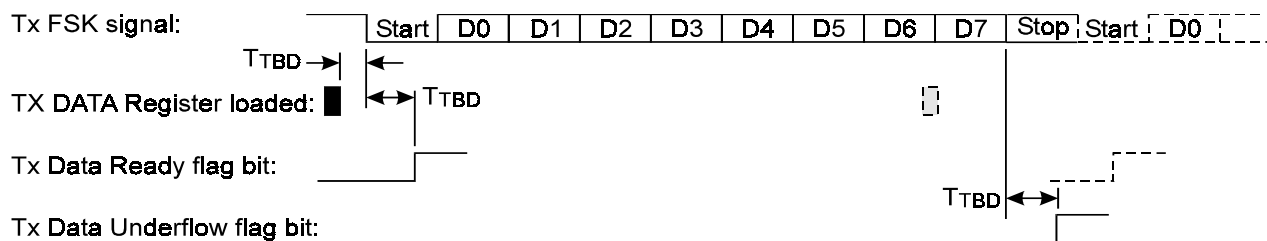


Figure 3: Transmit UART Functions (Async)

4.7 'C-BUS' Interface

This block provides for the transfer of data and control or status information between the CMX615's internal registers and the μ C over the 'C-BUS' serial bus. Each 'C-BUS' transaction consists of a single Register Address byte sent from the μ C, as illustrated in Figure 4, which may then be followed by either of:

A single data byte sent from the μ C to be written into one of the CMX615's Write Only Registers, as illustrated in Figure 5.

A single byte of data read out from one of the CMX615's Read Only Registers, as illustrated in Figure 6.

Data sent from the μ C on the Command Data (COMMAND DATA) line is clocked into the CMX615 on the rising edge of the Serial Clock (SERIAL CLOCK) input. Reply Data (REPLY DATA) sent from the CMX615 to the μ C is valid when the Serial Clock is high. The interface is compatible with the most common μ C serial interfaces such as SCI, SPI and Microwire, and may also be easily implemented with general purpose μ C I/O pins controlled by a simple software routine. See Figure 9 for detailed 'C-BUS' timing requirements.

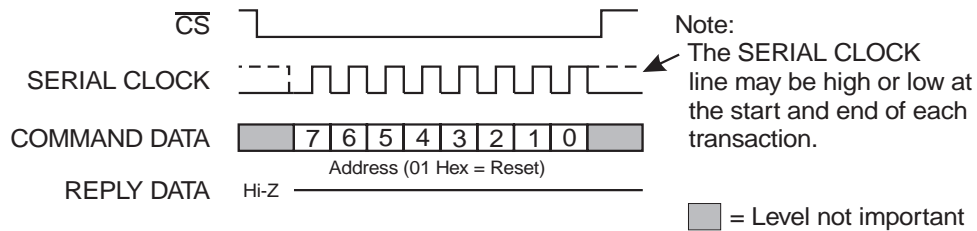


Figure 4: 'C-BUS' Transactions (Single byte from μ C)

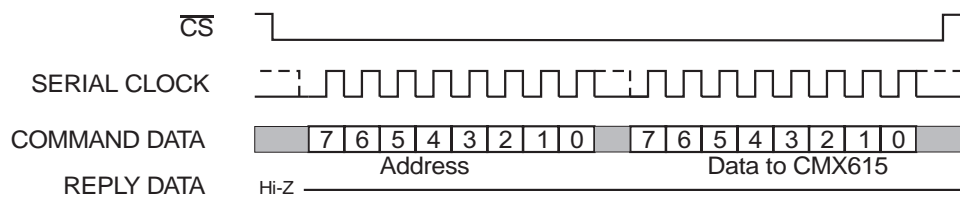


Figure 5: 'C-BUS' Transactions (One Address and one Data byte from μ C)

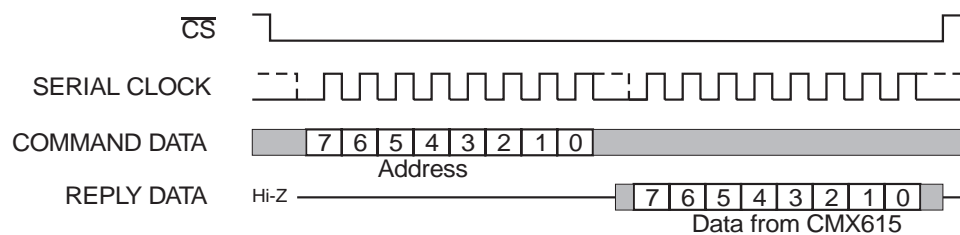


Figure 6: 'C-BUS' Transactions (One Address byte from μ C and one Reply byte from CMX615)

4.8 'C-BUS' Registers

Addr	Register	Command Data Byte (Bits 7 - 0)							
		7	6	5	4	3	2	1	0
\$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
\$D0	SETUP	Uncommitted Amplifier: 0 = Powersave 1 = Not Powersave	Tx Powersave: 0 = Powersave 1 = Not Powersave	Reserved set to 0	SPM: 0 = 12kHz 1 = 16kHz	Reserved set to 0	Reserved set to 0	FSK mode: 0 = Sync 1 = Async	FSK mode: 0 = V23 1 = Bell 202
\$D1	MODE	SPM O/P: 0 = Disable 1 = Enable	Tone/FSK: 0 = Disable 1 = Enable	Tone/FSK: 0 = Tone 1 = FSK	Tx Level: (MSB)	Tx Level: (LSB)	Tx Level: (LSB)	Tone Fields: (MSB)	Tone Fields: (LSB)
\$D3	TX DATA	D7	D6	D5	D4	D3	D2	D1	D0
\$D4	TX TONES	D7	D6	D5	D4	D3	D2	D1	D0

Table 9: Write Only Registers

Addr.	Register	Reply Data Byte (Bits 7 - 0)							
		7	6	5	4	3	2	1	0
\$DF	STATUS	FSK Mode: FSK Tx Data Underflow	FSK Mode: FSK Tx Data Ready	Reserved set to 0	Reserved set to 0	Reserved set to 0	Reserved set to 0	Reserved set to 0	Reserved set to 0

Table 10: Read Only Registers

Notes:

Accessing the RESET Register over the 'C-BUS' clears all of the bits in the SETUP, MODE, TX DATA, TX TONES and STATUS registers. This will set the device into the Zero Power mode. Note that this is a single-byte 'C-BUS' transaction consisting solely of the address byte value \$01.

If any of bits 6 or 7 of the STATUS Register is '1' then the \overline{IRQ} output will be pulled low.

Reading the STATUS Register clears the \overline{IRQ} output. Bits 6 and 7 of the STATUS Register are cleared on writing to the TX DATA Register.

5 Application Notes

When using the Tone/FSK bit (bit 6) of the MODE Register, each tone starts from V_{BIAS} and returns to V_{BIAS} before ending:

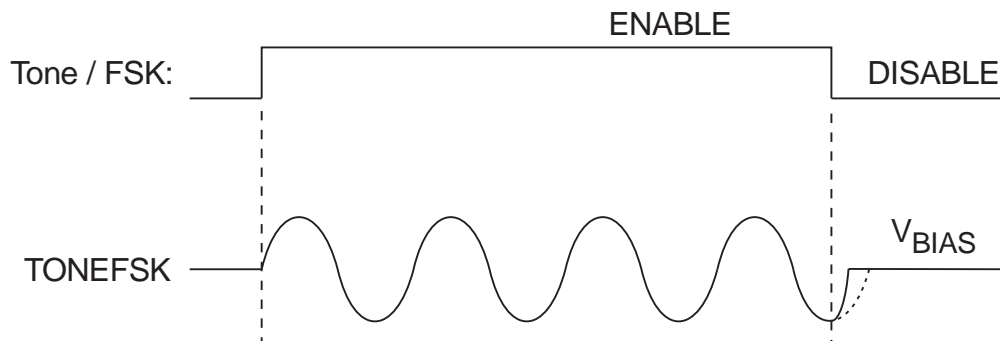


Figure 7: Tone Starting and Stopping

When switching between tones in the same column (bits 4 - 7 or bits 0 - 3) of the TX TONES Register, the transition will be phase continuous. However, switching to the "OFF" state will immediately take the output of that tone generator to V_{BIAS} .

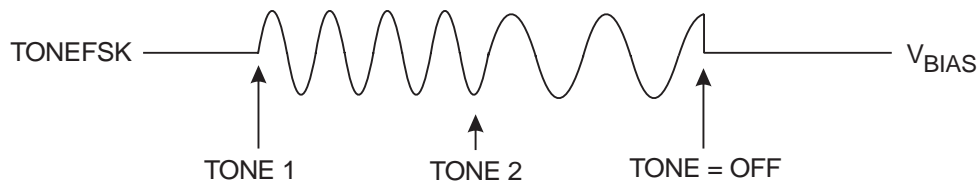


Figure 8: Tone Changing

TX TONES Register codes that do not have a frequency allocated are indicated by a dash (-) in the Tone Field tables. These values should not be used.

5.1 Telecom Tones

The following table provides the hex codes to be programmed into the particular tone field location for various telecommunications systems applications. The tables are not exhaustive, but list the more commonly used tones.

Single Tone (Hz)	Field 0 (Hex)	Dual Tone (Hz)	Field 0 (Hex)
375.2	\$60	375.2+1827	\$6E
404.3	\$70	404.3+1827	\$7E
468	\$80	468+1827	\$8E
495.8	\$90	495.8+1827	\$9E
520.6	\$A0	520.6+1827	\$AE
548	\$B0	548+1827	\$BE
562.8	\$C0	562.8+1827	\$CE
578.4	\$D0	578.4+1827	\$DE
1633	\$0D		

Table 11: On Hook 'CPE Alert Tone'

Group A (Hz)	Field 0 (Hex)	Group B (Hz)	Field 0 (Hex)
252.4	\$10	468	\$80
268.7	\$20	495.8	\$90
285.3	\$30	520.6	\$A0
315.5	\$40	562.8	\$C0
330.5	\$50	595	\$E0
375.2	\$60	612.5	\$F0

Table 12: NYNEX (MRAA) - AMR Alert Tones

(Hz)	Field 1 (Hex)
Off	\$00
120	\$10
150	\$20
154	\$30
250	\$40
300	\$50
350	\$60
400	\$C0
425	\$04
440	\$06
450	\$07
480	\$09
500	\$0A
600	\$0B
620	\$0C

Table 13: Single Frequency Call Progress Tones

Additive Mixing (Hz)	Field 1 (Hex)	Multiplicative Mixing (Hz)	Field 1 (Hex)
Off	\$00		
350+440	\$66	400*16.2	\$B2
440+480	\$F6	400*20	\$A3
480+620	\$FC	400*25	\$94
400+425	\$C4	400*33	\$85
400+450	\$C7	400*40	\$76
425+450	\$D4	400*50	\$67
425+480	\$F4	450*25	\$E4
120+620	\$1C	600*120	\$FD
150+450	\$27		

Table 14: Dual Frequency Call Progress Tones

(Hz)	Field 2 (Hex)
Off	\$00
941+1633	\$FF
697+1209	\$CC
697+1336	\$CD
697+1477	\$CE
770+1209	\$DC
770+1336	\$DD
770+1477	\$DE
852+1209	\$EC
852+1336	\$ED
852+1477	\$EE
941+1336	\$FD
941+1209	\$FC
941+1477	\$FE
697+1633	\$CF
770+1633	\$DF
852+1633	\$EF

Table 15: Dual Tone Multi Frequency Generation

(Hz)	Field 2 (Hex)
Off	\$00
950	\$80
1100	\$30
1300	\$40
1400	\$90
1800	\$A0
2100	\$08
2225	\$09
2130+2750	\$BB

Table 16: Special Information Tones, Fax and Modem Tones and Customer Premises Alert Tones

(Hz)	Field 2 (Hex)
700+900	\$12
700+1100	\$13
900+1100	\$23
700+1300	\$14
900+1300	\$24
1100+1300	\$34
700+1500	\$15
900+1500	\$25
1100+1500	\$35
1300+1500	\$45
700+1700	\$16
900+1700	\$26
1100+1700	\$36
1300+1700	\$46
1500+1700	\$56

Table 17: CCITT 'R1' Signaling Tones

Forward mode (Hz)	Field 3 (Hex)	Backward mode (Hz)	Field 3 (Hex)
Off	\$00	Off	\$00
1380+1500	\$89	1140+1020	\$65
1380+1620	\$8A	1140+900	\$64
1500+1620	\$9A	1020+900	\$54
1380+1740	\$8B	1140+780	\$63
1500+1740	\$9B	1020+780	\$53
1620+1740	\$AB	900+780	\$43
1380+1860	\$8C	1140+660	\$62
1500+1860	\$9C	1020+660	\$52
1620+1860	\$AC	900+660	\$42
1740+1860	\$BC	780+660	\$32
1380+1980	\$8D	1140+540	\$61
1500+1980	\$9D	1020+540	\$51
1620+1980	\$AD	900+540	\$41
1740+1980	\$BD	780+540	\$31
1860+1980	\$CD	660+540	\$21

Table 18: CCITT 'R2' Signaling Tones

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	$V_{DD} + 0.3$	V
Current into or out of			
V_{DD}	-50	50	mA
V_{SS}	-50	50	mA
Any other pin	-20	20	mA
D4/P3 Package	Min.	Max.	Unit
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		800	mW
Derating above 25°C		13	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply ($V_{DD} - V_{SS}$)		2.7	5.5	V
Operating Temperature		-40	85	$^{\circ}\text{C}$
Xtal Frequency	1	3.575965	3.583125	MHz

Notes:

1. A Xtal frequency of 3.579545MHz \pm 0.1% is required for correct operation.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 2.7V$ at $T_{AMB} = 25^{\circ}C$ and $V_{DD} = 3.0V$ to $5.5V$ at $T_{AMB} = -40$ to $+85^{\circ}C$,

XTAL Frequency = $3.579545MHz \pm 0.1\%$, 0dBm corresponds to $775mV_{RMS}$.

	Notes	Min.	Typ.	Max.	Unit
DC Parameters					
I_{DD}					
Zero-Power Mode	1, 2		<1.0		μA
OpAmp only, Enabled, $V_{DD} = 5.0V$	1		1.5		mA
OpAmp only, Enabled, $V_{DD} = 3.3V$	1		0.75		mA
All Enabled, $V_{DD} = 5.0V$	1		5.0	7.5	mA
All Enabled, $V_{DD} = 3.3V$	1		3.0	4.5	mA
Logic '1' Input Level	3	70%			V_{DD}
Logic '0' Input Level	3			30%	V_{DD}
Logic Input Leakage Current ($V_{IN} = 0$ to V_{DD}), (excluding XTAL/CLOCK input)	3	-1.0		+1.0	μA
Output Logic '1' Level ($I_{OH} = 360\mu A$)		$V_{DD}-0.4$			V
Output Logic '0' Level ($I_{OL} = 360\mu A$)				0.4	V
\overline{IRQ} output 'Off' State Current ($V_{OUT} = V_{DD}$)				1.0	μA
FSK Encoder and Tx UART					
Level at TONEFSK pin	4	-1.0	0.0	1.0	dBm
Twist (Mark level with respect to Space level)		-2.0	0	+2.0	dB
Tx 1200bits/sec (V23 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1297	1300	1303	Hz
Space (Logical 0) Frequency		2097	2100	2103	Hz
Tx 1200bits/sec (Bell 202 mode)					
Baud Rate (set by UART and Xtal frequency)		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1197	1200	1203	Hz
Space (Logical 0) Frequency		2197	2200	2203	Hz
TONEFSK Signal Level					
Level at TONEFSK pin for:					
Single tone	4	-1.0	0	1.0	dBm
Dual tone (per tone)	4	-4.0	-3.0	-2.0	dBm
DTMF High Frequency Group	4	-4.0	-3.0	-2.0	dBm
DTMF Low Frequency Group	4	-6.0	-5.0	-4.0	dBm
Output Impedance			10.0		$k\Omega$
Tone frequency resolution		-2.0		2	Hz
Tone output distortion	5		0.8		%
SPM Signal Level					
Level at SPM pin	4, 6	-1.5	0	1.0	dBm
Level at SPM pin, at T_{AMB}	4, 6, 8	-1.0	0	0.5	dBm
Tone frequency accuracy		-14.0		14.0	Hz
Tone output distortion	5		1.2		%
Output Impedance			10.0		$k\Omega$

	Notes	Min.	Typ.	Max.	Unit
Uncommitted Amplifier					
Open Loop Gain (input = 1mV _{RMS} at 100Hz)			60.0		dB
Unity Gain Bandwidth			5.0		MHz
Input Impedance (at 100Hz)		10.0			MΩ
Output Impedance (Open Loop)			10.0		kΩ
Power-Up Timing					
Zero-Power to reliable signal at AMPOUT, RING, SPM, or TONEFSK output pins			50		ms
XTAL/CLOCK Input					
'High' Pulse Width	7	100			ns
'Low' Pulse Width	7	100			ns
Input Impedance (at 100Hz)			1.0		MΩ
Gain (input = 1mV _{RMS} at 100Hz)		20.0			dB

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the CMX615 pins by external circuitry other than X1, C1 and C2.
2. All logic inputs at V_{SS} except for $\overline{\text{CS}}$ input, which is at V_{DD}.
3. Excluding XTAL/CLOCK pin.
4. At V_{DD} = 5.0V, load resistance greater than 40kΩ, signal levels are proportional to V_{DD}.
5. Frequency above 300Hz.
6. SPM has a soft rise and fall time of about 4.5ms. The level changes between V_{BIAS} and 0dBm in 2dB steps, 16 steps per rise and fall. When SPM is disabled, an extra 4.5ms falling tail end of signal should be taken into consideration.
7. Timing for an external input to the XTAL/CLOCK pin.
8. Over the range V_{DD} = 3.0V to 5.5V at T_{AMB} = 25°C

6.1.4 Timing

'C-BUS' Timings (See Figure 9)		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	\overline{CS} -Enable to Clock-High time		100			ns
t_{CSH}	Last Clock-High to \overline{CS} -High time		100			ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0			ns
t_{HIZ}	\overline{CS} -High to Reply Output 3-state time				1.0	μs
t_{CSOFF}	\overline{CS} -High Time between transactions		1.0			μs
t_{NXT}	Inter-Byte Time		500			ns
t_{CK}	Clock-Cycle time		500			ns
t_{CH}	Serial Clock-High time		200			ns
t_{CL}	Serial Clock-Low time		200			ns
t_{CDS}	Command Data Set-Up time		75			ns
t_{CDH}	Command Data Hold time		25			ns
t_{RDS}	Reply Data Set-Up time		75			ns
t_{RDH}	Reply Data Hold time		0			ns

Note: These timings are for the latest version of the 'C-BUS' as embodied in the CMX615, and allow faster transfers than the original 'C-BUS' timings provided in MX-COM's Publication Doc. # 20480060.001.

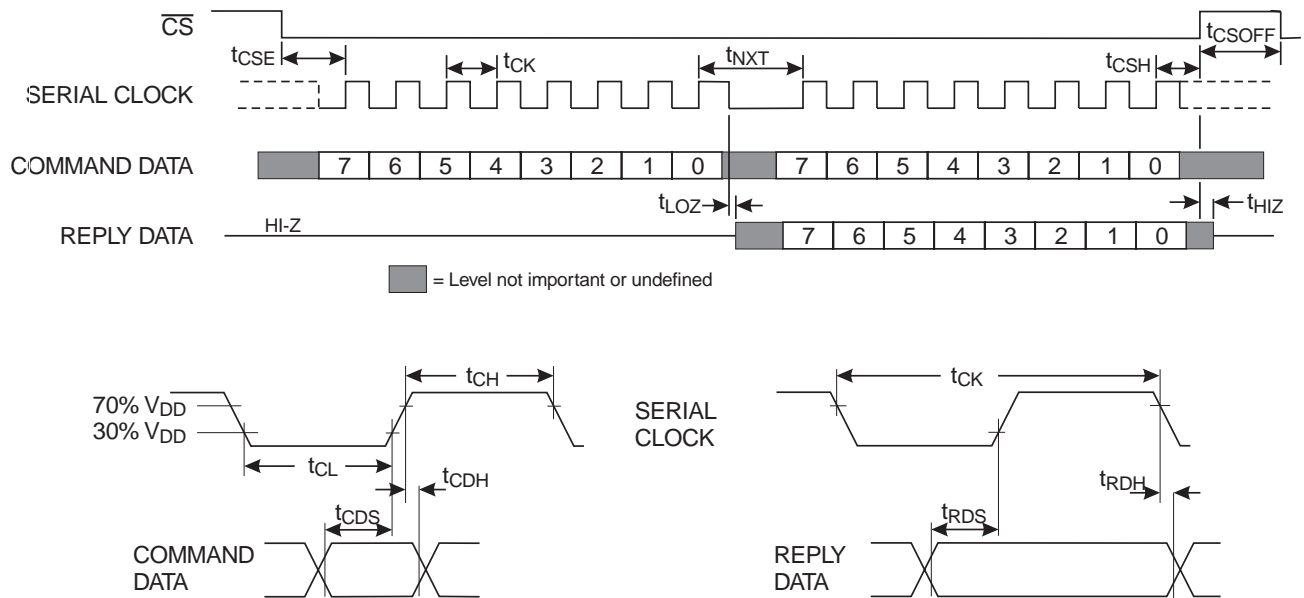


Figure 9: 'C-BUS' Timing

6.2 Packaging

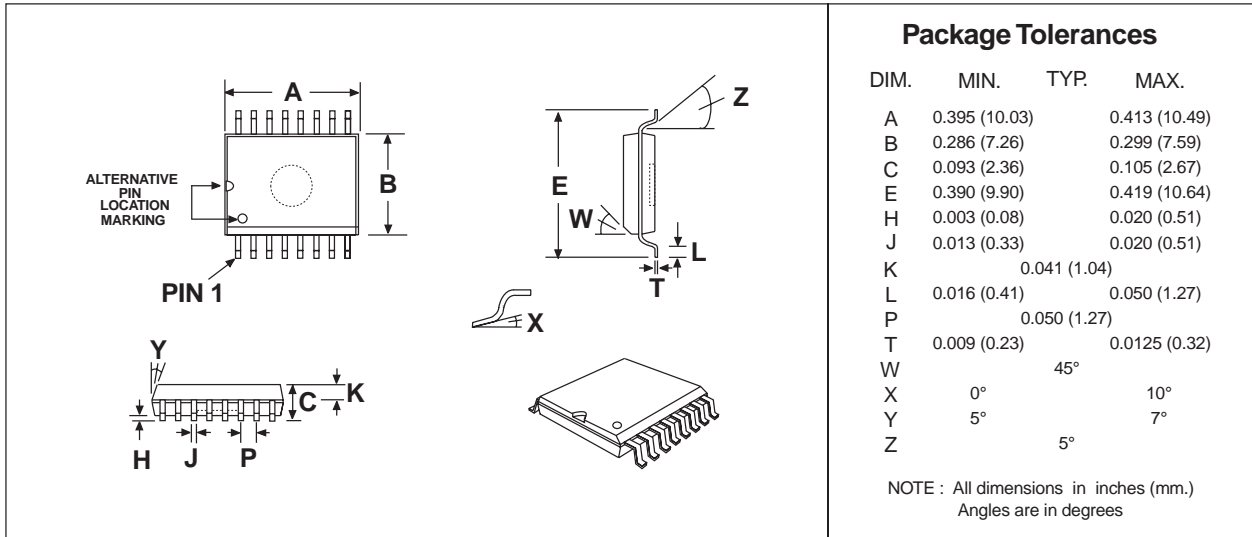


Figure 10: 16-pin SOIC (D4) Mechanical Outline: *Order as part no. CMX615D4*

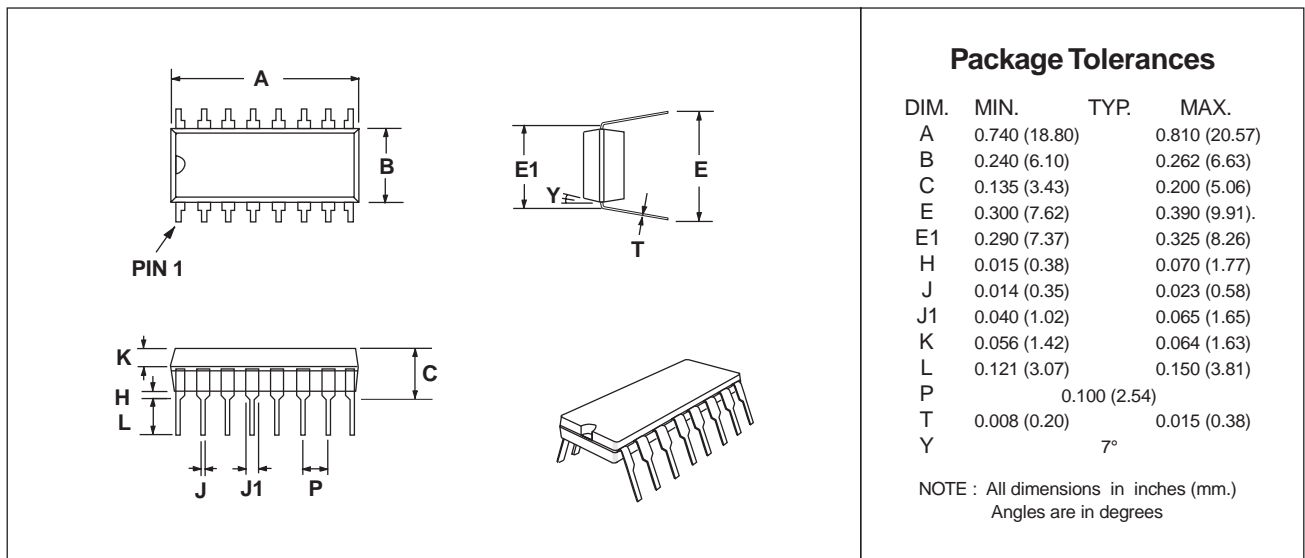


Figure 11: 16-pin PDIP (P3) Mechanical Outline: *Order as part no. CMX615P3*