CLEAR LOGIC

CL7256E
CL7256S

Laser Processed Logic Device Family

Key Features

- Laser Processed Logic Device (LPLD™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard Altera® MAX® 7000
- High Density
  - 5,000 Usable gates
  - 256 Macrocells
  - 184 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Low current consumption
- Supports 3.3 volt or 5.0 volt I/O operation
- Alpha particle immune

CL7000 Product Family Overview

Parameter	CL7128E CL7128S	CL7160E CL7160S	CL7192E CL7192S	CL7256E CL7256S
Useable Gates	2,500	3,200	3,750	5,000
Macrocells	128	160	192	256
Logic Blocks	8	10	12	16
Max user I/O pins	100	104	124	164
Speed Grades	-5, -6, -7, -10, -12, -15, -20	-5, -6, -7, -10, -12, -15, -20	-6, -7, -10, -12, -15, -20	-6, -7, -10, -12, -15, -20
Packages	84-pin PLCC 100-pin TQFP 100-pin PQFP 160-pin PQFP	84-pin PLCC 100-pin TQFP 100-pin PQFP 160-pin PQFP	160-pin PQFP	160-pin PQFP 208-pin PQFP 208-pin RQFP

7K tbl 01B

Description

The Clear Logic CL7000 Laser Processed Logic Device (LPLD®) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera MAX® 7000, 7000E, and 7000S products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LPLDs can be used for low cost, high volume production.

Clear Logic's innovative laser-based technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device uses a cell-based, PLD-like architecture. Clear Logic's NoFault® technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL7000 Laser Processed Logic Device family is based upon a large array of macrocells. Each macrocell contains a logic array with five product terms, a product-term select matrix, and a configurable register. A group of sixteen macrocells forms a block. Laser-configured metal fuses implement logical functions and control signal routing.

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

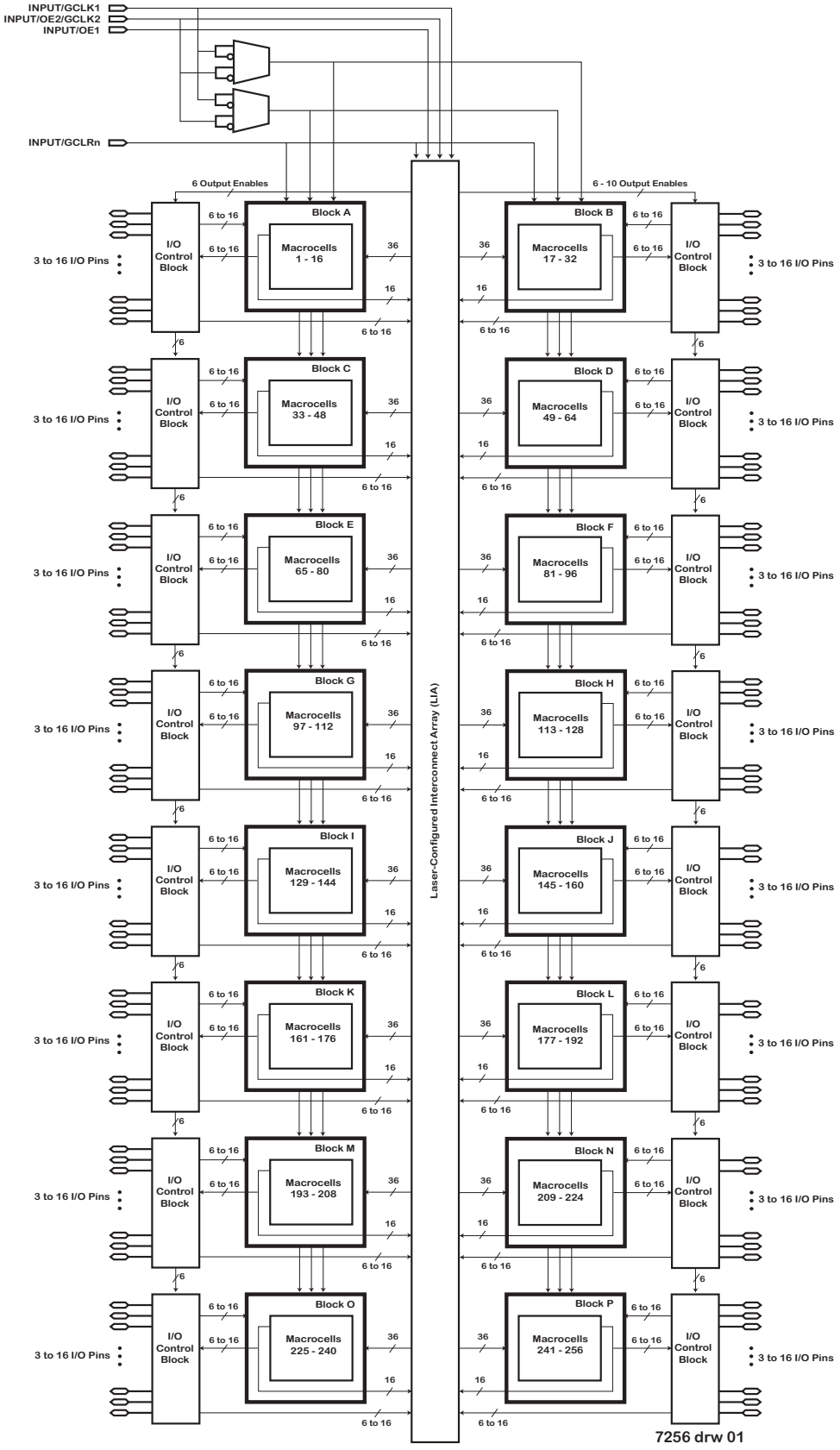
Additional Information

For further information on designing with the CL7000 LPLD family, please consult the following documents:

- AN-01: Requesting a First Article. This document provides instructions on how to submit a bitstream file for generation of first articles.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL7000 family.
- AN-09: CL7000 Technology White Paper. This document outlines the technologies employed by the CL7000 LPLD family.
- AN-10: Calculating CL7000 Power Consumption. This document provides guidelines for calculating power consumption based on design characteristics.
- AN-11: CL7000 Test Methodology. This document discribes how Clear Logic provides 100% stuck-at fault coverage.

- AN-12: CL7000 LPLD Timing and Function Compatability. This document shows how a seamless conversion from CPLD to ASIC can be achieve with no additional engineering with Clear Logic.

Block Diagram



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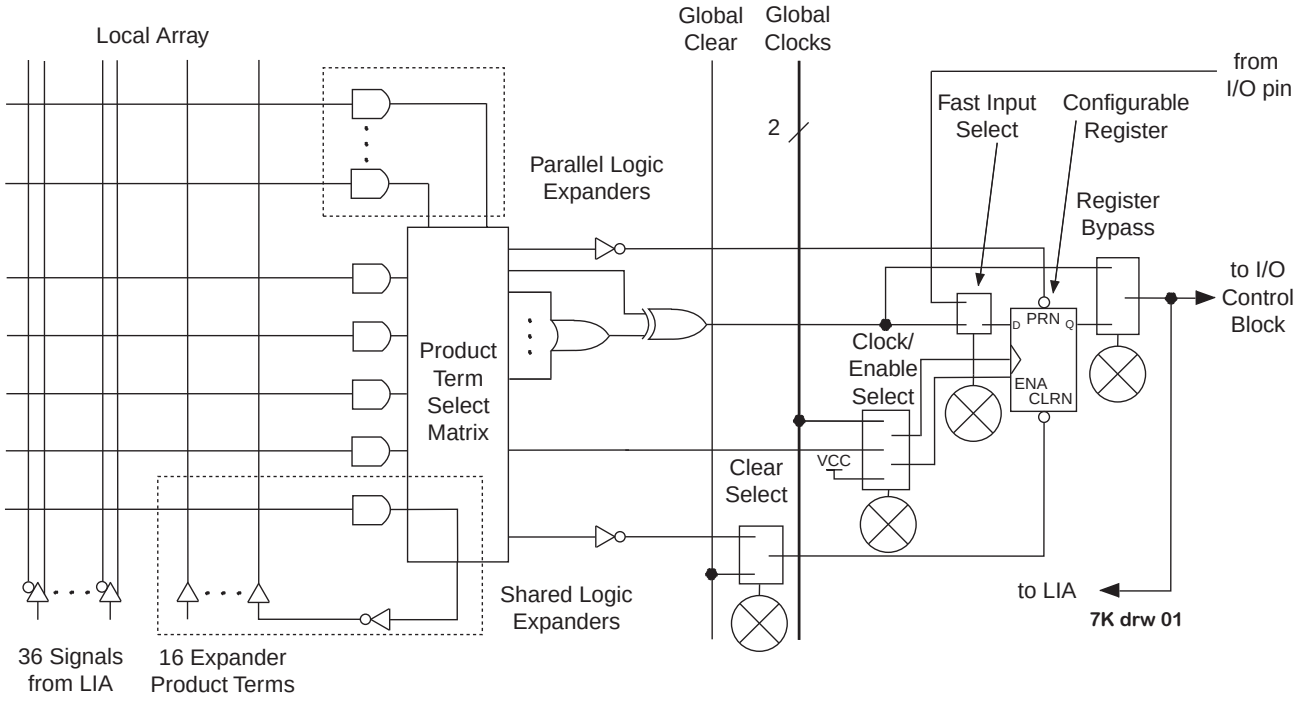
Macrocell Diagram



Pin Configuration

Pin Name	160 pin PQFP	208 pin RQFP/PQFP
INPUT/GCLK1	139	184
INPUT/GCLRn	141	182
INPUT/OE1	140	183
INPUT/OE2/GCLK2	142	181
TDI	146	176
TMS	23	127
TCK	98	30
TDO	135	189
GND	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCCINT	56, 65, 137, 144	74, 83, 179, 186
VCCIO	10, 25, 40, 55, 74, 89, 103, 118, 133, 155	5, 23, 41, 63, 85, 107, 125, 143, 165, 191
NC (No Connect)	-	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208
Total user I/O pins	**128**	**160**

7256 tbl 01

DC Electrical Specifications

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage, internal logic and input buffers				
	Commercial Grade Devices		4.75	5.25	V
	Industrial Grade Devices		4.50	5.50	V
V_{CCIO}	DC input voltage				
	5.0 volt commercial		4.75	5.25	V
	5.0 volt industrial		4.50	5.50	V
	3.3 volt operation		3.00	3.60	V
V_I	Input voltage		-0.5	V_{CCINT}+0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature				
	Commercial temperature range		0	70	°C
	Industrial temperature range		-40	85	°C
T_J	Junction Operating temperature				
	Commercial temperature range		0	90	°C
	Industrial temperature range		-40	105	°C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns
t_{RVCC}	V_{CC} rise time			100	ms

7K tbl 02

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	-2.0	7.0	V
V_I	DC input voltage[1]	With respect to ground	-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		135	°C

7K tbl 03

DC Electrical Specifications cont.

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input Voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Input LOW Voltage[1]		-0.5	0.8	V
V_{OH}	5.0-V high-level TTL output Voltage	I_{OH} = -4 mA DC, V_{CCIO} = 4.75 V	2.4		V
	3.3-V high-level TTL output Voltage	I_{OH} = -4 mA DC, V_{CCIO} = 3.00 V	2.4		V
	3.3-V high-level CMOS output Voltage	I_{OH} = -0.1 mA DC, V_{CCIO} = 3.0 V	V_{CCIO}-0.2		V
V_{OL}	5.0-V high-level TTL output Voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V		0.45	V
	3.3-V high-level TTL output Voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V		0.45	V
	3.3-V high-level CMOS output Voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V		0.2	V
I_{IN}	Input Leakage Current	V_I = VCC or GND	-10	10	µA
I_{OZ}	Output Leakage Current	V_O = VCC or GND	-40	40	µA

7K tbl 04

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

7K tbl 05

AC Electrical Specifications

I/O Element Timing Parameters [5]

			Speed: -6		Speed: -7		Speed: -10		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time		4.2		3.9		7.0		ns
t_H	Global clock hold time		-0.8		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.5		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF	1.0	3.7		4.7		5.0	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		ns
t_{ASU}	Array clock setup time		1.9		0.8		2.0		ns
t_{AH}	Array clock hold time		1.5		1.9		3.0		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		6.0		7.8		10.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		ns
t_{ODH}	Output data hold time after clock	C_L = 35 pF	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.9		7.8		10.0	ns
f_{CNT}	Max. internal global clock frequency		144.9		128.2		100.0		MHz
t_{ACNT}	Minimum array clock period			6.9		7.8		10.0	ns
f_{ACNT}	Max. internal array clock frequency		144.9		128.2		100.0		MHz

7K tbl 06E1

AC Electrical Specifications cont.

External Timing Parameters

			Speed: -12P		Speed: -12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		12.0		12.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		12.0		12.0	ns
t_{SU}	Global clock setup time		7.0		10.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF		6.0		6.0	ns
t_{CH}	Global clock high time		4.0		4.0		ns
t_{CL}	Global clock low time		4.0		4.0		ns
t_{ASU}	Array clock setup time		3.0		4.0		ns
t_{AH}	Array clock hold time		4.0		4.0		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		12.0		12.0	ns
t_{ACH}	Array clock high time		5.0		5.0		ns
t_{ACL}	Array clock low time		5.0		5.0		ns
t_{ODH}	Output data hold time after clock	C_L = 35 pF	1.0		1.0		ns
t_{CNT}	Minimum global clock period			11.0		11.0	ns
f_{CNT}	Maximum internal global clock frequency		90.9		90.9		MHz
t_{ACNT}	Minimum array clock period			11.0		11.0	ns
f_{ACNT}	Maximum internal array clock frequency		90.9		90.9		MHz

7K tbl 06E2

AC Electrical Specifications cont.

External Timing Parameters

			Speed: -15		Speed: -20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C_L = 35 pF		15.0		20.0	ns
t_{PD2}	I/O input to non-registered output	C_L = 35 pF		15.0		20.0	ns
t_{SU}	Global clock setup time		11.0		12.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		5.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C_L = 35 pF		8.0		12.0	ns
t_{CH}	Global clock high time		5.0		6.0		ns
t_{CL}	Global clock low time		5.0		6.0		ns
t_{ASU}	Array clock setup time		4.0		5.0		ns
t_{AH}	Array clock hold time		4.0		5.0		ns
t_{ACO1}	Array clock to output delay	C_L = 35 pF		15.0		20.0	ns
t_{ACH}	Array clock high time		6.0		8.0		ns
t_{ACL}	Array clock low time		6.0		8.0		ns
t_{ODH}	Output data hold time after clock	C_L = 35 pF	1.0		1.0		ns
t_{CNT}	Minimum global clock period			13.0		16.0	ns
f_{CNT}	Maximum internal global clock frequency		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13.0		16.0	ns
f_{ACNT}	Maximum internal array clock frequency		76.9		62.5		MHz

7K tbl 06E3

AC Electrical Specifications cont.

Internal Timing Parameters[4]

Symbol	Parameter	Conditions	Speed: -6 Min	Speed: -6 Max	Speed: -7 Min	Speed: -7 Max	Speed: -10 Min	Speed: -10 Max	Unit
t_{IN}	Input pad and buffer delay			0.6		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.3		0.5	ns
t_{FIN}	Fast input delay			2.7		3.4		1.0	ns
t_{SEXP}	Shared expander delay			2.5		3.9		5.0	ns
t_{PEXP}	Parallel expander delay			0.7		1.1		0.8	ns
t_{LAD}	Logic array delay			2.4		2.6		5.0	ns
t_{LAC}	Logic control array delay			2.4		2.6		5.0	ns
t_{IOE}	Internal output enable delay			0.0		0.8		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		0.4		0.5		1.5	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		0.9		1.0		2.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.4		5.5		5.5	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.9		1.1		2.0		ns
t_{H}	Register hold time		1.5		1.6		3.0		ns
t_{FSU}	Register setup time of fast input		0.8		2.4		3.0		ns
t_{FH}	Register hold time of fast input		1.7		0.6		0.5		ns
t_{RD}	Register delay			1.7		1.1		2.0	ns
t_{COMB}	Combinatorial delay			1.7		1.1		2.0	ns
t_{IC}	Array clock delay			2.4		2.9		5.0	ns
t_{EN}	Register enable time			2.4		2.6		5.0	ns
t_{GLOB}	Global control delay			1.0		2.8		1.0	ns
t_{PRE}	Register preset time			3.1		2.7		3.0	ns
t_{CLR}	Register clear time			3.1		2.7		3.0	ns
t_{LIA}	LIA delay			1.0		3.0		1.0	ns

7K tbl 07E1

AC Electrical Specifications cont.

Internal Timing Parameters[4]

Symbol	Parameter	Conditions	Speed: -12P Min	Speed: -12P Max	Speed: -12 Min	Speed: -12 Max	Unit
t_{IN}	Input pad and buffer delay			1.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t_{FIN}	Fast input delay			1.0		1.0	ns
t_{SEXP}	Shared expander delay			7.0		7.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0	ns
t_{LAD}	Logic array delay			7.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay			2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		1.0		3.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		2.0		4.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		5.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		6.0		6.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		7.0		7.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		6.0		6.0	ns
t_{SU}	Register setup time		1.0		4.0		ns
t_{H}	Register hold time		6.0		4.0		ns
t_{FSU}	Register setup time of fast input		4.0		2.0		ns
t_{FH}	Register hold time of fast input		0.0		2.0		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			7.0		5.0	ns
t_{GLOB}	Global control delay			2.0		0.0	ns
t_{PRE}	Register preset time			4.0		3.0	ns
t_{CLR}	Register clear time			4.0		3.0	ns
t_{LIA}	LIA delay			1.0		1.0	ns

7K tbl 07E2

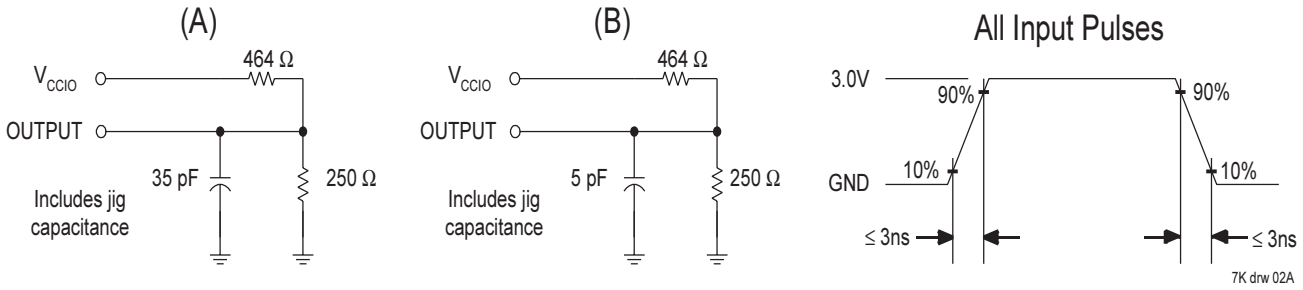
AC Electrical Specifications cont.

Internal Timing Parameters[4]

			Speed: -15		Speed: -20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		3.0	ns
t_{FIN}	Fast input delay			2.0		4.0	ns
t_{SEXP}	Shared expander delay			8.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		8.0	ns
t_{IOE}	Internal output enable delay			3.0		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		5.0		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		8.0		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 5.0 V	C_L = 35 pF		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, V_{CCIO} = 3.3 V	C_L = 35 pF		7.0		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	C_L = 35 pF		10.0		14.0	ns
t_{XZ}	Output buffer disable delay	C_L = 5 pF[3]		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		ns
t_H	Register hold time		4.0		5.0		ns
t_{FSU}	Register setup time of fast input		2.0		4.0		ns
t_{FH}	Register hold time of fast input		1.0		3.0		ns
t_{RD}	Register delay			1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0	ns
t_{IC}	Array clock delay			6.0		8.0	ns
t_{EN}	Register enable time			6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0	ns
t_{LIA}	LIA delay			2.0		3.0	ns

7K tbl 07E3

AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0V for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3V.

2. Typical values are at V_{CC} of 5.0 volts and ambient temperature of 25 ºC.

3. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

4. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Revision History

11 Jan. 1999:	Created new document
30 Apr. 1999:	Recompiled databook, no changes.
31 July 1999:	Added -6ns speed grade, revised Product Family Overview, Corrected Pin Configuration Table
13 Oct. 1999:	Corrected typographical error in AC Test Condition diagram (W changed to Ω)
1 Dec. 2000:	Updated application note reference.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL7256EQC160-20	Commercial	160-pin Plastic QFP	-20	EPM7256EQC160-20
CL7256EQC160-15			-15	EPM7256EQC160-15
CL7256EQC160-12			-12	EPM7256EQC160-12
CL7256EQC160-12P			-12 PCI	EPM7256EQC160-12P
CL7256EQC160-10			-10	N/A
CL7256ERC208-20		208-pin Power QFP	-20	EPM7256ERC208-20
CL7256ERC208-15			-15	EPM7256ERC208-15
CL7256ERC208-12			-12	EPM7256ERC208-12
CL7256ERC208-12P			-12 PCI	EPM7256ERC208-12P
CL7256ERC208-10			-10	N/A
CL7256ERI208-20	Industrial		-20	EPM7256ERI208-20
CL7256SQC208-15	Commercial	208-pin Plastic QFP	-15	EPM7256SQC208-15
CL7256SQC208-10			-10	EPM7256SQC208-10
CL7256SQC208-7			-7	EPM7256SQC208-7
CL7256SQC208-6			-6	N/A
CL7256SRC208-15		208-pin Power QFP	-15	EPM7256SRC208-15
CL7256SRC208-10			-10	EPM7256SRC208-10
CL7256SRC208-7			-7	EPM7256SRC208-7
CL7256SRC208-6			-6	N/A
CL7256SRI208-10	Industrial		-10	EPM7256SRI208-10

7256 tbl 02