N-Channel Power MOSFET 800 V, 4.5 Ω

Features

- ESD Diode-Protected Gate
- 100% Avalanche Tested
- 100% Rg Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDD	NDF	Unit
Drain-to-Source Voltage	V _{DSS}	800		٧
Continuous Drain Current R _{θJC}	Ι _D	2.9	3.3 (Note 1)	Α
Continuous Drain Current $R_{\theta JC}$, $T_A = 100^{\circ}C$	I _D	1.9	2.1 (Note 1)	Α
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	12	13	Α
Power Dissipation $R_{\theta JC}$	P _D	96	25	W
Gate-to-Source Voltage	V _{GS}	±30		V
Single Pulse Avalanche Energy, I _D = 2.5 A	E _{AS}	100		mJ
ESD (HBM) (JESD22-A114)	V _{esd}	2300		٧
RMS Isolation Voltage (t = 0.3 sec., R.H. \leq 30%, T _A = 25°C) (Figure 14)	V _{ISO}	4500		٧
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Continuous Source Current (Body Diode)	Is	3.3		Α
Maximum Temperature for Soldering Leads	TL	260		°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Limited by maximum junction temperature
- 2. $I_S = 3.3$ Å, $di/dt \le 100$ Å/ μ s, $V_{DD} \le BV_{DSS}$, $T_J = +150$ °C

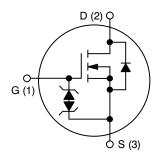


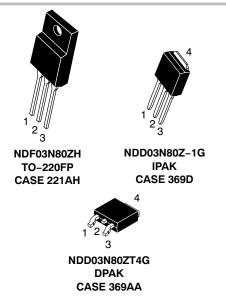
ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX
800 V	4.5 Ω @ 10 V

N-Channel





MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE

Parameter		Symbol	Value	Unit
Junction-to-Case (Drain)	NDF03N80Z NDD03N80Z	$R_{ heta JC}$	4.0 1.3	°C/W
Junction-to-Ambient Steady State	(Note 3) NDF03N80Z (Note 4) NDD03N80Z (Note 3) NDD03N80Z-1	$R_{ hetaJA}$	50 33 96	

^{3.} Insertion mounted

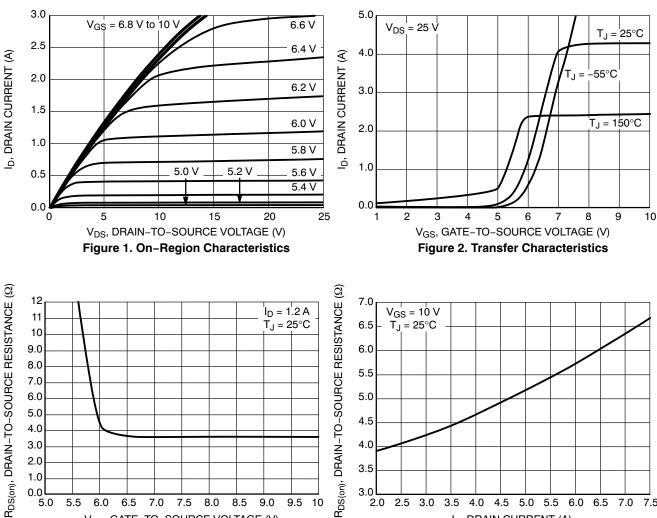
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

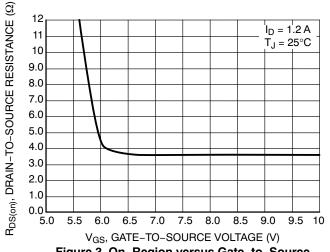
Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
OFF CHARACTERISTICS			-				
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$		800			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C, I _D = 1 mA			870		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 800 V, V _{GS} = 0 V	T _J = 25°C			1.0	μΑ
			T _J = 125°C			50	1
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V				±10	μΑ
ON CHARACTERISTICS (Note 5)			-		-		
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}$, $I_D = 50$	μΑ	3.0	4.1	4.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D =	= 50 μΑ		11		mV/°C
Static Drain-to-Source On Resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 1.	2 A		3.7	4.5	Ω
Forward Transconductance	9FS	V _{DS} = 15 V, I _D = 1.	2 A		2.1		S
DYNAMIC CHARACTERISTICS			_			-	
Input Capacitance (Note 6)	C _{iss}				440		pF
Output Capacitance (Note 6)	C _{oss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$			52		1
Reverse Transfer Capacitance (Note 6)	C _{rss}				9.0		
Total Gate Charge (Note 6)	Qg	V _{DS} = 400 V, I _D = 3.3 A, V _{GS} = 10 V			17		nC
Gate-to-Source Charge (Note 6)	Q _{gs}				3.5		1
Gate-to-Drain ("Miller") Charge (Note 6)	Q _{gd}				9.1		
Plateau Voltage	V _{GP}				6.5		V
Gate Resistance	R_g				5.5		Ω
RESISTIVE SWITCHING CHARACTER	ISTICS (Note 7)		-				
Turn-on Delay Time	t _{d(on)}				9.0		ns
Rise Time	t _r	$V_{DD} = 400 \text{ V}, I_D = 3.$	3 A,		7.0		1
Turn-off Delay Time	t _{d(off)}	$V_{GS} = 10 \text{ V}, R_{G} = 0$	Ω		17		1
Fall Time	t _f				9.0		1
SOURCE-DRAIN DIODE CHARACTEF	RISTICS						•
Diode Forward Voltage	V _{SD}		T _J = 25°C		0.9	1.6	V
		$I_S = 3.0 \text{ A}, V_{GS} = 0 \text{ V}$ $T_J = 100^{\circ}\text{C}$			0.8		1
Reverse Recovery Time	t _{rr}	$V_{GS} = 0 \text{ V}, V_{DD} = 30 \text{ V}$ $I_{S} = 3.3 \text{ A}, d_{i}/d_{t} = 100 \text{ A}/\mu\text{s}$			360		ns
Charge Time	t _a				81		1
Discharge Time	t _b				280		1
Reverse Recovery Charge	Q _{rr}				1.3		μС

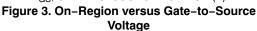
^{4.} Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq [2 oz] including traces).

Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.
 Guaranteed by design.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS







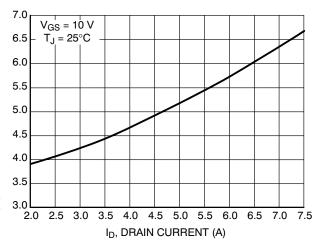


Figure 4. On-Resistance versus Drain **Current and Gate Voltage**

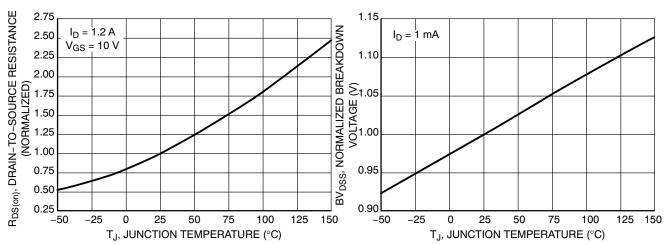


Figure 5. On-Resistance Variation with **Temperature**

Figure 6. BV_{DSS} Variation with Temperature

TYPICAL CHARACTERISTICS

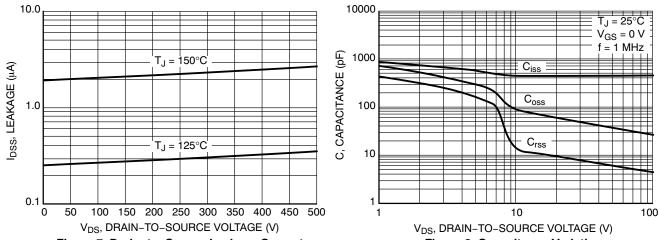


Figure 7. Drain-to-Source Leakage Current versus Voltage

Figure 8. Capacitance Variation

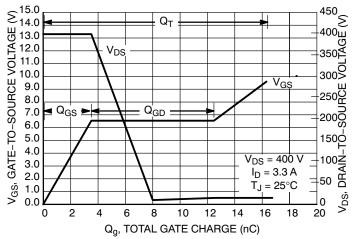


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

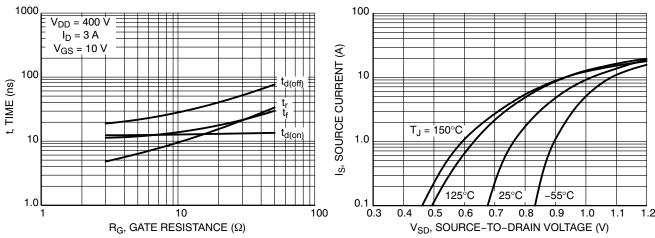


Figure 10. Resistive Switching Time Variation versus Gate Resistance

Figure 11. Diode Forward Voltage versus Current

TYPICAL CHARACTERISTICS

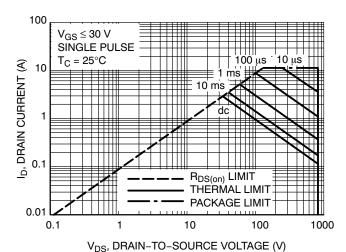


Figure 12. Maximum Rated Forward Biased
Safe Operating Area – NDD03N80Z

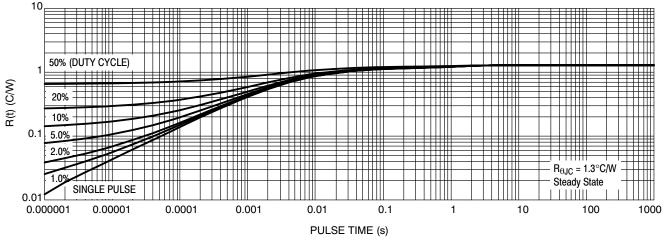


Figure 13. Thermal Impedance (Junction-to-Case) - NDD03N80Z

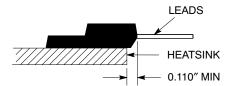


Figure 14. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

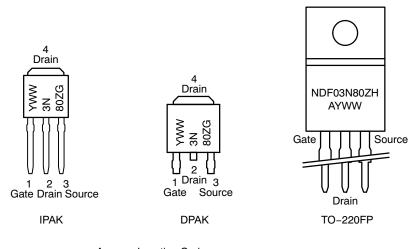
*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 1. ORDERING INFORMATION

Device	Package	Shipping [†]
NDD03N80Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD03N80ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDF03N80ZH (In Development)	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS



A = Location Code

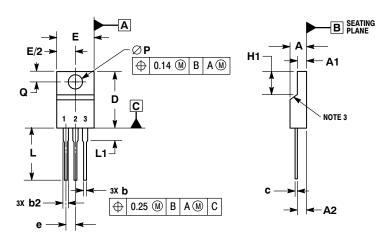
Y = Year

WW = Work Week

 $\mathsf{G},\,\mathsf{H}\quad\mathsf{=Pb\text{-}Free},\,\mathsf{Halogen\text{-}Free}\,\mathsf{Package}$

PACKAGE DIMENSIONS

TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE C



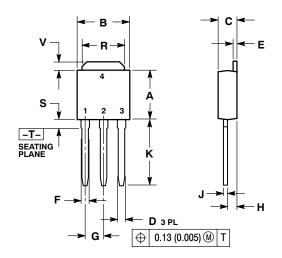
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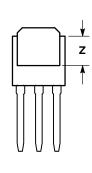
- IOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. CONTOUR UNCONTROLLED IN THIS AREA.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS AND TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS AND TO EXCEED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
 5. DIMENSION LEAD WIDTH INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.

	MILLIMETERS			
DIM	MIN MAX			
Α	4.30	4.70		
A1	2.50	2.90		
A2	2.50	2.70		
b	0.54	0.84		
b2	1.10	1.40		
С	0.49	0.79		
D	14.70	15.30		
E	9.70	10.30		
е	2.54	BSC		
H1	6.70	7.10		
L	12.70	14.73		
L1		2.80		
P	3.00	3.40		
Q	2.80	3.20		

IPAK CASE 369D ISSUE C



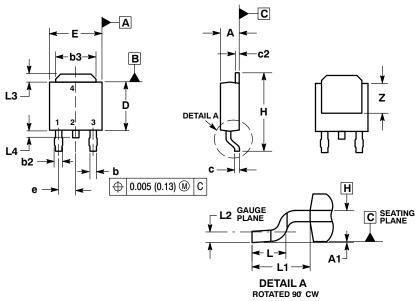


- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
7	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
s	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA ISSUE B

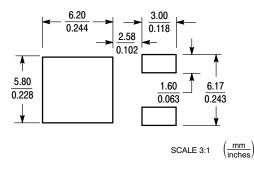


NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3. L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
 5. DIMENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PI ANF H

	INCHES		MILLIMETER		
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.030	0.045	0.76	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
Е	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29 BSC		
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.108	REF	2.74 REF		
L2	0.020	BSC	0.51 BSC		
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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