



M68AR256ML

4 Mbit (256K x16) 1.8V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 1.65 to 1.95V
- 256K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- SINGLE BYTE READ/WRITE
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 1.0V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages

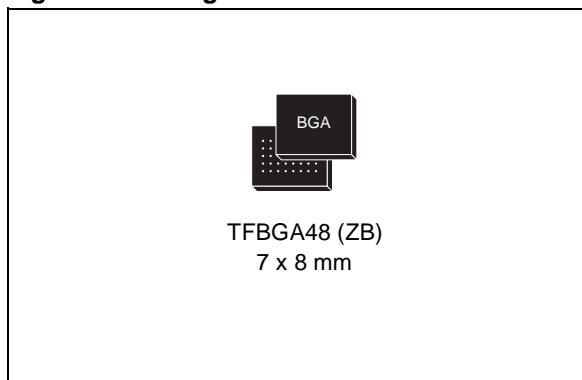


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SUMMARY DESCRIPTION

The M68AR256ML is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 262,144 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 1.8V ($\pm 150\text{mV}$) supply. This device has an

automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AR256ML is available in TFBGA48 (0.75 mm pitch) package.

Figure 2. Logic Diagram

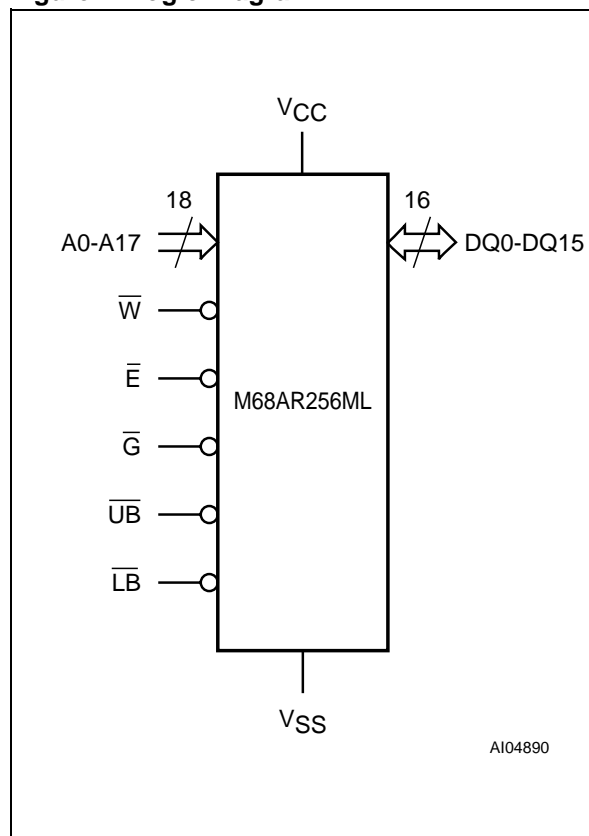


Table 1. Signal Names

| | |
|------------|-----------------------------------|
| A0-A17 | Address Inputs |
| DQ0-DQ15 | Data Input/Output |
| \bar{E} | Chip Enable |
| \bar{G} | Output Enable |
| \bar{W} | Write Enable |
| \bar{UB} | Upper Byte Enable Input |
| \bar{LB} | Lower Byte Enable Input |
| Vcc | Supply Voltage |
| Vss | Ground |
| NC | Not Connected Internally |
| DU | Don't Use as Internally Connected |

Figure 3. TFBGA Connections (Top view through package)

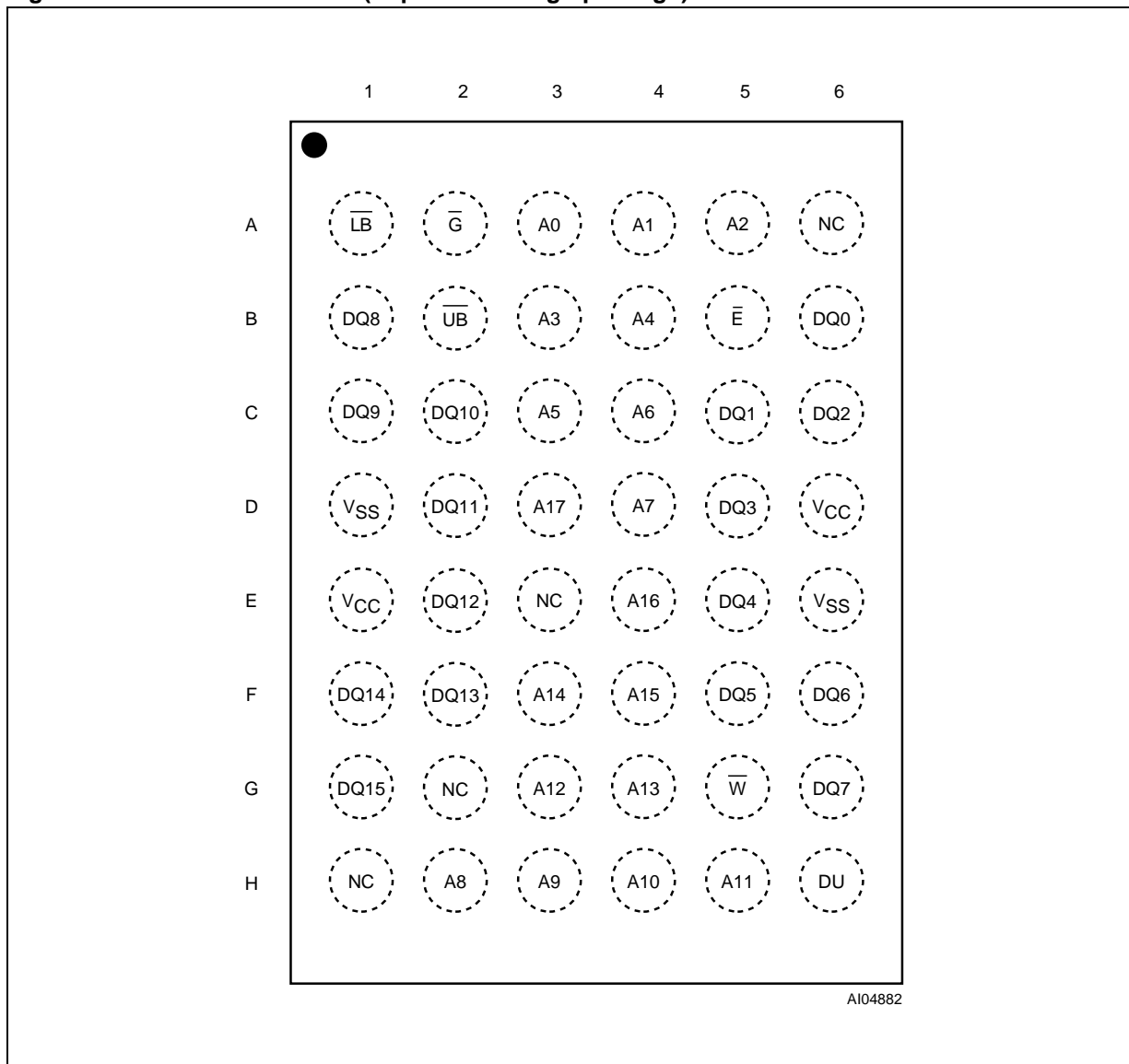
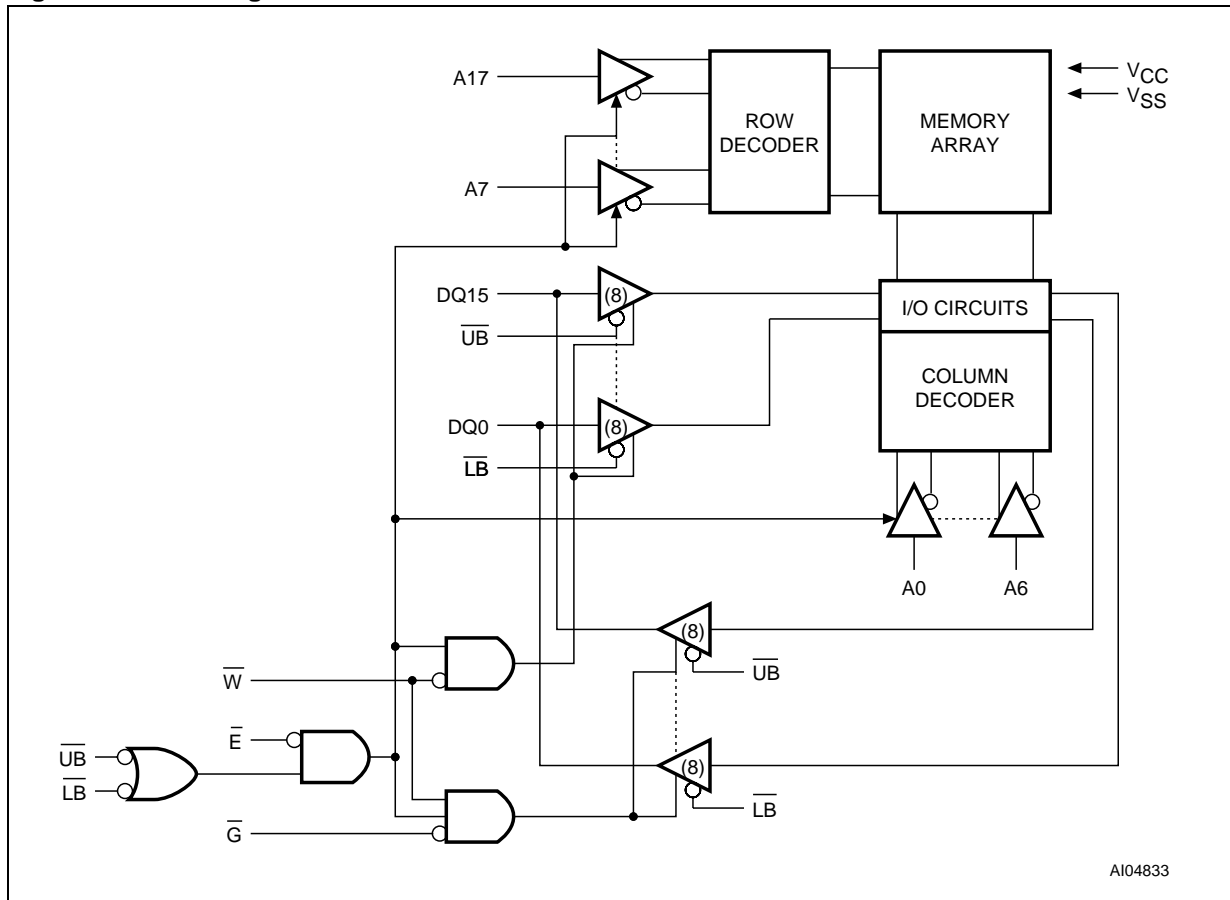


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------|------------------------|------|
| $I_O^{(1)}$ | Output Current | 20 | mA |
| T_A | Ambient Operating Temperature | -55 to 125 | °C |
| T_{STG} | Storage Temperature | -65 to 150 | °C |
| V_{CC} | Supply Voltage | -0.5 to 2.5 | V |
| $V_{IO}^{(2)}$ | Input or Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| P_D | Power Dissipation | 1 | W |

Note: 1. One output at a time, not to exceed 1 second duration.

2. Up to a maximum operating V_{CC} of 1.95V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

| Parameter | | M68AR256ML |
|--|---------|---|
| V _{CC} Supply Voltage | | 1.65 to 1.95V |
| Ambient Operating Temperature | Range 1 | 0 to 70°C |
| | Range 6 | -40 to 85°C |
| Load Capacitance (C _L) | | 30pF |
| Output Circuit Protection Resistance (R ₁) | | 15.3kΩ |
| Load Resistance (R ₂) | | 11.3kΩ |
| Input Rise and Fall Times | | 1ns/V |
| Input Pulse Voltages | | 0 to V _{CC} |
| Input and Output Timing Ref. Voltages | | V _{CC} /2 |
| Output Transition Timing Ref. Voltages | | V _{RL} = 0.3V _{CC} ; V _{RH} = 0.7V _{CC} |

Figure 5. AC Measurement I/O Waveform

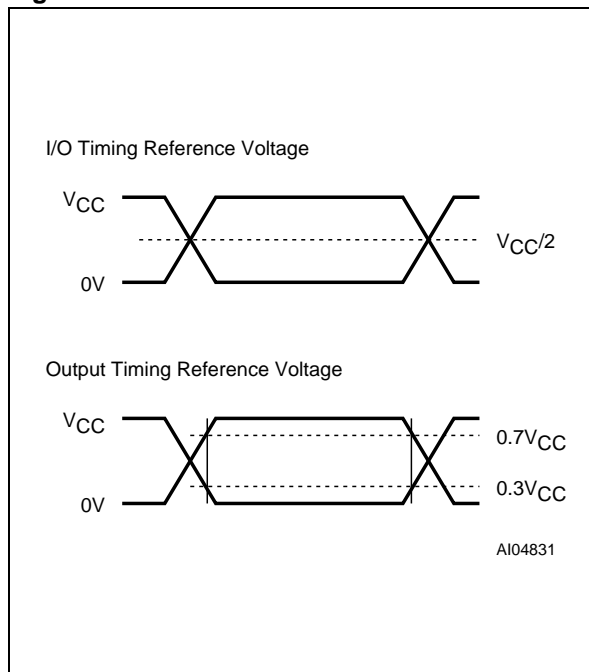


Figure 6. AC Measurement Load Circuit

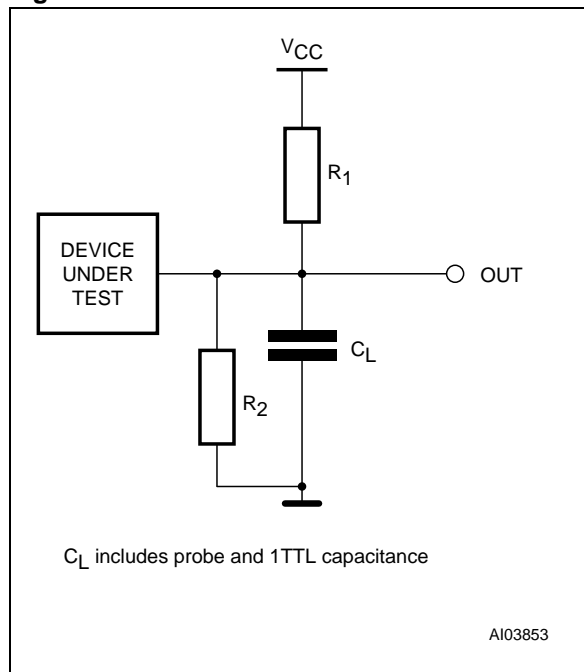


Table 4. Capacitance

| Symbol | Parameter ^(1,2) | Test Condition | Min | Max | Unit |
|------------------|---|-----------------------|-----|-----|------|
| C _{IN} | Input Capacitance on all pins (except DQ) | V _{IN} = 0V | | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | | 8 | pF |

Note: 1. Sampled only, not 100% tested.
 2. At T_A = 25°C, f = 1 MHz, V_{CC} = 1.8V.

Table 5. DC Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-----------------------------|--|------|-----|-----------------------|------|
| I _{CC1} ^(1,2) | Operating Supply Current | V _{CC} = 1.95V, f = 1/t _{AVAV} , I _{OUT} = 0mA | | 2 | 6 | mA |
| I _{CC2} ⁽³⁾ | Operating Supply Current | V _{CC} = 1.95V, f = 1MHz, I _{OUT} = 0mA | | 1 | 2 | mA |
| I _{LI} | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | -1 | | 1 | μA |
| I _{LO} ⁽⁴⁾ | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} ⁽³⁾ | -1 | | 1 | μA |
| I _{SB} | Standby Supply Current CMOS | V _{CC} = 1.95V, $\overline{E} \geq V_{CC} - 0.2V$ or $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$, f = 0 | | 0.5 | 8 | μA |
| V _{IH} | Input High Voltage | | 1.4 | | V _{CC} + 0.4 | V |
| V _{IL} | Input Low Voltage | | -0.5 | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -100μA | 1.5 | | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 100μA | | | 0.2 | V |

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
 2. \overline{E} = V_{IL}, \overline{LB} or/and \overline{UB} = V_{IL}, V_{IN} = V_{IL} or V_{IH}.
 3. $\overline{E} \leq 0.2V$, \overline{LB} or/and $\overline{UB} \leq 0.2V$, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V.
 4. Output disabled.

OPERATION

The M68AR256ML has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted (\overline{E} = High) or LB and UB are de-asserted (LB and UB = High). An Output Enable (\overline{G}) signal provides

a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs \overline{W} , \overline{E} , \overline{LB} and \overline{UB} as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

| Operation | \overline{E} | \overline{W} | \overline{G} | \overline{LB} | \overline{UB} | DQ0-DQ7 | DQ8-DQ15 | Power |
|------------------|----------------|----------------|----------------|-----------------|-----------------|-------------|-------------|----------------------|
| Deselected | V_{IH} | X | X | X | X | Hi-Z | Hi-Z | Standby (I_{SB}) |
| Deselected | X | X | X | V_{IH} | V_{IH} | Hi-Z | Hi-Z | Standby (I_{SB}) |
| Lower Byte Read | V_{IL} | V_{IH} | V_{IL} | V_{IL} | V_{IH} | Data Output | Hi-Z | Active (I_{CC}) |
| Lower Byte Write | V_{IL} | V_{IL} | X | V_{IL} | V_{IH} | Data Input | Hi-Z | Active (I_{CC}) |
| Output Disabled | V_{IL} | V_{IH} | V_{IH} | X | X | Hi-Z | Hi-Z | Active (I_{CC}) |
| Upper Byte Read | V_{IL} | V_{IH} | V_{IL} | V_{IH} | V_{IL} | Hi-Z | Data Output | Active (I_{CC}) |
| Upper Byte Write | V_{IL} | V_{IL} | X | V_{IH} | V_{IL} | Hi-Z | Data Input | Active (I_{CC}) |
| Word Read | V_{IL} | V_{IH} | V_{IL} | V_{IL} | V_{IL} | Data Output | Data Output | Active (I_{CC}) |
| Word Write | V_{IL} | V_{IL} | X | V_{IL} | V_{IL} | Data Input | Data Input | Active (I_{CC}) |

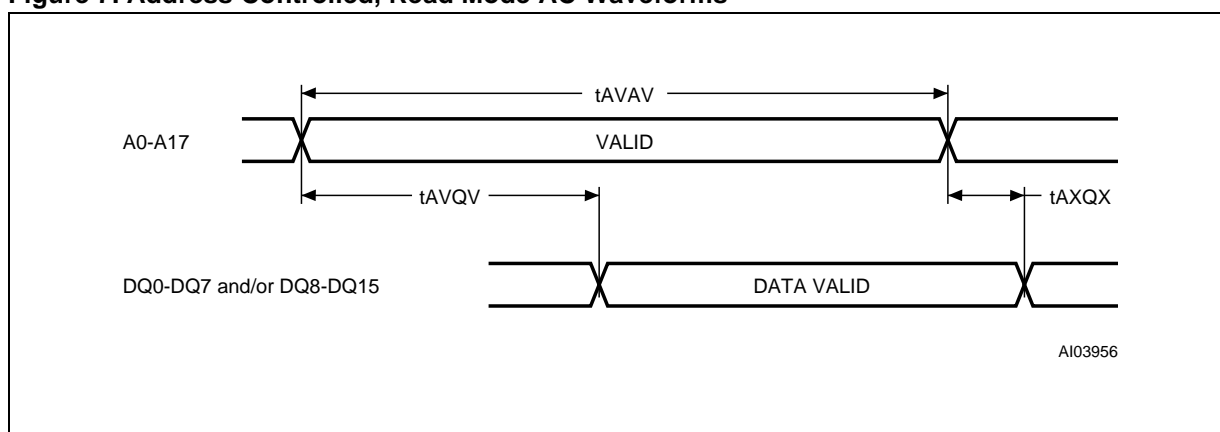
X = V_{IH} or V_{IL} .

Read Mode

The M68AR256ML is in the Read mode whenever Write Enable (\overline{W}) is High with Output Enable (\overline{G}) Low, and Chip Enables (\overline{E}) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal UB and LB, of the 4,194,304 locations in the static memory array, specified by the 18 address inputs. Valid data will be available at the eight or sixteen output pins

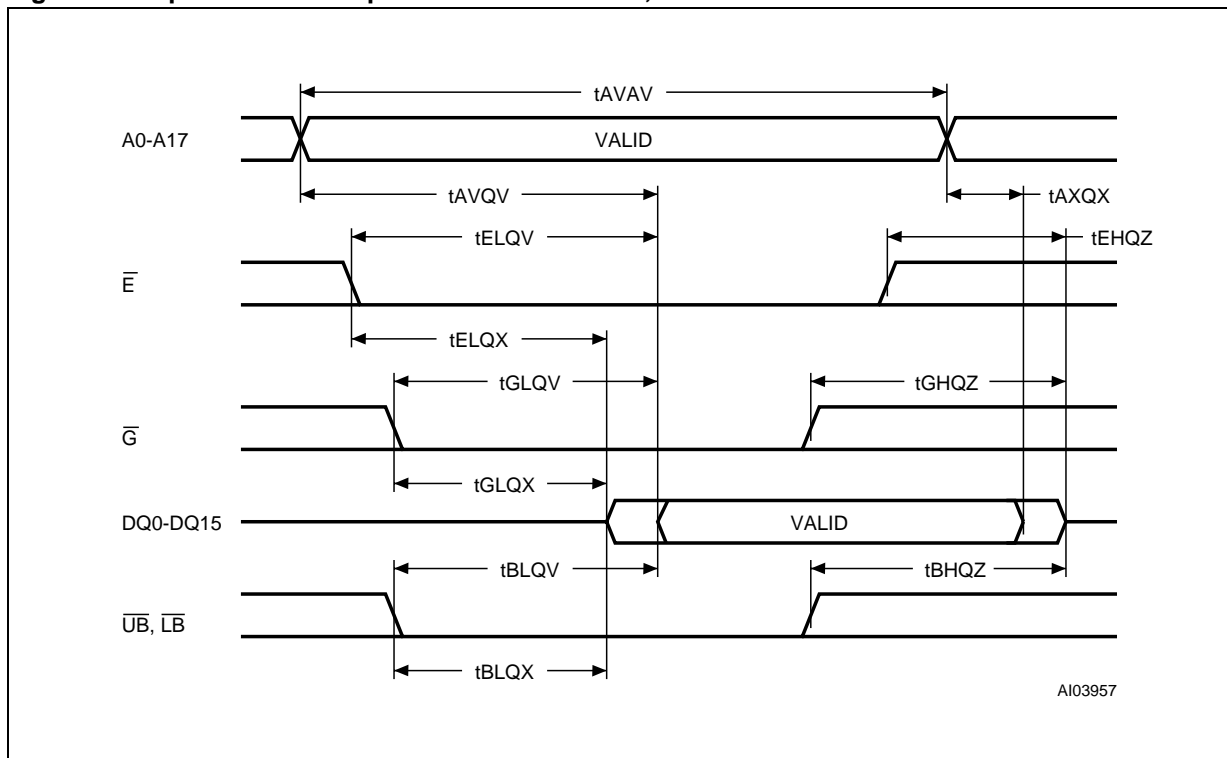
within t_{AVQV} after the last stable address, providing \overline{G} is Low and \overline{E} is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} , t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} , t_{BLQX} and t_{GLQX} , but data lines will always be valid at t_{AVQV} .

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: \overline{E} = Low, \overline{G} = Low, \overline{W} = High, \overline{UB} = Low and/or \overline{LB} = Low.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable (\bar{W}) = High.

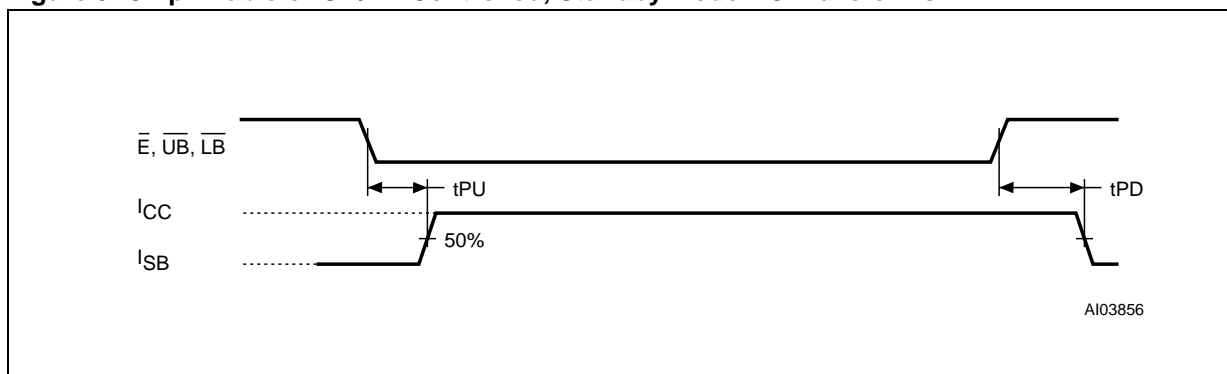
Figure 9. Chip Enable or \bar{UB}/\bar{LB} Controlled, Standby Mode AC Waveforms

Table 7. Read and Standby Mode AC Characteristics

| Symbol | Parameter | | M68AR256ML | | Unit |
|------------------------------------|---|-----|------------|----|------|
| | | | 55 | 70 | |
| t _{AVAV} | Read Cycle Time | Min | 55 | 70 | ns |
| t _{AVQV} | Address Valid to Output Valid | Max | 55 | 70 | ns |
| t _{AXQX} ⁽¹⁾ | Data hold from address change | Min | 5 | 5 | ns |
| t _{BHQZ} ^(2,3) | Upper/Lower Byte Enable High to Output Hi-Z | Max | 20 | 25 | ns |
| t _{BLQV} | Upper/Lower Byte Enable Low to Output Valid | Max | 55 | 70 | ns |
| t _{BLQX} ⁽¹⁾ | Upper/Lower Byte Enable Low to Output Transition | Min | 5 | 5 | ns |
| t _{EHQZ} ^(2,3) | Chip Enable High to Output Hi-Z | Max | 20 | 25 | ns |
| t _{ELQV} | Chip Enable Low to Output Valid | Max | 55 | 70 | ns |
| t _{ELQX} ⁽¹⁾ | Chip Enable Low to Output Transition | Min | 5 | 5 | ns |
| t _{GHQZ} ^(2,3) | Output Enable High to Output Hi-Z | Max | 20 | 25 | ns |
| t _{GLQV} | Output Enable Low to Output Valid | Max | 25 | 35 | ns |
| t _{GLQX} ⁽²⁾ | Output Enable Low to Output Transition | Min | 5 | 5 | ns |
| t _{PD} ⁽⁴⁾ | Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down | Max | 0 | 0 | ns |
| t _{PU} ⁽⁴⁾ | Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up | Min | 55 | 70 | ns |

- Note: 1. Test conditions assume transition timing reference level = 0.3V_{CC} or 0.7V_{CC}.
 2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
 3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
 4. Tested initially and after any design or process changes that may affect these parameters.

Write Mode

The M68AR256ML is in the Write mode whenever the \overline{W} and \overline{E} are Low. Either the Chip Enable input (\overline{E}) or the Write Enable input (\overline{W}) must be deasserted during Address transitions for subsequent write cycles. When \overline{E} (\overline{W}) is Low, and \overline{UB} or \overline{LB} is Low, write cycle begins on the \overline{W} (\overline{E})'s falling edge. When \overline{E} and \overline{W} are Low, and $\overline{UB} = \overline{LB} = \text{High}$, write cycle begins on the first falling edge of \overline{UB} or \overline{LB} . Therefore, address setup time is referenced to Write Enable, Chip Enable or $\overline{UB}/\overline{LB}$ as t_{AVWL} , t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of \overline{E} , \overline{W} or $\overline{UB}/\overline{LB}$.

If the Output is enabled ($\overline{E} = \text{Low}$, $\overline{G} = \text{Low}$, \overline{LB} or $\overline{UB} = \text{Low}$), then \overline{W} will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVBH} before the rising edge of $\overline{UB}/\overline{LB}$ whichever occurs first, and remain valid for t_{WHDX} , t_{EHDX} and t_{BHDX} respectively.

Figure 10. Write Enable Controlled, Write AC Waveforms

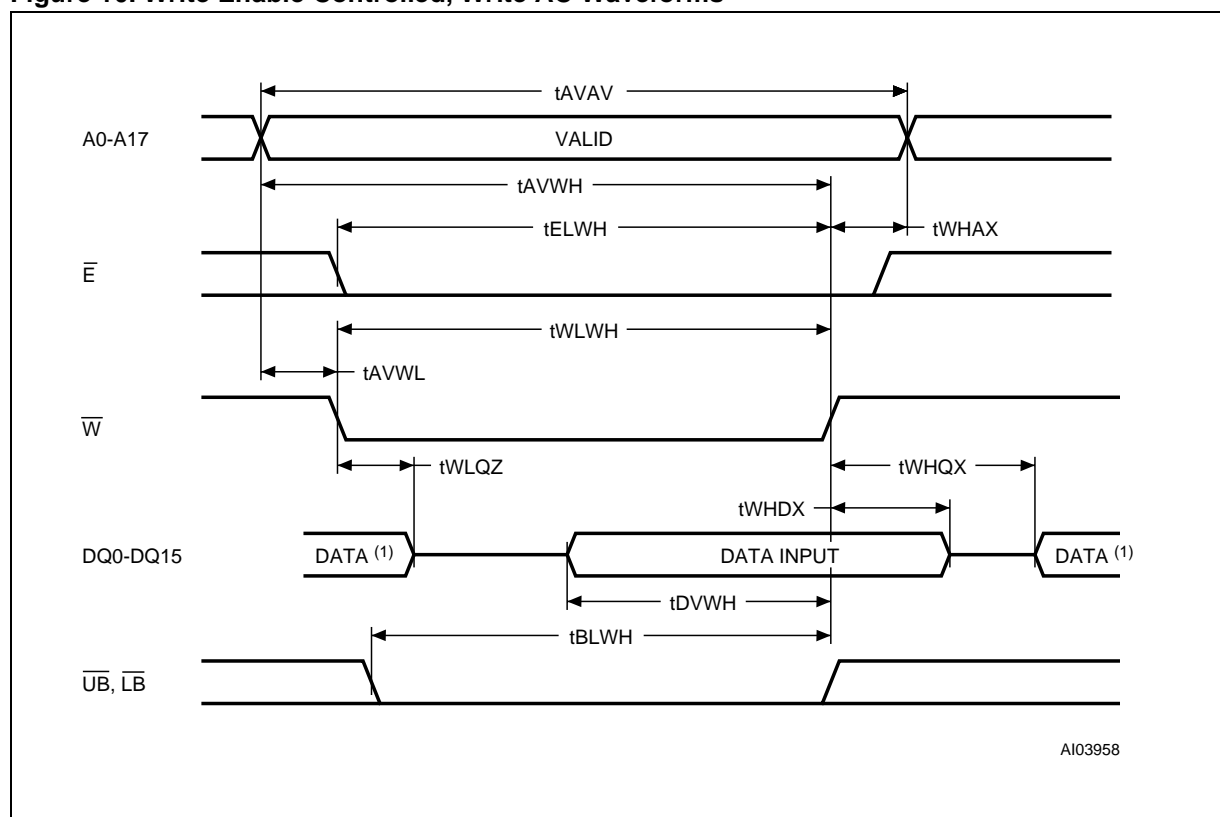


Figure 11. Chip Enable Controlled, Write AC Waveforms

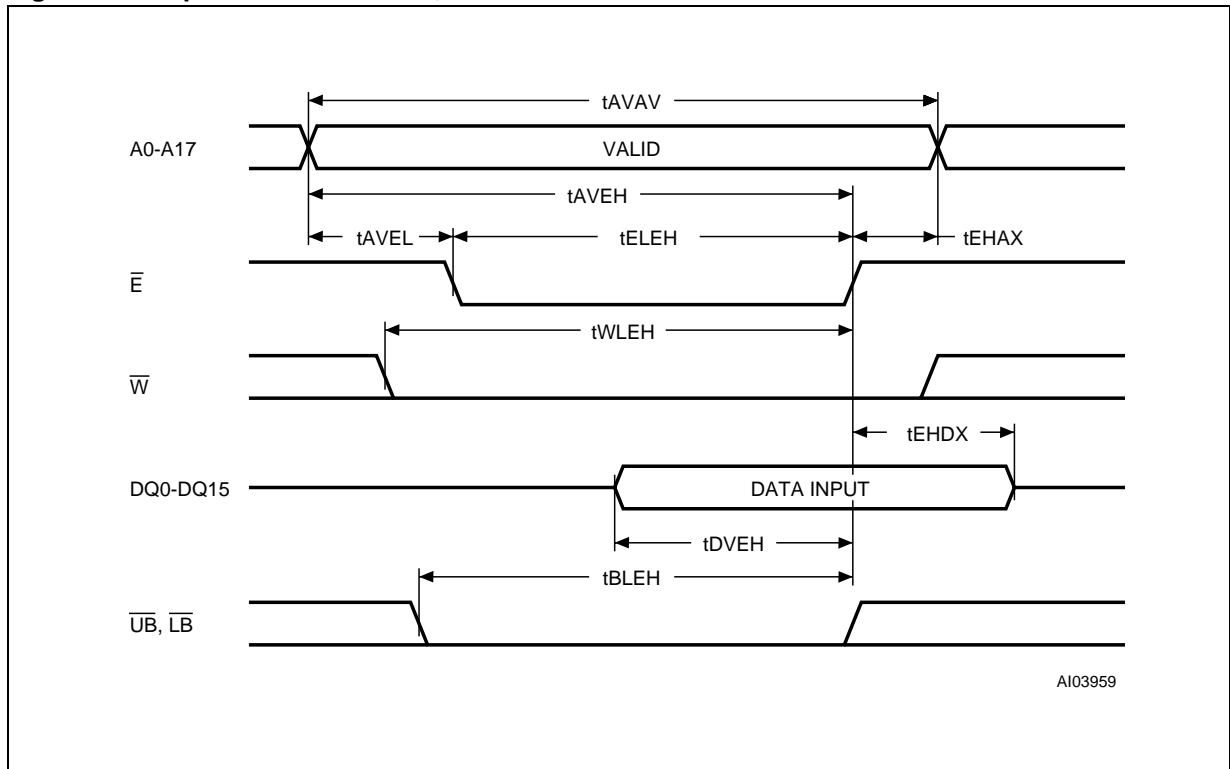
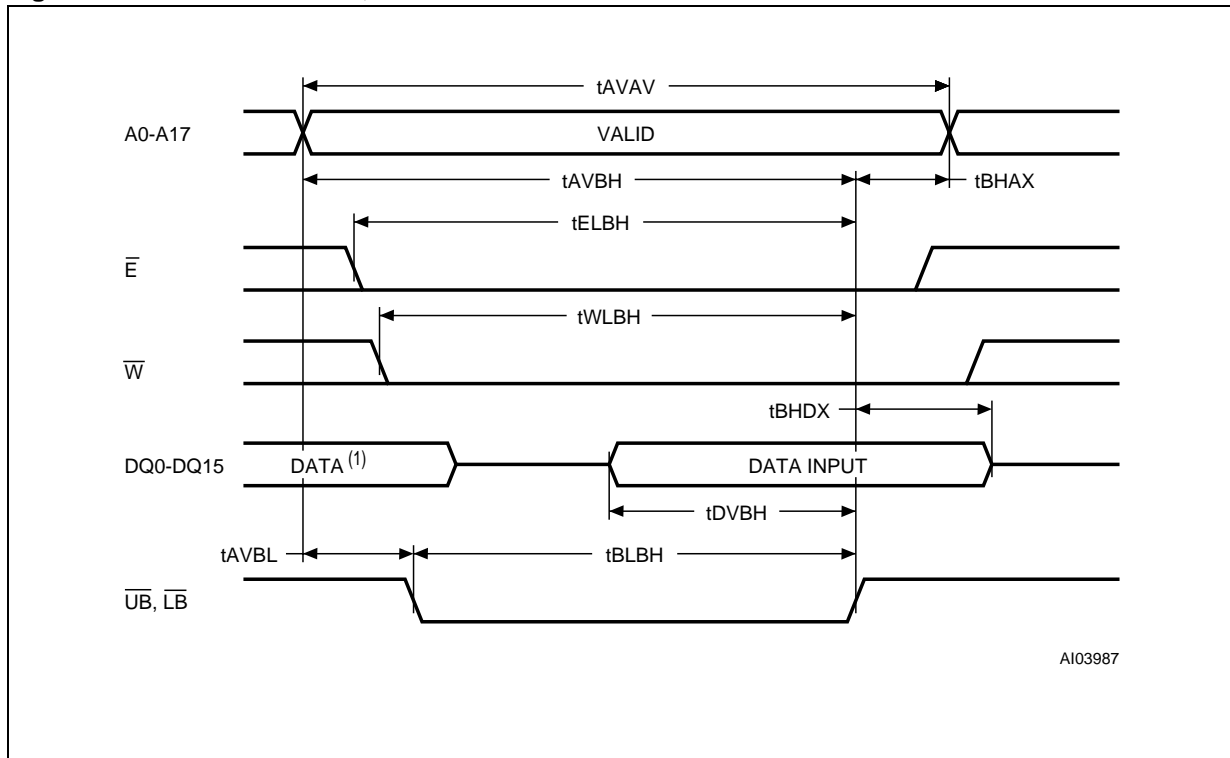


Figure 12. \bar{UB}/\bar{LB} Controlled, Write AC Waveforms



Note: 1. During this period $DQ0-DQ15$ are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

| Symbol | Parameter | | M68AR256ML | | Unit |
|------------------------------------|---|-----|------------|----|------|
| | | | 55 | 70 | |
| t _{AVAV} | Write Cycle Time | Min | 55 | 70 | ns |
| t _{AVBH} | Address Valid to \overline{LB} , \overline{UB} High | Min | 45 | 60 | ns |
| t _{AVBL} | Address Valid to \overline{LB} , \overline{UB} Low | Min | 0 | 0 | ns |
| t _{AVEH} | Address Valid to Chip Enable High | Min | 45 | 60 | ns |
| t _{AVEL} | Address valid to Chip Enable Low | Min | 0 | 0 | ns |
| t _{AVWH} | Address Valid to Write Enable High | Min | 45 | 60 | ns |
| t _{AVWL} | Address Valid to Write Enable Low | Min | 0 | 0 | ns |
| t _{BHAX} | \overline{LB} , \overline{UB} High to Address Transition | Min | 0 | 0 | ns |
| t _{BHDX} | \overline{LB} , \overline{UB} High to Input Transition | Min | 0 | 0 | ns |
| t _{BLBH} | \overline{LB} , \overline{UB} Low to \overline{LB} , \overline{UB} High | Min | 45 | 60 | ns |
| t _{BLEH} | \overline{LB} , \overline{UB} Low to Chip Enable High | Min | 45 | 60 | ns |
| t _{BLWH} | \overline{LB} , \overline{UB} Low to Write Enable High | Min | 45 | 60 | ns |
| t _{DVBH} | Input Valid to \overline{LB} , \overline{UB} High | Min | 25 | 30 | ns |
| t _{DVEH} | Input Valid to Chip Enable High | Min | 25 | 30 | ns |
| t _{DVWH} | Input Valid to Write Enable High | Min | 25 | 30 | ns |
| t _{EHAX} | Chip Enable High to Address Transition | Min | 0 | 0 | ns |
| t _{EHDX} | Chip enable High to Input Transition | Min | 0 | 0 | ns |
| t _{ELBH} | Chip Enable Low to \overline{LB} , \overline{UB} High | Min | 45 | 60 | ns |
| t _{ELEH} | Chip Enable Low to Chip Enable High | Min | 45 | 60 | ns |
| t _{ELWH} | Chip Enable Low to Write Enable High | Min | 45 | 60 | ns |
| t _{WHAX} | Write Enable High to Address Transition | Min | 0 | 0 | ns |
| t _{WHDX} | Write Enable High to Input Transition | Min | 0 | 0 | ns |
| t _{WHQX} ⁽¹⁾ | Write Enable High to Output Transition | Min | 5 | 5 | ns |
| t _{WLBH} | Write Enable Low to \overline{LB} , \overline{UB} High | Min | 45 | 60 | ns |
| t _{WLEH} | Write Enable Low to Chip Enable High | Min | 45 | 60 | ns |
| t _{WLQZ} ^(1,2) | Write Enable Low to Output Hi-Z | Max | 20 | 20 | ns |
| t _{WLWH} | Write Enable Low to Write Enable High | Min | 45 | 60 | ns |

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.

2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 13. Low V_{CC} Data Retention AC Waveforms

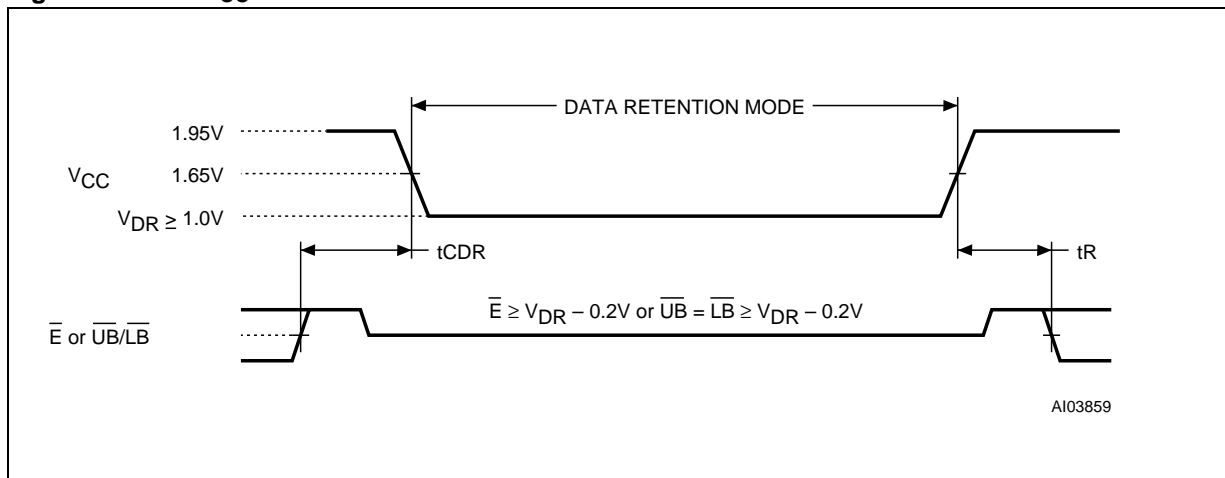


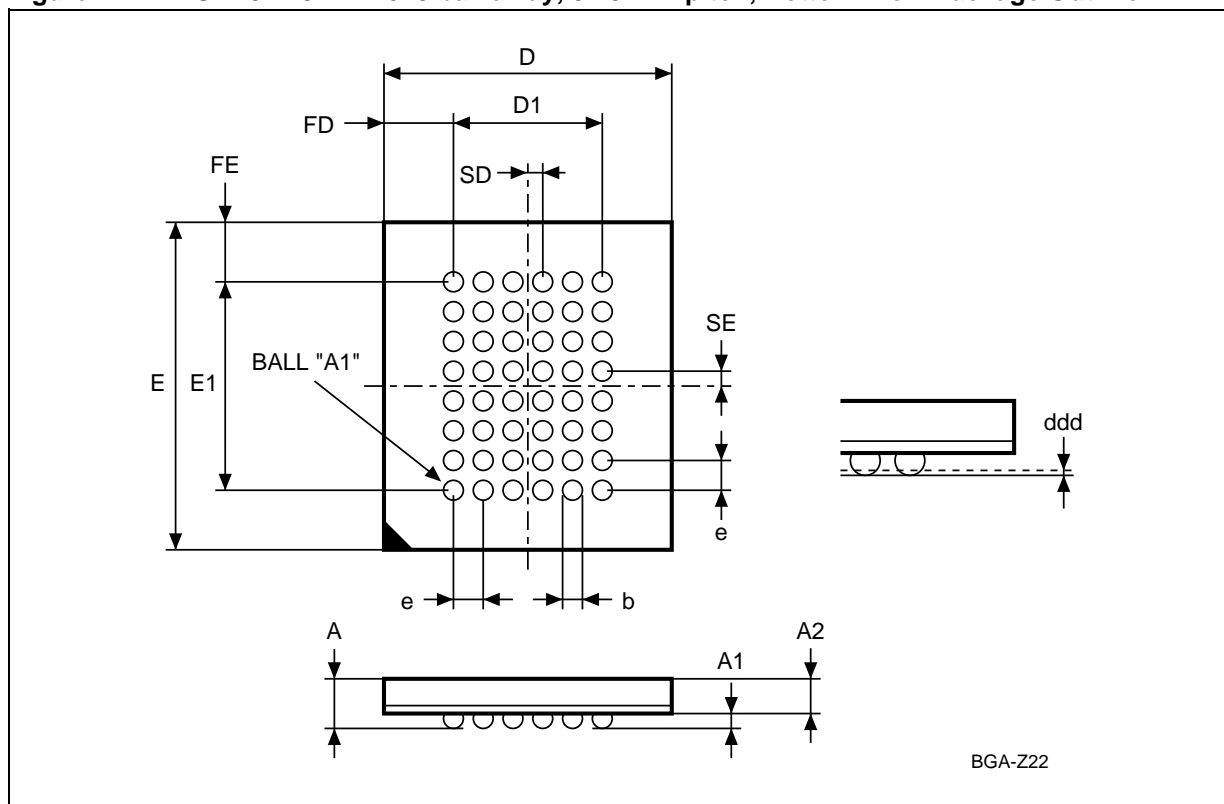
Table 9. Low V_{CC} Data Retention Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|--|--|-------------------|-----|-----|------|
| I _{CCDR} ⁽¹⁾ | Supply Current (Data Retention) | V _{CC} = 1.0V, $\bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V, f = 0$ ⁽³⁾ | | 0.5 | 3 | μA |
| t _{CDR} ^(1,2) | Chip Deselected to Data Retention Time | | 0 | | | ns |
| t _R ⁽²⁾ | Operation Recovery Time | | t _{AVAV} | | | ns |
| V _{DR} ⁽¹⁾ | Supply Voltage (Data Retention) | $\bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V, f = 0$ | 1.0 | | | V |

Note: 1. All other Inputs at V_{IH} ≥ V_{CC} - 0.2V or V_{IL} ≤ 0.2V.
 2. Tested initially and after any design or process changes that may affect these parameters. t_{AVAV} is Read cycle time.
 3. No input may exceed V_{CC} + 0.2V.

PACKAGE MECHANICAL

Figure 14. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

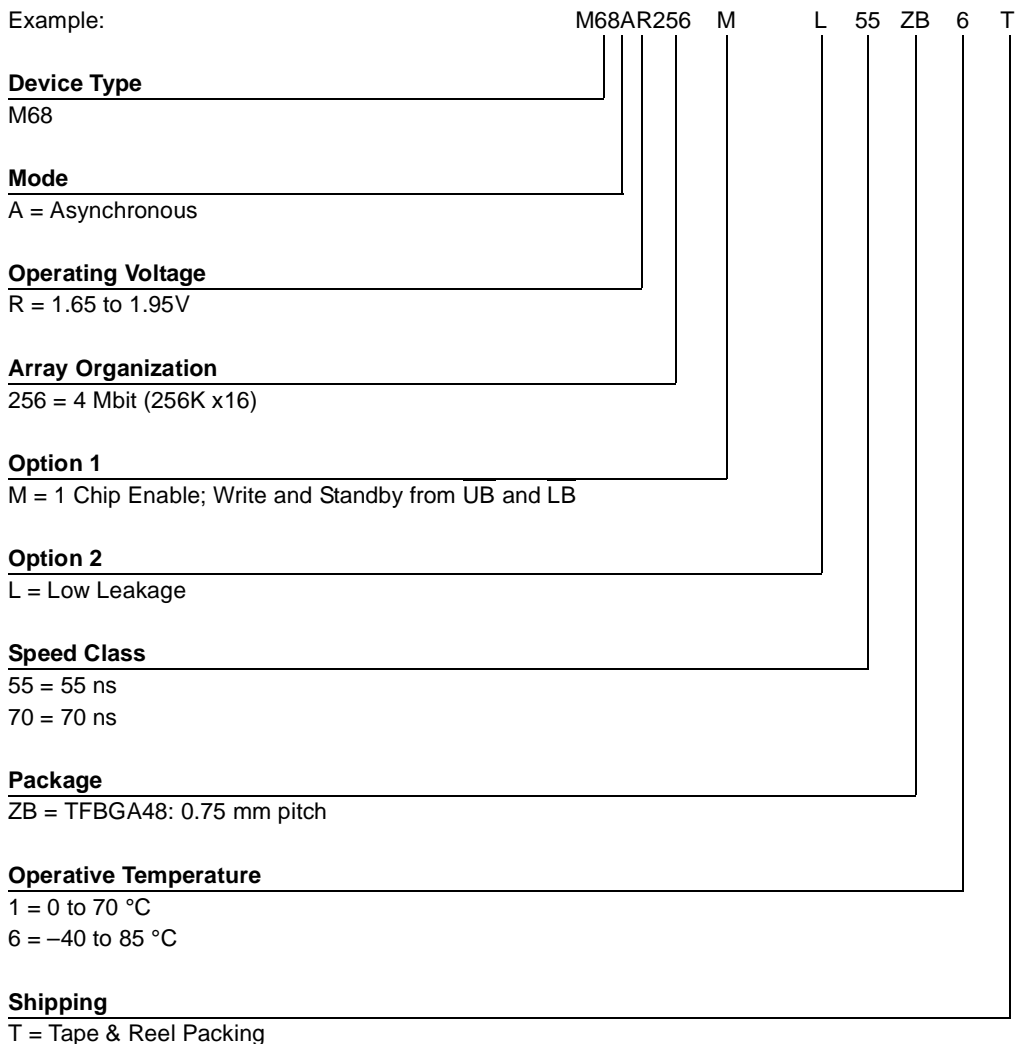
Table 10. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.260 | | | 0.0102 | |
| A2 | | | 0.900 | | | 0.0354 |
| b | | 0.350 | 0.450 | | 0.0138 | 0.0177 |
| D | 7.000 | 6.900 | 7.100 | 0.2756 | 0.2717 | 0.2795 |
| D1 | 3.750 | – | – | 0.1476 | – | – |
| ddd | | | 0.100 | | | 0.0039 |
| E | 8.000 | 7.900 | 8.100 | 0.3150 | 0.3110 | 0.3189 |
| E1 | 5.250 | – | – | 0.2067 | – | – |
| e | 0.750 | – | – | 0.0295 | – | – |
| FD | 1.625 | – | – | 0.0640 | – | – |
| FE | 1.375 | – | – | 0.0541 | – | – |
| SD | 0.375 | – | – | 0.0148 | – | – |
| SE | 0.375 | – | – | 0.0148 | – | – |

M68AR256ML

PART NUMBERING

Table 11. Ordering Information Scheme



For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

| Date | Version | Revision Details |
|-------------|---------|-------------------------------------|
| July 2001 | -01 | First Issue |
| 23-Oct-2001 | -02 | Speed class changed from 80 to 70ns |
| 20-May-2002 | -03 | Document globally revised |

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