Document Title

256K x 16bit 2.7 ~ 3.6V Super low Power FCMOS Slow SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Dec.26.2001	Preliminary
0.1	Absolute Maximum Ratings - Vcc changed -0.3V to 4.6V -> -0.3V to 4.0V DC Electric Characteristics - ICC changed 4mA -> 3mA - ICC1 changed 25mA at 55ns -> 20mA at 55ns - ICC1 changed 20mA at 70ns -> 15mA at 70ns - ICC1 changed 3mA at 1us -> 2mA at 1us AC Test Conditions - Output Load changed 5pF -> 30pF Data Retention Electric Characteristics - ICCDR changed 10uA -> 6uA Marking Information - Part Name changed HY62KF6403E -> HY62KF16403E	Nov.14.2002	Final
0.2	Add 44-Pin Padpitch to TSOPII Package Information	Dec.26.2003	Final

DESCRIPTION

The HY62KF16403E is a high speed, super low power and 4Mbit full CMOS SRAM organized as 256K words by 16bits. The HY62KF16403E uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application.
This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

FEATURES

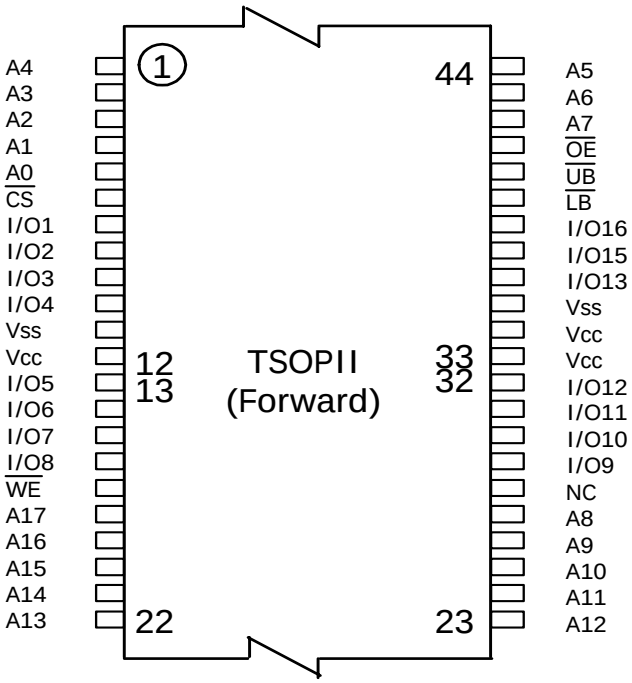
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
  - 1.2V(min) data retention
- Standard pin configuration
  - 44pin 400mil TSOP-II (Forward)

16M Pseudo SRAM PRODUCT FAMILY

Part Number	Voltage	Speed	Operation Current / Icc	Standby Current		Temp.(°C)
				SL	LL	
HY62KF16403E-I	2.7~3.6 (V)	55/70 (ns)	3mA	6uA	15uA	-40 ~ 85

Note 1) I : Industrial Temperature.
2) Current value is max.

PIN CONNECTION

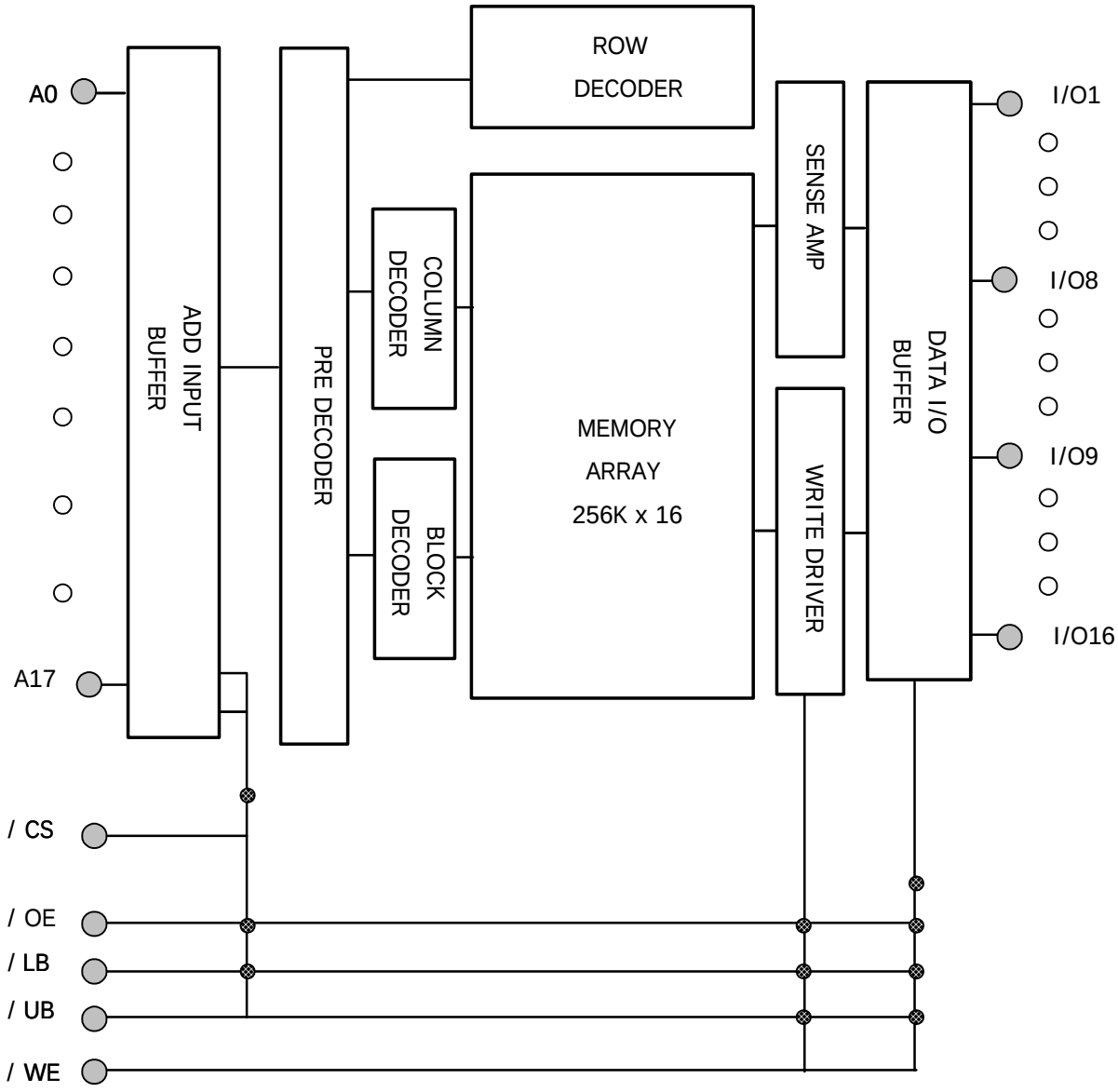


PAD DESCRIPTION

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower Byte Control (IO1~IO8)
$\overline{UB}$	Upper Byte Control (IO9~IO16)
I/O1 ~ I/O16	Data Inputs/Outputs
A0 ~ A17	Address Inputs
VDD	Power(2.7V~3.6V)
VSS	Ground
NC	No connection

FUNCTIONAL BLOCK DIAGRAM

256K x 16bit Super low Power FCMOS Slow SRAM



ORDERING INFORMATION

Part Number	Speed	Power	Temparature	Package
HY62KF16403E-SD(I)	55/70	SL-Part	I[1)]	TSOP-II
HY62KF16403E-DD(I)	55/70	LL-Part	I[1)]	TSOP-II

Note 1) I : Industrial -40 ~ 85 °C

ABSOLUTE MAXIMUM RATING[1)]

Parameter	Symbol	Rating	Unit
Input/Output Voltage	VIN, VOUT	-0.3 to VCC+0.3V	V
Power Supply	VDD	-0.3 to 4.0	V
Ambient Temperature	TA	-40 to 85	°C
Storage Temperature	TSTG	-55 to 150	°C
Power Dissipation	PD	1.0	W
Ball Soldering Temperature & Time	TSOLDER	260 · 10	°C · Sec

Note1) Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied.
Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O		POWER
						I/O1 ~ I/O8	I/O9 ~ I/O16	
Deselected	H	X	X	X	X	High-Z	High-Z	Standby
Output Disabled	L	X	X	H	H	High-Z	High-Z	Active
	L	H	H	X	X	High-Z	High-Z	
Read	L	H	L	L	H	DOUT	High-Z	Active
				H	L	High-Z	DOUT	
				L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	Active
				H	L	High-Z	DIN	
				L	L	DIN	DIN	

Note 1). H=VIH, L=VIL, X=Don't Care(VIL or VIH)
2). $\overline{UB}$, $\overline{LB}$(Upper, Lower Byte enable)
These active LOW inputs allow individual bytes to be written or read.
When $\overline{LB}$ is LOW, data is written or read to the lower byte, I/O1 - I/O8.
When $\overline{UB}$ is LOW, data is written or read to the upper byte, I/O9 - I/O16.

DC OPERATING CONDITION (T_A= -40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	2.7	3.0 or 3.3	3.6	V
Gruond	V_{SS}	0	-	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3[1)]	-	0.6	V

Note : 1) V_{IL}=-1.5V for Pulse Width less then 30ns.
Undershoot is sampled, not 100% tested.

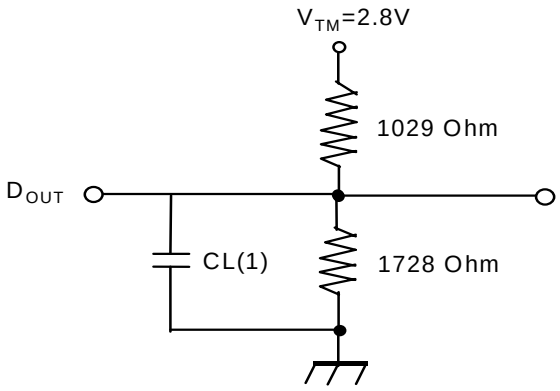
DC CHARACTERISTICS (V_{DD}= 2.7V ~ 3.6V, T_A= -40 to 85°C)

Parameter	Symbol	Test Condition		Speed			Unit
				Min	Tpy.	Max	
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{CC}$		-1		1	uA
Output Leakage Current	I_{LO}	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}		-1		1	
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0mA		-		3	mA
Average Operating Current	I_{CC1}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, Cycle Time= min. 100% Duty, $I_{I/O}$=0mA	55ns			20	
			70ns			15	
		$\overline{CS} \le$ 0.2V, $V_{IN} \le$ 0.2V or V_{CC}-0.2V $\le V_{IN}$, Cycle Time=1us. 100% Duty, $I_{I/O}$=0mA		-		2	
TTL Standby Current	I_{SB}	$\overline{CS}$=V_{IH}, V_{IN}=V_{IH} or V_{IL}		-		300	uA
Standby Current (CMOS Input)	I_{SB1}	V_{CC}-0.2V $\le \overline{CS}$, V_{CC}-0.2V $\le V_{IN}$ or $V_{IN} \le V_{SS}$+0.2V	3.0 ~ 3.6 V	-	0.2	6	
				-	0.2	15	
			2.7 ~ 3.3 V	-	0.2	6	
				-	0.2	12	
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= -1.0mA		2.4	-	-	V

AC OPERATING TEST CONDITION (TA= -40 to 85 °C)

Parameter		Value
Input Pulse Level		0.4 to 2.2V
Input Rising and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, tOW	CL = 30pF + 1TTL Load
	Others	CL = 30pF + 1TTL Load

AC TEST LOADS



Note 1) Including jig and scope capacitance.

CAPACITANCE (Temp.= 25 °C, f=1.0MHz)

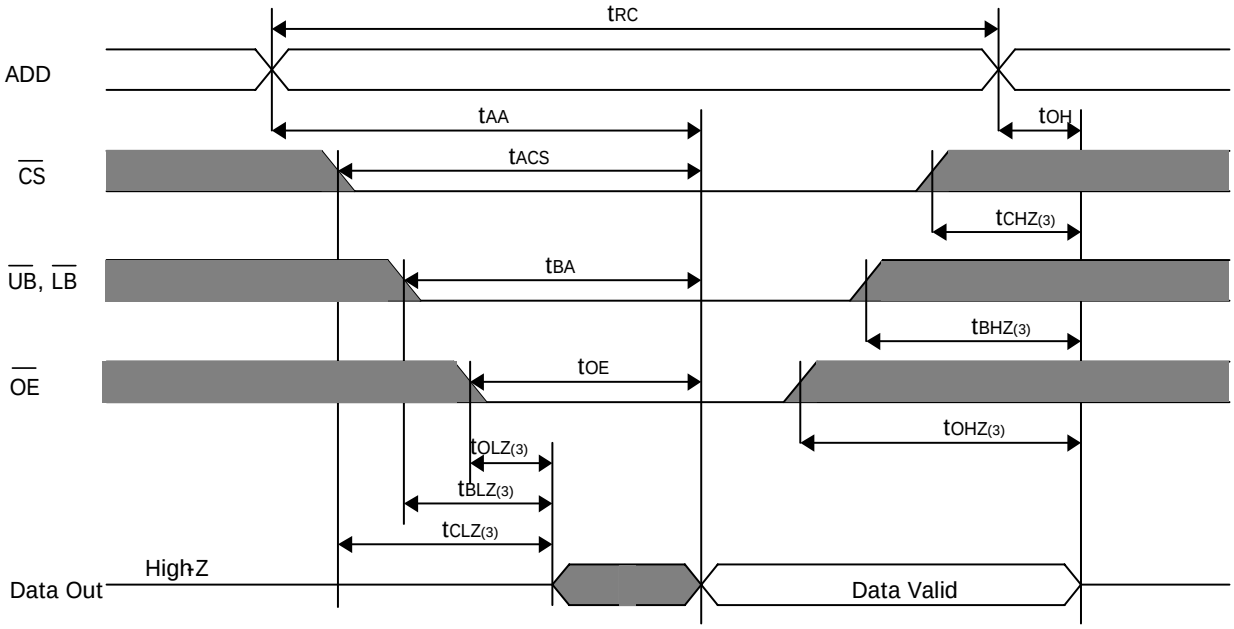
Parameter	Symbol	Condition	Max.	Unit
Input Capacitance (Add, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	CIN	VIN = 0V	8	pF
Output Capacitance (I/O)	COUT	VI/O = 0V	10	pF

Note : These parameters are sampled and not 100% tested.

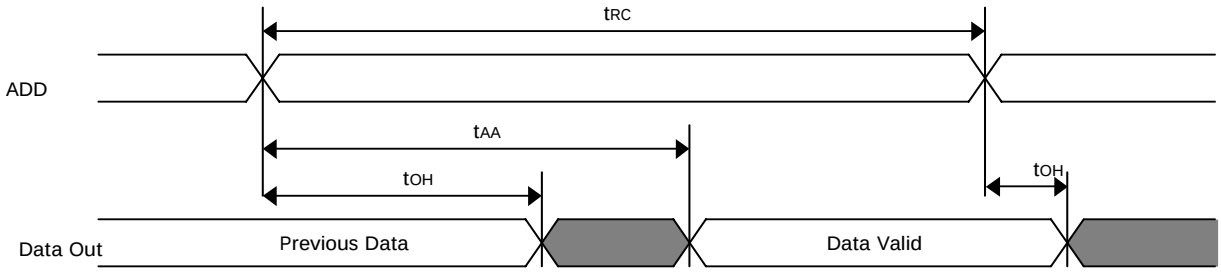
AC CHARACTERISTICS (AC operating conditions unless otherwise specified)

Parameter	Symbol	55ns		75ns		Unit
		Min	Max	Min	Max	
Read Cycle						
Read Cycle Time	tRC	55	-	75	-	ns
Address Access Time	tAA	-	55	-	75	ns
Chip Select Access Time	tACS	-	55	-	75	ns
Output Enable to Output Valid	tOE	-	30	-	35	ns
$\overline{LB}$, $\overline{UB}$ Access Time	tBA	-	55	-	75	ns
Chip Select to Output in Low Z	tCLZ	10	-	10	-	ns
Output Enable to Output in Low Z	tOLZ	5	-	5	-	ns
$\overline{LB}$, $\overline{UB}$ Enable to Output in Low Z	tBLZ	10	-	10	-	ns
Chip Disable to Output in High Z	tCHZ	0	20	0	25	ns
Out Disable to Output in High Z	tOHZ	0	20	0	25	ns
$\overline{LB}$, $\overline{UB}$ Disable to Output in High Z	tBHZ	0	20	0	25	ns
Output Hold from Address Change	tOH	10	-	10	-	ns
Write Cycle						
Write Cycle Time	tWC	55	-	75	-	ns
Chip Selection to End of Write	tCW	50	-	60	-	ns
Address Valid to End of Write	tAW	50	-	60	-	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	tBW	50	-	60	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Write Pulse Width	tWP	45	-	50	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output in High Z	tWHZ	0	20	0	20	ns
Data to Write Time Overlap	tDW	25	-	30	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
Output Active from End of Write	tOW	5	-	5	-	ns

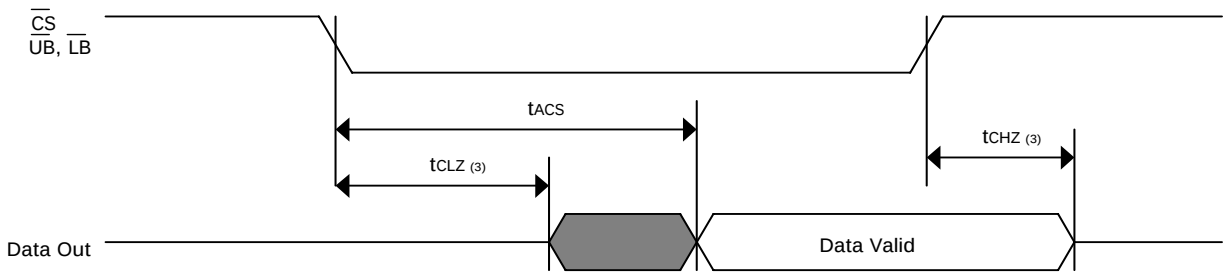
READ CYCLE 1 (Note 1, 4)



READ CYCLE 2 (Note 1, 2, 4)

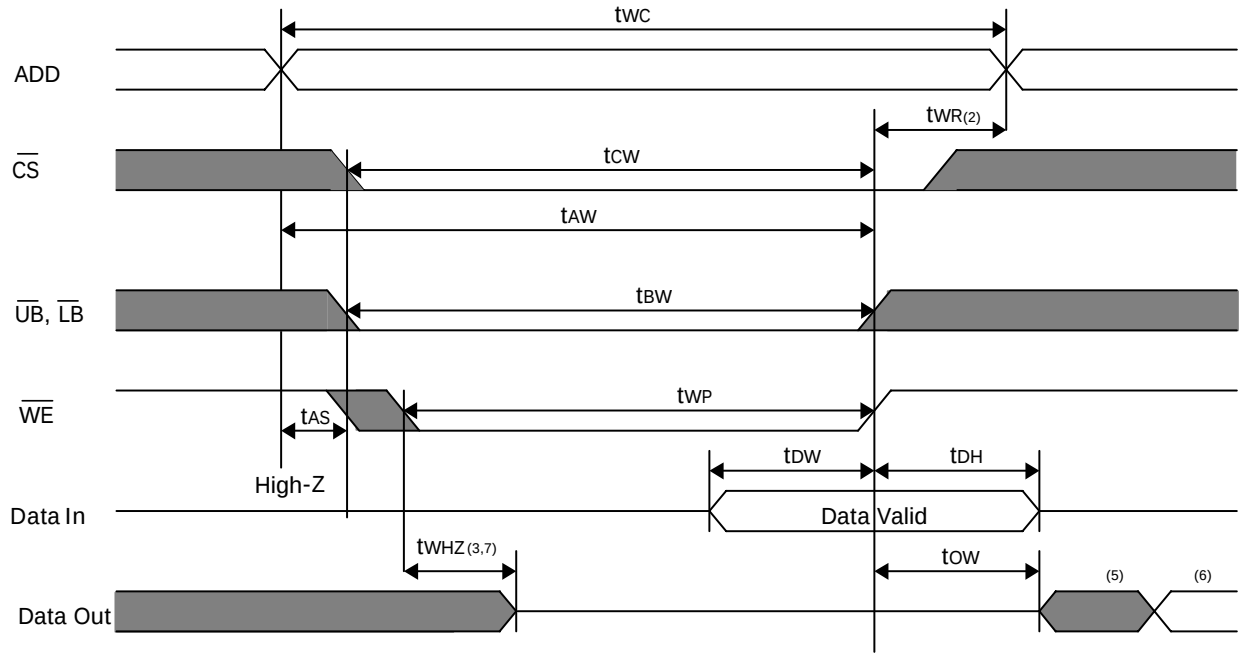


READ CYCLE 3 (Note 1, 2, 4)

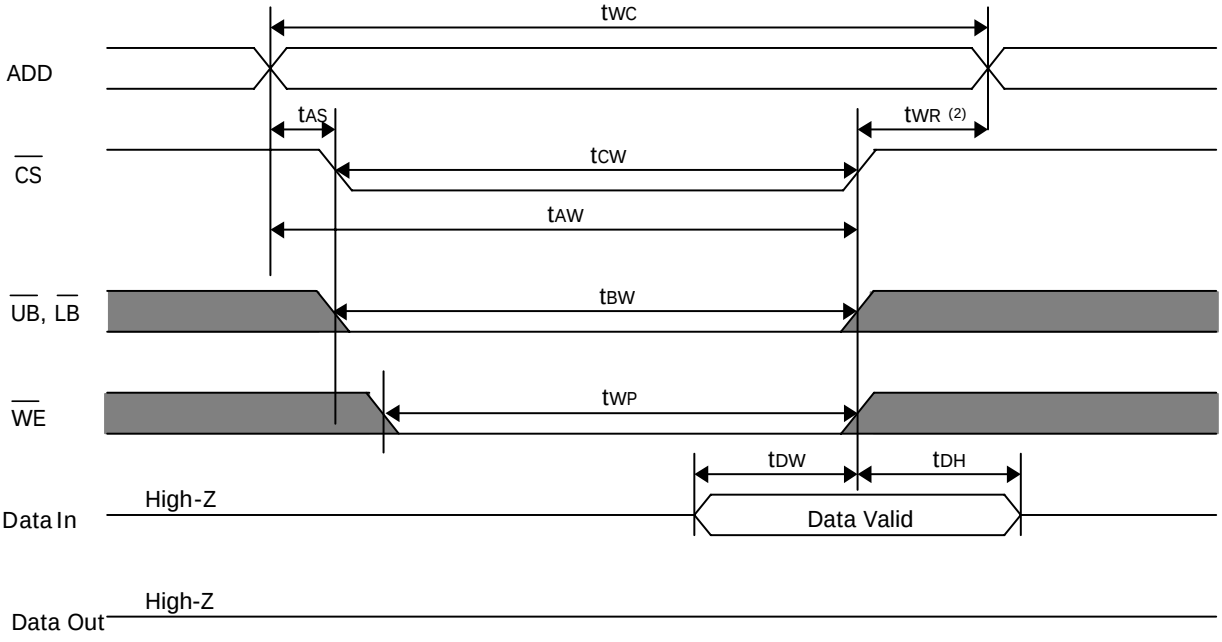


Notes : 1. A read occurs during the overlap of a low $\overline{OE}$, a high $\overline{WE}$, a low $\overline{CS}$ and $\overline{UB}$ and /or $\overline{LB}$.
2. $\overline{OE}$ = V_{IL}
3. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
4. $\overline{CS}$ in high for the standby, low for active.
$\overline{UB}$ and $\overline{LB}$ in high for the standby, low for active.

WRITE CYCLE 1 (Note 1, 4, 8) ($\overline{WE}$ Controlled)



WRITE CYCLE 2 (Note 1, 4, 8) ($\overline{CS}$ Controlled)



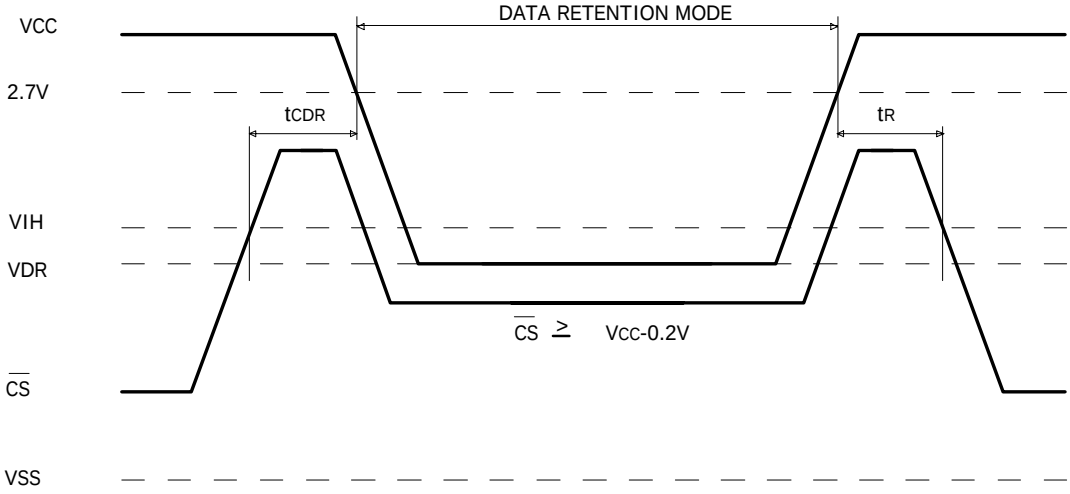
Notes : 1. A write occurs during the overlap of a low $\overline{WE}$, a low $\overline{CS}$ and a low $\overline{UB}$ and/or $\overline{LB}$.
2. tWR is measured from the earlier of $\overline{CS}$, $\overline{LB}$, UB, or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$, $\overline{LB}$ and $\overline{UB}$ low transition occur simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. Q(data out) is the invalid data.
6. Q(data out) is the read data of the next address.
7. $\overline{CS}$ in high for the standby, low for active $\overline{UB}$ and $\overline{LB}$ in high for the standby, low for active.

DATA RETENTION ELECTRIC CHARACTERISTIC (T_A= -40 to 85 ^oC)

Symbol	Parameter	Test Condition		Min	Typ.[1)]	Max	Unit
V_{DR}	Vcc for Data Retention	V_{CC}-0.2V ≤ $\overline{CS}$, V_{CC}-0.2V ≤ V_{IN} or V_{IN} ≤ V_{SS}+0.2V		1.2	-	3.6	V
I_{ccdr}	Data Retention Current	V_{CC}=1.5V V_{CC}-0.2V ≤ $\overline{CS}$ or V_{CC}-0.2V ≤ V_{IN} or V_{IN} ≤ V_{SS}+0.2V	SL	-	0.1	3.0	uA
			LL	-	0.1	6.0	
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
t_R	Operating Recovery Time			tRC	-	-	

Notes : 1. Typical values are under the condition of TA = 25^{o}C.
2. Typical value are sampled and not 100% tested.

DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package Forward (D)

UNIT : Inch (mm) Max / Min