FEDL9098B-01
Issue Date: Aug. 10, 2010

ML9098B

Clock IC with Static and 1/2-Duty LCD Drivers

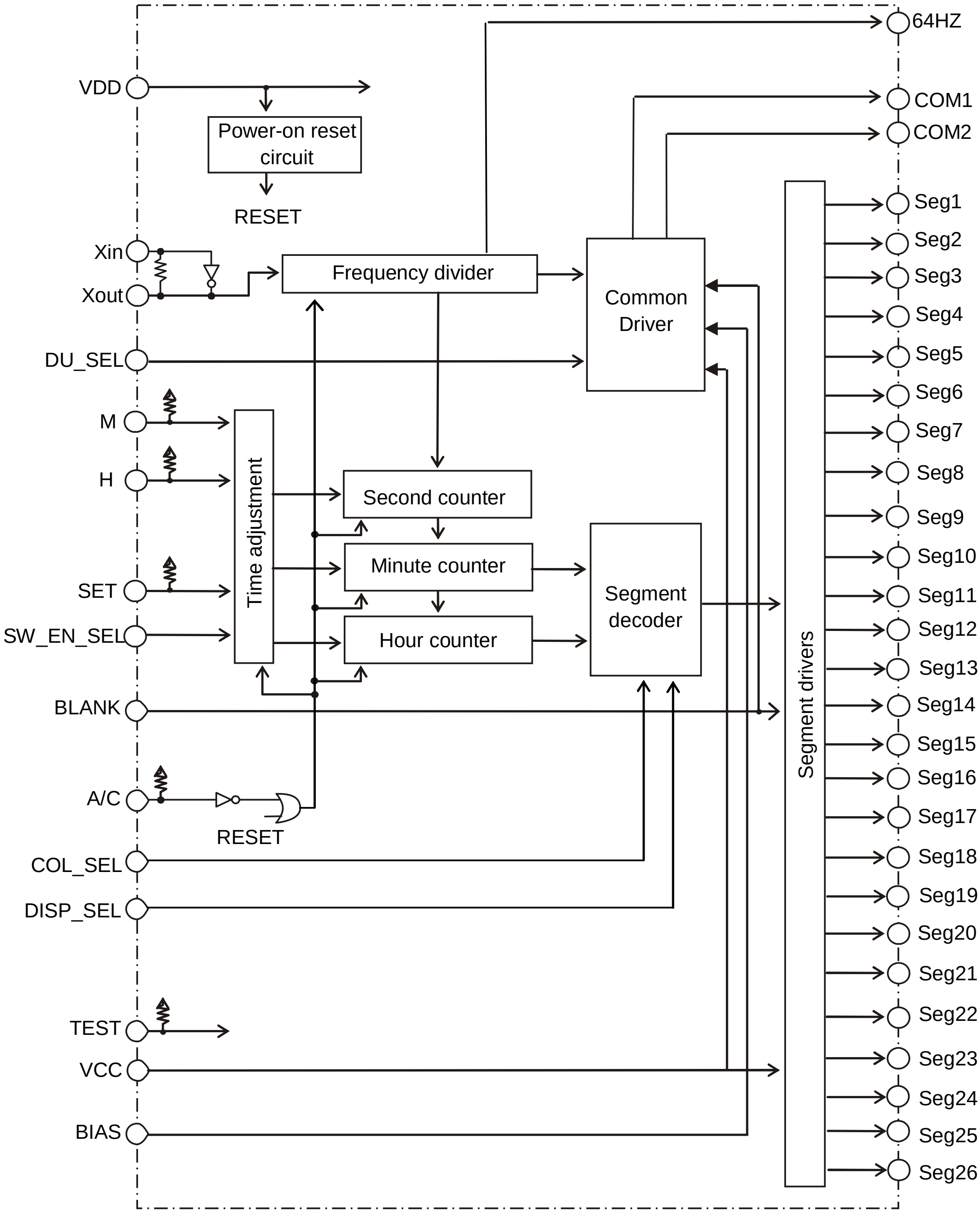
GENERAL DESCRIPTION

The ML9098B is a 24-hour/ 12-hour car clock IC that drives 1/2-duty dynamic or static LCDs. It has a wide range of power supplies using oscillation of 4.194304 MHz. The ML9098B has time adjustment functions in hour, minute, and 30-minute units.

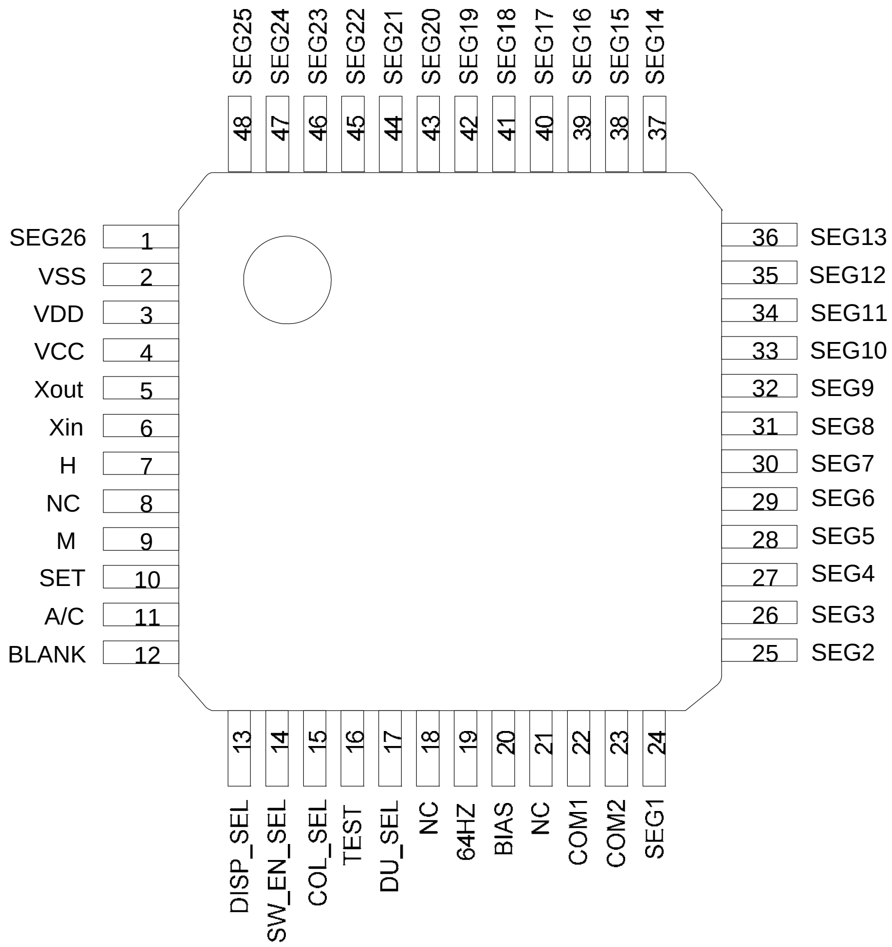
FEATURES

- 24-hour or 12-hour system
- Power supplies ranging from 3.0 to 5.5V
- Designed for 1/2-duty or static LCDs
- 4.194304MHz (crystal oscillation)
- Package:
  48-pin plasticTQFP (TQFP48-P-0707-0.50-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Pin	I/O	Pull-up/ Pull-down	Description
COM1	O	—	Output pin for LCD common driver.
COM2	O	—	Output pin for 1/2-duty mode LCD common driver.
A/C	I	Pull-up	Pin for clearing all circuits. This pin is placed normally at a "H" level with an internal pull-up resistor. The counters and frequency divider are reset when this pin goes at a “L” level.
H	I	Pull-up	Hour adjustment pin (for general areas). This pin is placed normally at a "H" level with an internal pull-up resistor. The "Hour" indication is fast forwarded at 2 Hz when this pin is low.
M	I	Pull-up	Minute adjustment pin. This pin is placed normally at a "H" level with an internal pull-up resistor. The "Minute" indication is fast forwarded at 2 Hz when this pin is low.
BLANK	I	—	Display ON/OFF pin. "L" level: Display Off, “H” level: Display On.
COL_SEL	I	—	Pin for selecting the colon output as "Flashing" or "Lighting". "L" level: Flashing, "H" level: Lighting
Xin	I	—	Crystal oscillation pins for connecting a crystal and the capacitors (Cin and Cout) externally.
Xout	O		
SET	I	Pull-up	Zero adjustment pin. This pin is placed normally at a "H" level with an internal pull-up resistor. The clock provides 30-minute adjustment when this pin is low.
64HZ	O	—	64Hz output pin
SEG1 to SEG26	O	—	Output pins from SEG1 to SEG13 are used in 1/2-duty mode. Output pins from SEG1 to SEG26 are used in static mode.
VDD	—	—	Power supply pin for the logic section.
VCC	—	—	Power supply pin for the driver section.
VSS	—	—	Ground pin.
DISP_SEL	I	—	Pin for selecting the 12-hour or 24-hour system. “H” level: 24-hour system, “L” level: 12-hour system with AM/PM display.
SW_EN_SEL	I	—	Adjustment enable pin. “L” level: The H, M, and SET pins are disabled. “H” level: The H, M, and SET pins are enabled.
DU_SEL	I	—	Duty select pin. "H" level: 1/2-duty dynamic mode, "L" level: Static mode.
BIAS	—	—	Supply voltage pin for the middle level voltage of the common outputs. In the static display mode, this pin should be open.
NC	—	—	No connection.
TEST	I	Pull-up	IC testing pin. This pin is placed normally at a "H" level with an internal pull-up resistor. Leave this pin open or fix it to a “H” level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (Drivers)	VCC	Ta = 25°C	–0.3 to +6.5	V
Power supply voltage (Logic circuitry)	VDD	Ta = 25°C	–0.3 to +6.5	V
Power supply voltage (Drivers & logic circuitry)	VSS	Ta = 25°C	0	V
Input voltage (Logic circuitry)	V_I	Ta = 25°C	–0.3 to VDD+0.3	V
Output voltage (Drivers)	V_{DO}	Ta = 25°C	–0.3 to VCC+0.3	V
Output voltage (Logic circuitry)	V_{LO}	Ta = 25°C	–0.3 to VDD+0.3	V
Output current (Drivers)	I_{DO}	Ta = 25°C	–5 to +5	mA
Output current (Logic circuitry)	I_{LO}	Ta = 25°C	–5 to +5	mA
Power dissipation	P_D	Ta ≤ 105°C	416	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

* VDD=VCC

RECOMMENDED OPERATING CONDITIONS

VSS = 0V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (Drivers & logic circuitry)	VCC & VDD	—	3.0	—	5.5	V
Operating temperature	Ta	—	–40	—	105	°C
Crystal frequency	f(Xtal)	—	4.194304			MHz

* VDD = VCC

ELECTRICAL CHARACTERISTICS

DC Characteristics

(VCC = VDD=3.0 to 5.5 V, Ta = –40 to +105°C)

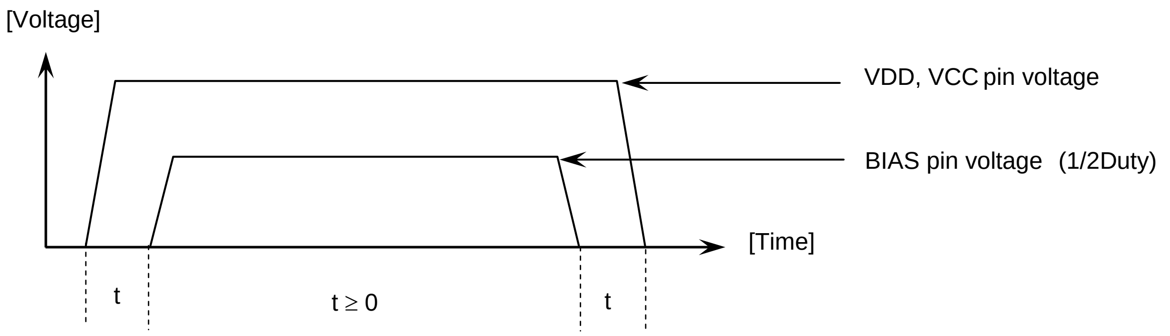
Parameter	Applicable pin	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	*1)	V_{IH}	VDD = 3.0 to 5.5 V	VDD×0.8	—	—	V
"L" input voltage	*1)	V_{IL}	VDD = 3.0 to 5.5 V	—	—	VDD×0.2	V
Input current	SET, H, M , A/C,TEST	I_{IH2}	VDD = VIN = 3.3±0.3V VDD = VIN = 5.0±0.5V	–1	—	1	μA
		I_{IL2}	VDD = 3.3±0.3V, VIN = 0 V	–200	–65	–20	μA
			VDD = 5.0±0.5V, VIN = 0 V	–400	–155	–40	
	COL_SEL, DISP_SEL, SW_EN_SEL, DU_SEL, BLANK	I_{IH3}	VDD = VIN = 3.3±0.3V VDD = VIN = 5.0±0.5V	–1	—	1	μA
		I_{IL3}	VDD = 3.3±0.3V, VIN = 0 V VDD = 5.0±0.5V, VIN = 0 V	–1	—	1	μA
Output voltage	COM output voltage	V_{OCH}	VCC = 3.3 V, BIAS = 1.65 V, VSS = 0 V, IO = –150 μA	3.1	—	—	V
			VCC = 5.0 V, BIAS = 2.5 V, VSS = 0 V, IO = –150 μA	4.8	—	—	V
		V_{OCM}	VCC = 3.3 V, BIAS = 1.65 V, VSS = 0 V, IO = ±150 μA	1.45	—	1.85	V
			VCC = 5.0 V, BIAS = 2.5 V, VSS = 0 V, IO = ±150 μA	2.3	—	2.7	V
		V_{OCL}	VCC = 3.3 V, BIAS = 1.65 V, VSS = 0 V, IO = 150 μA	—	—	0.2	V
			VCC = 5.0 V, BIAS = 2.5 V, VSS = 0 V, IO = 150 μA	—	—	0.2	V
	SEG output voltage	V_{OSH}	VCC = 3.3 V, BIAS = 1.65 V, VSS = 0 V, IO = –30 μA	3.1	—	—	V
			VCC = 5.0 V, BIAS = 2.5 V, VSS = 0 V, IO = –30 μA	4.8	—	—	V
		V_{OSL}	VCC = 3.3 V, BIAS = 1.65 V, VSS = 0 V, IO = +30 μA	—	—	0.2	V
			VCC = 5.0 V, BIAS = 2.5 V, VSS = 0 V, IO = +30 μA	—	—	0.2	V
	64HZ	V_{OH}	VDD = 3.3V, IOH = –0.1mA VDD = 5.0V, IOH = –0.1mA	VDD –0.5	—	—	V
		V_{OL}	VDD = 3.3V, IOL = 0.1mA VDD = 5.0V, IOL = 0.1mA	—	—	0.5	V
Power-on reset	VDD	V_{RES}	*2)	0.9	1.7	2.6	V
Dynamic supply current	VDD & VCC	I_{D1}	VDD = 3.3V, No Operation *3	—	—	400	μA
		I_{D2}	VDD = 5.0V, No Operation *3	—	—	600	μA

*1) Applicable to the following pins:
BLANK, SET, H, M, A/C, and COL_SEL, DISP_SEL, SW_EN_SEL, DU_SEL, TEST

*2) Do the followings to operate the power-on reset circuit properly:
- Make a slope of a rise time of VCC/VDD equal to or smaller than 28.7V/ms.
- Connect a smoothing capacitor of 1000 pF ±20% or more between the VDD pin and GND.

*3) f = 4.194304 MHz, open inputs, and non-loaded outputs.

POWER-ON/OFF TIMING



- Connect VDD and VCC pins externally to provide the equal potential.
- To prevent IC erroneous operation, keep the power ON/OFF timing.

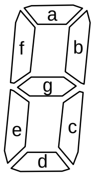
FUNCTIONAL DESCRIPTIONS

Time Base

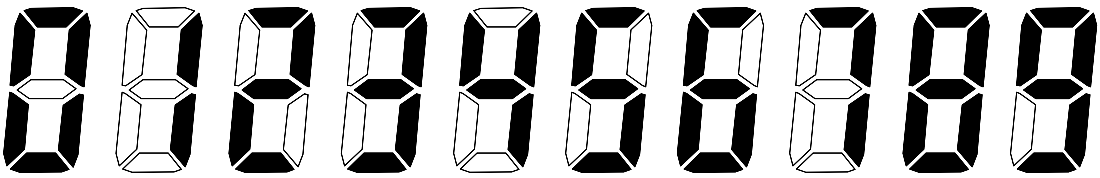
A 4.194304MHz crystal oscillation circuit (including an amplifier and a feedback resistor) is built in the LSI

* Keep the crystal and external capacitors as close to this LSI as possible to minimize wiring for connections.
* The values of external components, such as a crystal and capacitors, should be determined including capacitance of user's circuit boards. It is recommended to contact a crystal manufacturer.

7-Segment Display Format



(7 segments)

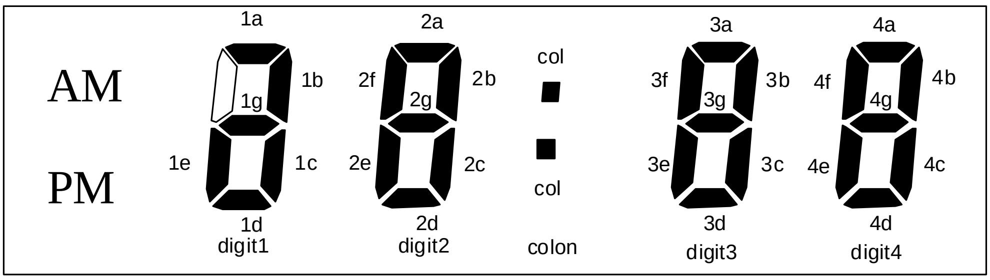


Display Device

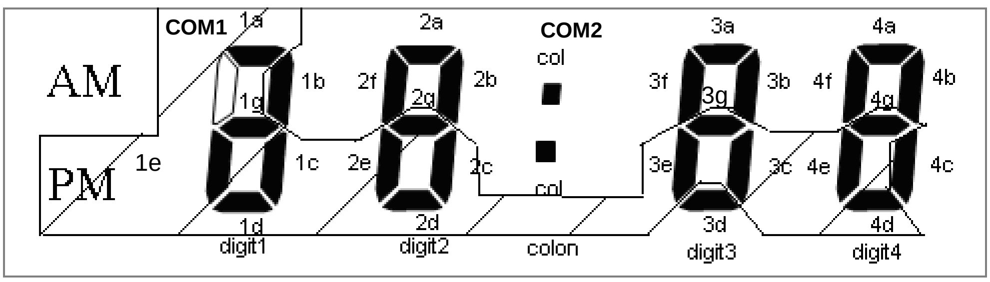
1/2-duty dynamic or static LCDs

Relationship between COM Output and Display

Static mode



Dynamic mode



Driver Connection with LCD

Pin	1/2 Duty		Static
COM1	COM1	—	COM1
COM2	—	COM2	—
SEG1	PM	AM	AM
SEG2	1a, 1g, 1e, 1d	4c	PM
SEG3	1c	1b	1a, 1g, 1e, 1d
SEG4	2e	2f	1b
SEG5	2g	2a	1c
SEG6	2d	2b	2e
SEG7	2c	col	2f
SEG8	3e	3f	2a
SEG9	3g	3a,3d	2g
SEG10	3c	3b	2b
SEG11	4e	4f	2c
SEG12	4g	4a	2d
SEG13	4d	4b	col
SEG14	—	—	3e
SEG15	—	—	3f
SEG16	—	—	3a, 3d
SEG17	—	—	3g
SEG18	—	—	3b
SEG19	—	—	3c
SEG20	—	—	4e
SEG21	—	—	4f
SEG22	—	—	4a
SEG23	—	—	4g
SEG24	—	—	4b
SEG25	—	—	4c
SEG26	—	—	4d

Display Mode
4-digit hour and minute display in 24/12 -hour system
Hour display 1 to 12 or 0 to 23
Minute display 00 to 59
Time is not displayed when the most significant digit is 0 (Most Significant Digit Zero Suppressing function)

24-hour display	12-hour display
1:00	AM 1:00
2:00	AM 2:00
3:00	AM 3:00
4:00	AM 4:00
5:00	AM 5:00
6:00	AM 6:00
7:00	AM 7:00
8:00	AM 8:00
9:00	AM 9:00
10:00	AM 10:00
11:00	AM 11:00
12:00	PM 12:00
13:00	PM 1:00
14:00	PM 2:00
15:00	PM 3:00
16:00	PM 4:00
17:00	PM 5:00
18:00	PM 6:00
19:00	PM 7:00
20:00	PM 8:00
21:00	PM 9:00
22:00	PM 10:00
23:00	PM 11:00
0:00	AM 12:00

Time Adjustment
Hour/minute fast-forward function
The hour and minute digits can be fast forwarded separately. The H (Hour setting)/M (Minute setting) pins fast forward the hour/minute digits. One push counts one hour/minute. When the hour/minute switch is continuously pressed, the hour/minute digit is incremented at 2Hz.
The H and M pins are high (inactive state) by the pull-up resistors when the pins are open.
These pins are active when driven at a “L” level externally.
The hour and minute digits can be adjusted at the same time.
The lower counters continue to operate regularly while the hour digit is adjusted, but a carry from the minute to hour digit is not performed.
A carry to the hour digit is not performed while the minute digit is adjusted.

Zero Adjustment Function (±30 minute reset to zero)

The SET (Zero adjustment) pin is held at a “H” level (inactive state) with a pull-up resistor when the pin is open. The minute and second digits are reset to 00’00” when the SET pin is driven at a “L” level externally, while the hour digit is unchanged or 1 is added to the hour digit.
If the minute digit is less than 30 minutes, the hour digit is unchanged.
When the minute digit exceeds 30 minutes, 1 is added to the hour digit.

<Examples of Zero Adjustments>

(X−1) hours 30 minutes 00 seconds
X hours 00 minutes 00 seconds
(X) hours 29 minutes 59 seconds

→ X hours 00 minutes 00 seconds

(X) hours 30 minutes 00 seconds
X hours 59 minutes 59 seconds
(X+1) hours 29 minutes 59 seconds

→ (X+1) hours 00 minutes 00 seconds

Blanking of Display

Display ON/OFF pin. "L" level: Display Off, “H" level: Display On.

64 Hz Pin

This is the output pin for adjusting the oscillation frequency. This pin constantly outputs a 64 Hz signal.

External Reset

This LSI can be reset by placing the A/C pin at a “L” level, and the display is off when the pin is at a “L” level. After reset, the display starts from “1: 00”.

DISP_SEL

Pin for selecting the 12-hour system with AM/PM or the 24-hour system. The 12-hour system with AM/PM is selected when the pin is driven at a “L” level and the 24-hour system is selected when the pin is driven at a “H” level.

SW_EN_SEL

Adjustment enable pin. The H, M, and SET pins are disabled by driving the SW_EN_SEL pin at a “L” level externally.

DU_SEL

LCD duty selection pin. The static mode is selected when the pin is driven at a “L” level, and the 1/2-duty dynamic mode is selected when the pin is driven at a “H” level.

BIAS

Supply voltage pin for the middle level voltage of the common outputs.
The value of BIAS is calculated by the following formula:

BIAS=VCC/2

In the static display mode, this pin should be open.

Xin, Xout

Crystal oscillation pins for connecting a crystal and the capacitors (Cin and Cout) externally.

COM1, COM2

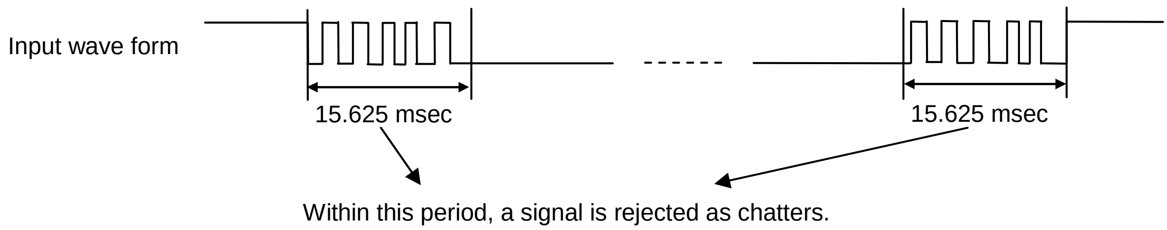
Output pins for LCD common.

Driving method	Frame frequency
Static	64Hz
1/2 Duty	64Hz

TEST pin
Pin for manufacturer testing.
The pin should be left open or fixed at a “H” level when not used.

Power-On Reset
The power-on reset circuit built in this device eliminates the need for providing an external reset circuit.

Chatter Rejection
The chatter rejecting circuits are connected to the H, M, and SET pins.
A signal less than 15.625 msec is rejected as chatters.



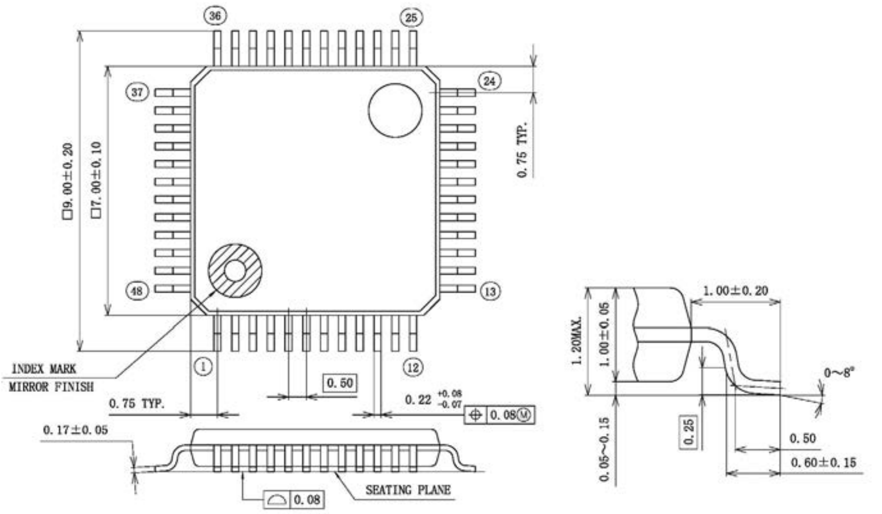
Colon Flashing/Lighting Selection
Flashing or lighting of colon is selected by the COL_SEL pin.

COL_SEL	Operating mode
L	Flashing at 1 Hz
H	Lighting

PACKAGE DIMENSIONS

(Unit: mm)

TQFP48-P-0707-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.13 TYP.
Rev. No./Last Revised	1/Oct. 22, 2007

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9098B-01	Aug. 10, 2010	–	–	Final edition 1

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